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Micro-Power Low-Area Multichannel Integrated Circuits for Precise Measurement of Ionizing Radiation Energy

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ROZPRAWA DOKTORSKA

Mikromocowe, niskopowierzchniowe, wielokanałowe układy scalone przeznaczone do precyzyjnego pomiaru energii promieniowania jonizującego

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Abstract

X-rays and computed tomography are undeniably one of the foundations of modern medical diagnostics. Over the years, they have undergone many modifications to offer the today's possibilities, and the process is still ongoing.

The basis of modern imaging is the measurement of X-ray intensity (similar to black and white photography). Still, there are materials differing in the chemical composition and the mass density which can generate identical images. Therefore, their differentiation may pose serious difficulties. Still, such materials show different transparency levels when exposed to various X-ray energies. Therefore, it is crucial to distinguish such energies (as in color photography) so as to identify particular tissues. Such possibilities are provided by single photon counting (SPC) systems.

The aim of the research summarized in this dissertation was to propose a new method of signal processing in the reading channel of a hybrid pixel detector operating in the SPC mode. The device produced in the 28 nm submicron CMOS technology was expected to provide the precise energy measurement, while ensuring the high spatial resolution at the lowest possible power consumption.

The dissertation presents three approaches to the photon energy measurement in a single pixel. They employed, respectively: multiple discriminators, an analog-to-digital converter, and an asynchronous charge compensation loop using current pulses. The last two methods were tested in the fabricated integrated circuits, and then compared in terms of speed, power consumption, area occupancy and energy measurement resolution.

The final integrated circuit containing 100 pixels of $50\,\mu m \times 50\,\mu m$ in size has proved successful. The prototype reveals the high spatial resolution. The method of the charge compensation with current pulses allows for the effective measurement of radiation energy. Moreover, it ensures the fast signal processing and the low power consumption. Thus, it constitutes a promising solution for detectors applied in multi-energy computed tomographs.

Streszczenie

Prześwietlenie rentgenowskie oraz tomografia komputerowa, stanowią niezaprzeczalnie jeden z fundamentów współczesnej diagnostyki medycznej. Na przestrzeni lat przeszły one wiele modyfikacji, aby móc zaoferować dostępne dziś możliwości, a proces ten trwa nadal.

Podstawą współczesnego obrazowania jest pomiar intensywności promieniowania (podobnie jak w czarno-białej fotografii). Stwarza to jednak pewne trudności w odróżnieniu niektórych tkanek na zarejestrowanym obrazie, ponieważ materiały różniące się składem chemicznym, ale również gęstością atomów, mogą generować identyczny obraz. Są one jednak transparentne dla promieni o różnych energiach. Rozróżnienie tych energii (jak w fotografii kolorowej) pozwoliłoby także zidentyfikować poszczególne tkanki. Takie możliwości dają systemy zliczające pojedyncze fotony (ang. *single photon counting*, SPC).

Celem badań, których podsumowaniem jest niniejsza rozprawa, było zaproponowanie nowego sposobu przetwarzania sygnału w kanale odczytowym hybrydowego detektora pikselowego pracującego w trybie SPC, pozwalającego na precyzyjny pomiar energii, zapewniającego jednocześnie wysoką rozdzielczość przestrzenną przy możliwie niskim poborze mocy w submikronowej technologii CMOS 28 nm.

W rozprawie zaprezentowano trzy podejścia do pomiaru energii fotonu w pojedynczym pikselu, takie jak: wykorzystanie wielu dyskryminatorów, zastosowanie przetwornika analogowo cyfrowego oraz użycie asynchronicznej pętli kompensacji zebranego ładunku przy pomocy impulsów prądowych. Dwie ostatnie metody zostały przetestowane w wyprodukowanych układach scalonych, a następnie porównane ze sobą pod kątem szybkości pracy, poboru mocy, zajętości powierzchni oraz rozdzielczości pomiaru energii.

Metoda kompensacji ładunku impulsami prądowymi została zaimplementowana w prototypowym układzie scalonym zawierającym 100 pikseli o wymiarach $50\,\mu m \times 50\,\mu m$, zapewniających wysoką rozdzielczość przestrzenną. Na podstawie przeprowadzonych testów wykazano, że pozwala ona na efektywny pomiar energii promieniowania przy jednoczesnym zapewnieniu szybkiego przetwarzania sygnału i niskiego poboru mocy. Stanowi zatem obiecujące rozwiązanie dla detektorów do wieloenergetycznych tomografów komputerowych.

Contents

List of Symbols

Symbol	Description	Unit
c	speed of light in vacuum (3×10^8)	m/s
C_{DB}	MOSFET small-signal drain-bulk capacitance	F
C_{DS}	MOSFET small-signal drain-gate capacitance	F
e^-	electron	
E_{eh}	electron-hole creation energy	eV
E_{ph}	photon energy	eV
f_T	MOSFET transit frequency	Hz
g_m	MOSFET small-signal transconductance	S
h	Planck constant (6.626×10^{-34})	J·s
λ	photon wavelength	m
N_h	number of electrons	
N_e	number of holes	
r_O	MOSFET small-signal output resistance	Ω
V_{TH}	discriminator threshold voltage	V

Abbreviations and Acronyms

A/D	Analog-to-Digital
AC	Alternating Current
ADC	Analog-to-Digital Converter
ASIC	Application-Specific Integrated Circuit
CCD	Charge-Coupled Device
CDS	Correlated Double Sampling
CdTe	Cadmium Telluride
CMOS	Complementary MOS
CSA	Charge Sensitive Amplifier
CT	Computed Tomography
CZT	Cadmium Zinc Telluride
DAC	Digital-to-Analog Converter
DC	Direct Current
DNL	Differential Non-Linearity
ENC	Equivalent Noise Charge
ENOB	Effective Number of Bits
FWHM	Full Width at Half Maximum
GBW	Gain-Bandwidth Product
HDL	Hardware Description Language
HgI_2	Mercuric Iodide
IC	Integrated Circuit
INL	Integral Non-Linearity
LSB	Least Significant Bit

MOM	Metal-Oxide-Metal
MOS	Metal-Oxide-Semiconductor
MOSFET	MOS Field-Effect Transistor
MSB	Most Significant Bit
NIC	Negative Impedance Converter
NMOS	N-channel MOSFET
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PDH	Peak Detect and Hold
PMOS	P-channel MOSFET
PSO	Particle Swarm Optimization
PVT	Process, Voltage and Temperature
RAM	Random Access Memory
REMIC	Radiation Energy Measuring Integrated Circuit
SAR	Successive-Approximation Register
SNR	Signal-to-Noise Ratio
SPC	Single Photon-Counting
SPICE	Simulation Program with Integrated Circuit Emphasis
T&H	Track-and-Hold
TDC	Time-to-Digital Converter
ToT	Time-over-Threshold
TSMC	Taiwan Semiconductor Manufacturing Company
TSV	Through-Silicon Via
UNSCEAR	United Nations Scientific Committee on the Effects of Atomic Radiation

Chapter 1

Introduction

Probably no one needs to be convinced how important a role the sight plays in the perception process. Light from the sun or another source is reflected from some objects and penetrates through others, outlining shapes and colors. The eye lens focuses the incident rays and forms an image on the retina. This image is detected by the corresponding receptors (cones and rods), and then, in the form of impulses sent to the brain.

Visible light is only a narrow range of the electromagnetic radiation spectrum. In the higher energy range, among others, X-rays are distinguished. They have a greater ability to penetrate various materials, including the human body, just as visible light penetrates objects that are at least somewhat transparent, showing the insides. Such a process occurs in the immensely popular and widely used radiological examinations. The X-rays from an appropriate source fall on the patient's body, partially penetrate it, and then fall on a detector that can "see" this kind of light. The design of such a detector, especially for medical applications with emphasis on a radiation energy measurement, is the subject of this thesis.

The thesis takes the form of a publication series, including the following positions, organized by the topics that will be further discussed:

[1] Piotr Kaczmarczyk and Piotr Kmon, "Continuous-time discriminator design in CMOS 28 nm process," in *Proceedings of 26th International Conference "Mixed Design of Integrated Circuits and Systems" MIXDES*, Rzeszów, 2019, pp. 186–189. DOI: 10.23919/MIXDES.2019.8787153

[2] Piotr Kaczmarczyk and Piotr Kmon, "8 b 10 MS/s differential SAR ADC in 28 nm CMOS for precise energy measurement," *Journal of Instrumentation*, vol. 17, no. 03, p. C03027, 2022. DOI: 10.1088/1748-0221/17/03/C03027

[3] Piotr Kaczmarczyk and Piotr Kmon, "Dynamic comparator design in 28 nm CMOS," *International Journal of Microelectronics and Computer Science*, vol. 9, no. 4, pp. 149–154, 2018, [Online]. Available: https://ijmcs.dmcs.pl/vol.-9-no.-4, ISSN: 2080-8755

[4] Piotr Kaczmarczyk and Piotr Kmon, "Projekt dynamicznego komparatora z korekcją napięcia niezrównoważenia w dziedzinie czasu (design of a dynamic comparator with time-domain offset calibration)," *Przegląd Elektrotechniczny*, vol. 96, no. 12, pp. 121–124, 2020. DOI: 10.15199/48.2020.12.23

[5] Piotr Kaczmarczyk and Piotr Kmon, "Automated, adaptive, fast reset circuit for wide-energy range detector front-end," *Journal of Instrumentation*, vol. 18, no. 03, p. C03010, 2023, ISSN: 1748–0221. DOI: 10.1088/1748-0221/18/03/c03010

[6] Piotr Kaczmarczyk, "Automatic design of a cascoded-inverter-based charge-sensitive amplifier using g_m/I_D technique and particle swarm optimization in 28 nm CMOS," in *Proceedings of 30th International Conference "Mixed Design of Integrated Circuits and Systems" MIXDES*, Kraków, 2023

[7] Piotr Kaczmarczyk and Piotr Kmon, "Fast asynchronous 12-bit in-pixel ADC for high spatial resolution multi-energy radiation detectors in CMOS 28 nm," *IEEE Transactions on Circuits and Systems—Part II: Express Briefs*, 2023, sent for review

The complete publications are included in Chapter 3, where I also describe my detailed contribution to each of them. All the publications are authored only by my Supervisor and me, so wherever the form *we* is used in the dissertation, it refers to the two of us.

Besides the publication series, the thesis consists of two additional chapters. In Chapter 1 I briefly explain the use of radiation detectors in medical imaging and present some detector classification. I also give an insight in a front-end electronics channel architecture and list benefits of the particle energy measurement. Next I cover the state of the art in the energy-resolved integrated circuits (ICs). Finally, I pose research problems with proposed solutions. There I briefly describe our contribution to the discipline and point out what is the scientific novelty.

In Chapter 2 I lead the reader through the publication series, putting each paper in a big picture of the energy measurement topic. I explain a mutual relationship between the work performed in the particular articles and how it contributed to the final project outcome.

1.1 Background, motivation and state of the art

1.1.1 Background

Since the Nobel Prize-winning Wilhelm Röntgen's discovery in 1895, X-rays have been increasingly frequently used in medical diagnostics. Two main imaging modalities are: projection radiography (often simply called *X-ray*) which produces two-dimensional images of the transmitted X-ray intensities, and computed tomography (CT) providing three-dimensional images of the linear attenuation coefficient distribution within a patient [8]. According to the reports of the United Nations Scientific Committee on the Effects of Atomic Radiation (UNSCEAR) [9], [10], the annual global number of radiation-involving examinations for period 1997–2007 was 3.6 billion and for period 2009–2018 reached 4.2 billion. (Fig. 1.1). That shows both its high importance in patients diagnostics and the dynamically growing market.

At the same time, the effective radiation dose per capita has diminished from 0.65 mSv to 0.57 mSv. One of the reported reasons for this phenomenon is a technological advance in radiation detectors. Many conventional film-screen systems have been replaced with digital techniques, and new detectors with the higher detective quantum efficiency are being developed continuously.

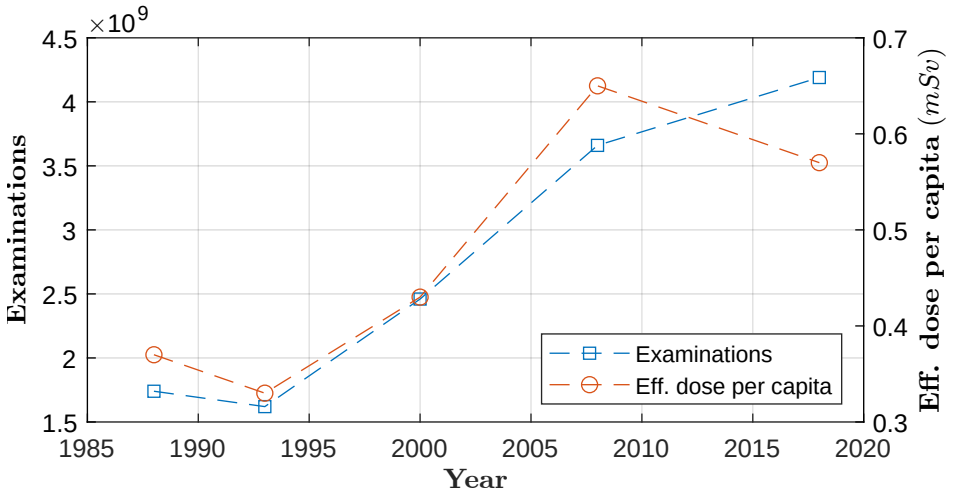


Figure 1.1: Number of radiation-involving examinations and effective dose (excluding radiotherapy) per capita according to the UNSCEAR reports.

Considering the way the ionized particle energy is transferred to the detecting system, one can distinguish *indirect-* and *direct-conversion sensors* [11]–[13]. In the first case, a photon impinging a sensing material (e.g. a scintillator) excites visible light flashes. These in turn reach a photodiode combined with a readout application-specific integrated circuit (ASIC). In the direct conversion, the interaction of the particle with the detector material results in the creation of an electron-hole pair. Thanks to the present electric field, the charge carriers flow into the sensor electrodes, one of which is connected directly to the readout channel. The carriers of one sign, e.g. electrons in a cadmium telluride (CdTe) detector (commonly used in medicine), are fed to the front-end amplifier, forming a current pulse for further processing, while the opposite charge carriers flow towards the other electrode.

The predominant advantages of the direct-conversion detectors are the better spatial resolution and conversion efficiency. On the other hand, the indirect detectors allow working with much higher input energies, thanks to the materials used for photons energy conversion [12].

The average number of the created electrons N_h and holes N_e depends directly on the ratio of the energy of the impinging photon E_{ph} and the electron-hole creation energy E_{eh} of a particular sensor material. This feature is crucial for building the energy-resolved imaging systems.

$$N_h = N_e = \frac{E_{ph}}{E_{eh}} \tag{1.1}$$

Let me present an example. The most popular X-ray detecting machine, i.e. a commonly used dental imaging system, emits radiation of an average energy of 40 keV. Given the CdTe semiconductor sensor has the pair creation energy of 4.43 eV, the number of pairs created by a single particle equals 9029. Typical energies used in medicine are presented in Table 1.1.

However, to make use of (1.1), the appropriate readout electronics has to be involved. Regarding the type of the signal processing architecture in the readout electronics, detectors can be classified as *integrating* or *single photon counting (SPC)*.

The operation principle of the integrating system is to collect the incoming charge for a certain period of time and to read the summed value periodically. Yet, the information about the individual photon energy

Table 1.1: General specification for X-ray imaging and CT [14].

	Count rate Gc/(s mm^2)	**Pixel pitch** µm	**Max energy** keV
Mammography	0.05	typ. 85	28–40
General X-ray	0.001–0.5	typ. 150	70–120
Computed tomography	1	55–1 000	80–140

is lost. Moreover, not only the particle energies are integrated, but also the background and electronic noise. Such an operation mode also limits the dynamic range. Still, an unquestionable advantage of integrating detectors is their ability to maintain a linear operation even at high fluxes [13].

On the other hand, the SPC detectors process photons one by one. Thus, they maintain the information about the impingement time and the deposited energy, plus the data regarding the intensity and position. On the contrary, the integrating detectors keep only the latter two. Moreover, when distinguishing the energy level, some non-interesting photons of energy below a certain value can be disregarded and the background can be cut-off by means of a *discriminator*[1]. All these factors dramatically increase the signal-to-noise ratio (SNR), improving the registered image quality [12], [13]. Thanks to this phenomenon, the intensity of a radiation source (e.g. an X-ray tube) can be lowered, reducing the dose absorbed by a patient. It is of great importance due to increasing numbers of radiological investigations [10]. A known disadvantage of the SPC detectors is the limited operation speed related to the pulse processing time. However, there are some reported techniques allowing to partially address this issue, e.g. the analog memory [15], [16]. Moreover, the complementary metal-oxide-semiconductor (CMOS) production has progressed. The metal-oxide-semiconductor field-effect transistor (MOSFET) channel length was reduced. Therefore, the transit frequency f_T makes it possible to obtain faster and more advanced devices.

The most common sensor architectures are strips (to register one-dimensional image at a single scan) and pixels (two-dimensional imaging at a single scan). The spatial resolution of an image depends on the sensor pitch. If the readout ASIC active area fits exactly to the sensor pitch, the sensing material can be placed directly on a chip and connected via bump-bonding. Otherwise, the connection can be realized via an interposer.

Even though the indirect sensors with integrating electronics are the most popular in today medical X-ray imaging [13], there are many research projects on the direct converting SPC system application [17]–[20]. For instance, the first clinical SPC CT system was already reported [21]. The research aims at developing the SPC systems to detect as high and as intense incoming photons energies as the integrating system does. This requires not only modern technologies but new techniques on signal processing as well.

Having all the issue complexity in mind, my research mainly focused on hybrid pixel detectors consisting of SPC readout electronics intended to work with a direct conversion sensor. Only these solutions will be further discussed in the thesis. Fig. 1.2 presents a simple SPC readout channel. An ionized particle hits the sensor (presented as a reverse-biased diode), creating electron-hole pairs. Carrier of one type are fed to the

[1]This is a jargon name for a comparator in such an application

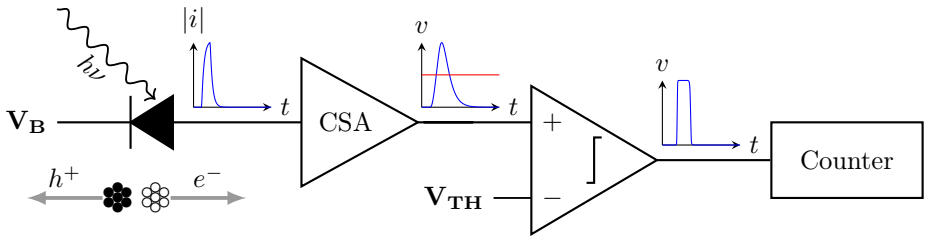


Figure 1.2: Simple SPC readout channel.

readout electronics as a current pulse, while the other type is sunk by the bias supply voltage. The pulse is then amplified by a charge sensitive amplifier (CSA). If the output pulse exceeds the discriminator threshold V_{TH}, a logical *one* is present on the discriminator output, thereby incrementing a digital counter by one. Thus, the value stored in the counter represents the beam intensity expressed in photons whose energy is above a certain level.

1.1.2 Motivation

Although the use of the integrating detectors allows for more intense radiation beams, the benefits of switching to the SPC mode are remarkable. The ability to cut off the background noise improves the image quality, and the time and energy measurement can carry valuable diagnostic information [8], [13], [22].

X-ray radiation is a form of high-energy electromagnetic radiation of wavelengths ranging from 10 pm to 10 nm. For comparison, the visible light spectrum spans from 380 nm (blue) to 700 nm (red). The photon energy E_{ph} and its wavelength λ are related by the following formula:

$$E_{ph} = \frac{hc}{\lambda}, \tag{1.2}$$

where h is Planck constant and c is speed of light. The channel from Fig. 1.2 has one discriminator to register all photons whose energy exceeds a certain level. This way the intensity image can be created. It can be compared to black-and-white photography. However, if there are more energy thresholds, photons in specified energy ranges (similar to visible colors) can be distinguished. This case can be compared to color photography, and for this reason, energy-resolved CTs are sometimes called *color CT* by analogy, or *spectroscopic CT*.

To provide some insight, look at Fig. 1.3a. Let us say, you want to have a lime drop. Are you able to pick which of them is of lime flavor, if any? Then look at Fig. 1.3b — is the choice easier now? A color (energy) can carry a lot of useful information. This issue is even more important in medicine. In a monoenergetic CT scan, materials of different elemental composition can be represented by identical or very similar pixel values (depending on the mass density), making it difficult or impossible to classify different types of tissue [22]. As a classic example, [22] quotes *the difficultly in differentiating between calcified plaques and iodine-containing blood*. However, by measuring the linear attenuation coefficient of the materials at two different energies, their decomposition becomes easier.

(a) (b)

Figure 1.3: Drops of different flavors.

The first benefits of *dual-energy* CT were already reported in 1973 by the inventor of the first commercially viable CT scanner, Sir Godfrey Hounsfield [23]. He was the Nobel Prize winner together with Allan MacLeod Cormack. Thenceforth, several approaches to the dual-energy CT have been developed. According to [22], one can distinguish:

- Temporally sequential scanning of the entire scan volume
- Temporally sequential scanning of a single axial rotation
- Rapid switching of the X-ray tube potential
- Multilayer detector
- Dual X-ray sources
- Photon-counting detectors.

The last one opens up new horizons for medical imaging, facilitating *multi-energy* scanning.

Thanks to the transistor down scaling it is possible to pack more functionality into a single ASIC or even into a single pixel, transferring some off-chip data processing into the silicon. The on-chip preprocessing reduces the amount of data that have to be transferred out of the chip, thus improving the speed and decreasing the power consumption of the system. The reduced transistor size makes the pixel size smaller, enhancing the spatial resolution of a detector.

Another advantage of the technological scaling is the higher transistor operation frequency, particularly manifesting in a shorter digital CMOS switching time. However, the analog design does not benefit as much from the newer processes as the digital one. Indeed, some parameters deteriorate, e.g.: the transconductance g_m lowers and thus the intrinsic gain of a transistor. Also, the supply voltage decreases, reducing the available headroom required for the transistor saturation. That state of things promotes to acquire the analog signal with all the available precision and switch to the digital domain as soon as possible.

All the described facts, observations and possibilities inspired me to research and develop an SPC detector for color imaging in a modern available CMOS technology.

1.1.3 State of the art

The energy measurement in hybrid pixel SPC detectors has been most commonly performed in the following manners so far [15]:

- using multiple thresholds (energy windows)
- measuring the CSA pulse time-over-threshold (ToT)
- by means of an analog-to-digital converter (ADC)
  - one per chip
  - one per group of channels (e.g. a column of pixels)
  - one per single channel.

Each of these solutions has its pros and cons, and differs in resolution, time of conversion, power consumption and silicon area.

Multiple thresholds

This method is very common and quite obvious, as it basically involves multiplication of the discriminator and the counter for each threshold, regarding the circuit from Fig. 1.2. It is similar to the construction of a flash analog-to-digital converter (ADC), but usually with no encoder between the array of discriminators and counters. When a photon of a certain energy hits the detector, all the discriminators fire when the particular threshold levels are exceeded, incrementing their counters. Thus, the number of photons in particular energy bins can be calculated as a difference between the neighboring counters. However, it leads to the uneven use of the counters and to the faster overflow of the lowest-energy-related one.

Flash ADCs are renowned for their high conversion speed but also for the considerable power and area consumption. Each additional bit of resolution implies doubling those values. Moreover, discriminators are usually continuous-time comparators, requiring a static bias current. The typical pixel dimension varies from $500\,\mu m \times 500\,\mu m$ to even $50\,\mu m \times 50\,\mu m$. As a result, the resolution enhancement of the discriminator-based multi-threshold system is strictly constrained by the available pixel area and the power budget.

For this reason, multi-discriminator architecture is widely used in dual-energy systems and less frequently in multi-energy ones. As examples of solutions containing two discriminators, the following can be highlighted: *Medipix3* from *CERN* [24], [25], *Pixie II* and *Pixie III* from *Pixirad* [26], [27], *PXD18k*, *PXD23k*, *UFXC32k* and *LNPIX* from *AGH University* [28]–[31], *IBEX* from *Dectris* [32], *Actina* from *CEA-Leti* and *Siemens* collaboration [33], [34] or *XPAD3-C* from *CPPM* [35].

Channels with 4 independent discriminators are available in *ChromAIX* from *Philips* [36], *MC1* from *Siemens* [37], *MPIX* from *AGH* [38], detectors from: *Hosei University* and *Telesystems Co.* [39], and *DxRay* and *Interon* [40], and also in the already mentioned *IBEX*, working in the so-called *merging mode* (combining four regular pixels into one larger pixel) [32].

Phillips in *ChromAIX2* uses 5 discriminators [41], *ERICA* has 6 of them [42], and *Medipix3* up to 8, while working in the *spectroscopic mode* (similar to the *IBEX*'s *merging mode*) [24], [25].

Time-over-threshold

The time the CSA output pulse spends over the discriminator threshold is in general proportional to the input signal amplitude, being in turn directly proportional to the incoming photon energy. Therefore, by measuring the duration of a comparator response, the information about the energy of a detected particle can be extracted [43], [44]. This method is known as the time-over-threshold (ToT).

In a basic approach, the feedback capacitor is discharged by a resistive element which leads to the exponential behavior of the CSA pulse. Such a behavior then results in the non-linear relationship between the energy and the discriminator pulse width. If the resistive component is replaced with the one providing a constant current, the conversion characteristics become more linear [45]–[47]. The ToT method is reported as one of the fastest and simplest in multichannel readout systems, while maintaining low power consumption [48], [49]. However, the feedback and the CSA nonlinear behavior degrade the time-energy linearity, especially at low threshold values.

In medical applications, readout ASICs from the *Timepix* family, designed in *CERN*, are especially popular [50]–[52].

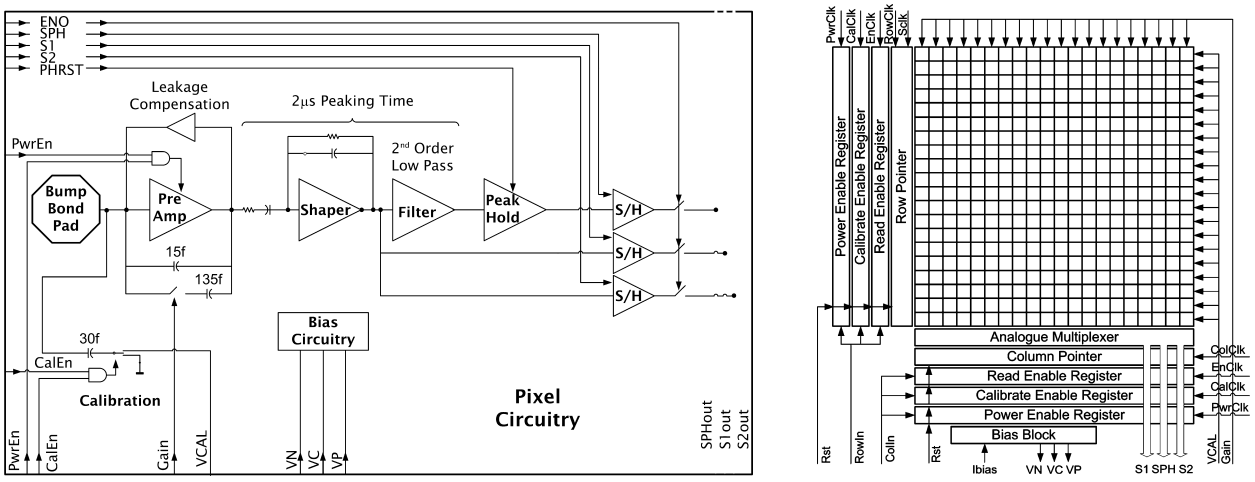
Additionally, the ToT implementation requires a pulse counter with an *enable* input controlled by the discriminator. Pulses to the counter must be provided by an oscillator. This element can be placed either locally in each pixel (imposing an increase in the overall power and area consumption, and contributing to the pixel-to-pixel mismatch) or globally for all the pixels (requiring the additional fast clock signal distribution through the entire chip).

Analog-to-digital converters

Another common solution of the photon energy measurement is the use of an analog-to-digital converter. It has become especially popular in the last decade along with the transistor down-scaling. Some classification can be performed regarding two aspects: the location of the ADC relative to the readout electronics in the pixel, and the applied ADC architecture.

Off-chip conversion There are some designs which perform only the analog signal processing in a pixel and expose the analog result outside the chip. An example is the *HEXITEC* ASIC designed in the 350 nm CMOS with the 250 µm pixel size [53], [54]. The authors propose to perform the analog-to-digital (A/D) conversion off-chip or in the second chip, vertically integrated by through-silicon vias (TSVs). The pixel and chip architecture are presented in Fig. 1.4.

On-chip conversion As already mentioned in 1.1.2, the transistor feature size reduction allows more functionality to be placed in the same silicon area. This applies also to A/D converters whose various architectures are more and more frequently implemented in a single pixel to improve the energy measurement capabilities. Some interesting examples of the in-pixel converter implementations are presented below.



(a) (b)

Figure 1.4: *HEXITEC*: (a) single pixel and (b) the entire chip architecture. (Source: [53])

In-pixel TDC-based ADC Scientists from the *University of Illinois* and *Ajat*[2] describe a time-to-digital converter (TDC)-based ADC placed in every 350 µm × 350 µm pixel of an energy-resolved SPC detector for gamma ray imaging, fabricated in the 350 nm CMOS [55]. The front-end channel (Fig. 1.5) consists of an alternating current (AC)-coupled CSA, a peak detect and hold (PDH) circuit, a discriminator and a 10-bit counter to count photons or measure energy. The shaping time of the amplifier is about 1 µs and its gain is 10 µV/e$^-$. The operation principle of this TDC-based ADC is as follows. The CSA output is fed simultaneously to the discriminator and the PDH. The rising edge of the discriminator output is a *start* signal for the TDC. At the same time, a ramp generator starts as well. When the ramp meets the PDH voltage level, the *stop* signal for the TDC is generated. Therefore, the TDC output is proportional to the signal amplitude. This method resembles ToT, but the attempts to linearly discharge the capacitor were replaced by a linearly increasing second voltage to "catch up" with the CSA peak amplitude. The ramp generator consists of an 8-bit digital-to-analog converter (DAC) controlled by a 10 MHz clock. Depending on the required count rate, the conversion resolution can be selected from 4 to 8 bits, by changing the ramp step. Performing a 6-bit conversion takes a maximum of 6.4 µs while for 8-bit it lasts 25.6 µs. It results in the count rates of 0.8 Mc/s at 6-bit A/D conversion and 0.2 Mc/s at 8-bit one. The energy resolution measured with a cadmium zinc telluride (CZT) sensor is the 2.5 keV–3.5 keV full width at half maximum (FWHM) at 140 keV. The dynamic range is 35 keV–250 keV.

In-pixel SAR-like ADC Researchers from *KAIST* and *Samsung* present a sampling-based SPC detector with an in-pixel asynchronous successive-approximation register (SAR)-like ADC, manufactured in the 130 nm CMOS[3], aimed at working with a mercuric iodide (HgI_2) direct current (DC)-coupled detector [56]. The analog part is supplied from 3.3 V and the digital one from 1.2 V. Each 60 µm × 60 µm pixel contains

[2]Current *Direct Conversion*

[3]It is not clear what the authors mean saying that the *chip was fabricated in a* 0.13 µm/0.35 µm *7-metal standard CMOS process*. Perhaps, judging from the supply voltages, the analog part was designed with thick-oxide transistors with minimum allowable channel length of 350 nm.

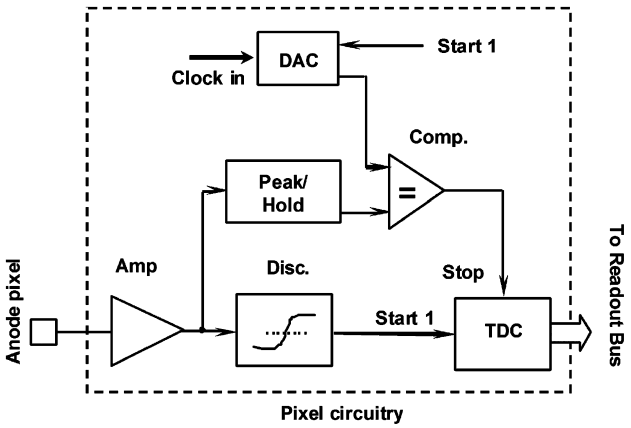


Figure 1.5: Pixel with a TDC-based ADC. (Source: [55])

a CSA equipped with a correlated double sampling (CDS) mechanism, an asynchronous switch-based self-reset circuit, a clock-less discriminator, an ADC, and three 15-bit counters. The CSA gain is 107 µV/e$^-$, the peaking time is below 200 ns and the falling slope time constant is set very high by an open metal-oxide-semiconductor (MOS) switch. The conversion starts when the discriminator fires. The discriminator V_{TH} input is replaced with the ADC's internal 4-level thermometer-code DAC. The CSA output is consecutively compared to each DAC level. If that level is exceeded, the corresponding counter is incremented. When the conversion is complete, the feedback capacitor is discharged in <150 ns by the switch reset optimized for the minimum charge-injection. Thanks to the linear DAC switching, the conversion can run simultaneously with the CSA pulse leading edge. The static power consumption per pixel amounts to 4.6 µW. The equivalent noise charge (ENC) equals 110 e$^-$ (1.57 keV in case of HgI_2) at 0.1 MHz of the input pulses frequency and 68 e$^-$ (0.97 keV) at 1 MHz. The minimum detectable charge is 290 e$^-$ (4.14 keV). The input energy measurements from 1.15 ke$^-$ to 7.4 ke$^-$ (16.4 keV–105.7 keV) are reported. Due to the purely resistive feedback, the detector leakage current is not compensated, and this issue is only partially solved by the preliminary discriminator threshold. Given the random character of the radiation particles arrival, the incidental part of the leakage current is integrated, leading to a variable CSA output offset voltage.

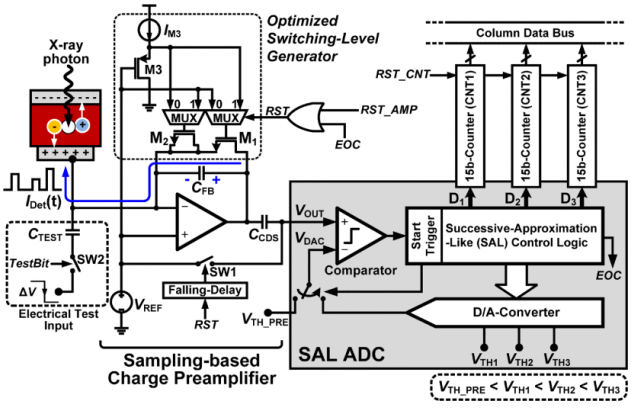


Figure 1.6: Pixel with a SAR-like ADC. (Source: [56])

In-pixel SAR ADC with energy histogram *MultiX* from *CEA* [16] and *Spectrum1k* from *AGH* [57] are very powerful designs. They reconstruct the energy histogram for each pixel with high precision. They both comprise a synchronous SAR ADC with 8 and 6 bits of resolution, respectively.

Spectrum1k [57] is manufactured in the 40 nm CMOS with the 75 µm × 75 µm pixel pitch. It is dedicated to work with both electrons and holes of charge from 2.2 ke$^-$ to 35 ke$^-$ in a *low-gain* configuration, or to 27 ke$^-$ in *high-gain*. Each channel (Fig. 1.7) contains a CSA with the Krummenacher feedback [58], a discriminator, a PDH circuit [59], an ADC, and a random access memory (RAM) composed of 64 × 12-bit counters. According to the simulation results, the CSA and the PDH cores consume 22 µA and 12 µA of a static current, respectively. The ASIC is able to work in two modes: driving the ADC input either directly from the CSA output or from the PDH. In one mode, the feedback equivalent resistance is set high (about 1 GΩ, not to affect the ADC conversion), and in the other it is about 4 MΩ (resulting in the signal processing in less than 100 ns). The pulse duration may vary from a few µs (in high feedback resistance mode) to several dozen ns. Whenever a photon is detected, depending on the mode, the CSA or the PDH output is sampled by the ADC, and the RAM counter of the address corresponding to the ADC output code is incremented. The ADC resolution in the *high-gain* configuration is about 500 e$^-$ and about 1.2 ke$^-$ in the *low-gain* one. The CSA gain values are around 20 µV/e$^-$ and 8.5 µV/e$^-$.

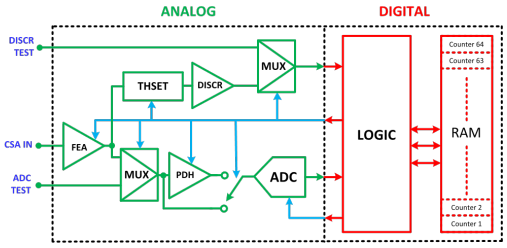


Figure 1.7: Block idea of *Spectrum1k* readout channel. (Source: [57])

MultiX [16] is fabricated in the 130 nm technology, capable of working at 8 Mc/s with a CdTe sensor, featuring the pixel size of 756 µm × 800 µm. The sensor leakage current (about 10 nA/pixel) is decoupled with a 40 pF capacitor and a 10 MΩ resistor. The aimed energy range is 20 keV–200 keV (resulting in charge 4.5 ke$^-$–45 ke$^-$). The channel is quite complex (Fig. 1.8). It consists of a CSA, a programmable sampled shaper, an amplifier, a derivation circuit, a discriminator, spectral cleaning blocks, an 8-seat analog queue, a 10 MS/s 8 bit SAR ADC, a 256 words of 6 bits memory, and a full adder. The CSA feedback includes a 50 fF capacitor and a 10 MΩ resistor, causing a staircase-like voltage response to a particle hit. This signal is then subtracted from the delayed CSA output in the shaper with programmable delay (5 ns–50 ns). Next, the shaper output is amplified, derived, and fed to the discriminator. In the spectral cleaning blocks, the invalid events are rejected. An average time between two consecutive photons is assumed at 100 ns. Yet, given the Poisson probability distribution of X-ray radiation [15], it may shrink even to 40 ns. The analog queue solves the problem and, additional, it relaxes the ADC speed requirement. The derived voltage signal, whose value is proportional to the detected photon energy, is converted to an 8-bit digital word. It thereafter provides an address to the memory. The stored value from the memory is read, incremented in the full adder, and put back to the memory. The ADC least significant bit (LSB) is around 1 keV. The power consumption, however, is substantial, reaching 10 mW/pixel.

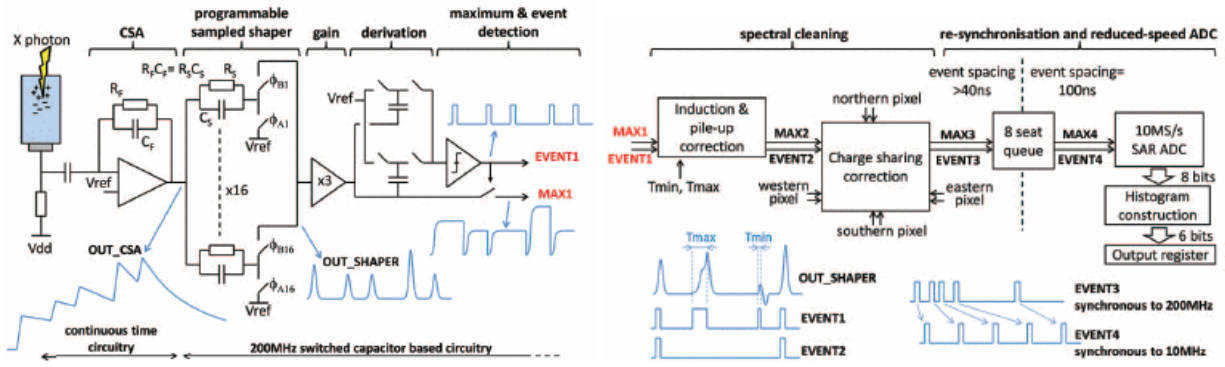
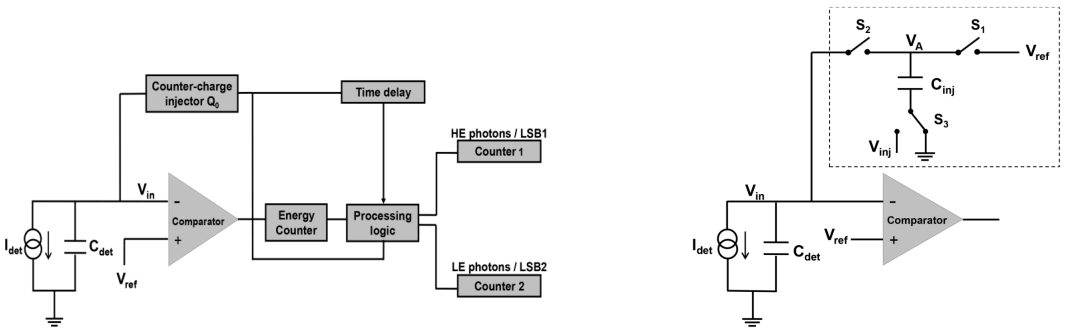


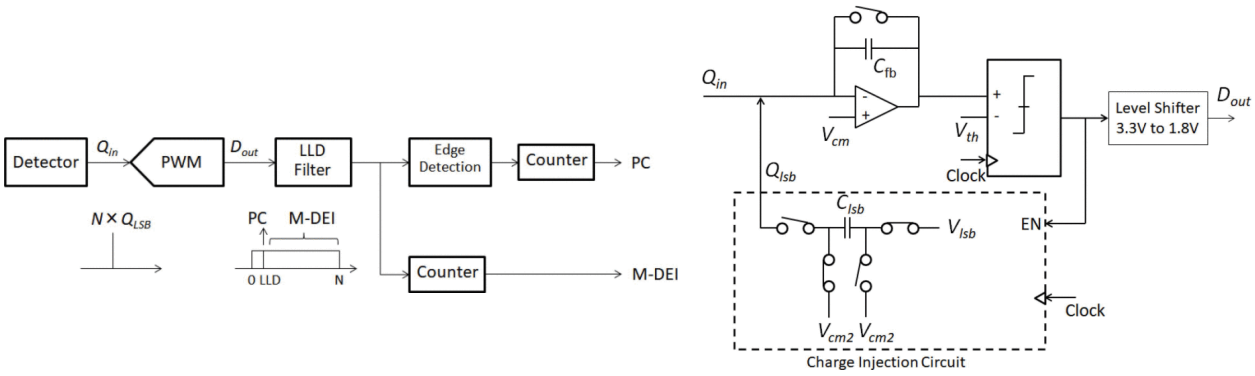
Figure 1.8: Block idea of *MultiX* readout channel. (Source: [16])

Pulse generator A slightly different approach is implemented in *Sphinx1* from *CEA-Leti* [60], [61], where a current-to-frequency converter, basing on the charge balancing technique [62] is used. The channel is presented in Fig. 1.9. The sensor is connected directly to a discriminator, and whenever the energy threshold is crossed, the input charge collected so far is compensated by a counter-charge injector. This process is repeated as long as the input voltage exceeds V_{TH}. Each activation of the injector increments an energy counter, and thus the number of counts is proportional to the total deposited energy. A similar method was applied in previous works, but there the goal was to extend the dynamic range and accuracy of integrating detectors [63], [64]. *Sphinx1* is designed in the 130 nm CMOS with the 200 µm × 200 µm pixel pitch. It is able to work in either the integrating or the spectroscopic SPC mode. In the latter, after the first discriminator pulse, a time window starts. It is the time for the charge injector and the energy counter to compensate the input charge and measure the energy. After this time elapses, the energy counter value is compared to a reference level, and one of two 15-bit photon counters is incremented. Finally, the energy counter is reset and the circuit is ready for another acquisition. The time window is set to 1 µs to be compatible with both the direct and indirect detectors. The LSB of the charge injector is 100 e^-. The paralyzable dead time between two consecutive photons in the SPC mode is 2.5 µs. It results in the maximum acceptable flux of 10 Mc/(s mm^2) which is insufficient for CT applications (compare with Table 1.1). The ENC for the 10 fF detector is 50 e^- and for 30 fF around 55 e^-. The static power consumption is 1.2 µW/pixel and during operation it amounts to 8.2 µW. There is no sensor leakage current compensation, so the current integrating on the capacitor can finally fire the discriminator, causing a false low-energy photon count.



(a) (b)

Figure 1.9: *Sphinx1*: (a) the pixel architecture and (b) the charge injector. (Source: [60])



(a) (b)

Figure 1.10: (a) Parallel energy integrating (M-DEI) and photon counting (PC) paths. (b) Implementation of the PWM block. (Source: [65])

The scientists from *Shizuoka University* in [65] modified the concept and merged the information from two parallel paths: the digital energy integration (based on the pulse generator) and the SPC. Compared to [61], an operational transconductance amplifier (OTA)-based CSA is added at the channel input, and a continuous-time discriminator is replaced with a dynamic one. The input charge is integrated at the CSA capacitor, causing a step voltage response, and after that, the counter-charge injection process starts to gradually discharge them. The energy resolution is regulated by the discriminator V_{TH}. Both the charge injector and the discriminator require a system clock. Its maximum allowable frequency is 20 MHz. Two separate ASICs, with the same analog and different digital parts, were fabricated in the 180 nm CMOS — one for the integrating mode and the other for the SPC verification. The final result of the proposed method is calculated by merging the separate collected data offline. The pixel size is 80 µm × 80 µm, the photon counter is 12-bit width and the energy integrator counter is 16-bit width. Some tests were performed with a CdTe detector in the SPC mode with the maximum energy of 200 keV. The energy resolution of 12.5 keV was obtained by setting 15 different values of the digital energy threshold (the minimum required number of discharging pulses). The analog part is supplied from 3.3 V and the digital one from 1.8 V. Although the energy value of each detected photon is measured in a pixel, it is summed in the energy integrator counter, and the resultant pixel value is the total accumulated energy. Spectrometric and imaging possibilities were reported separately, so this method does not allow for color CT.

1.2 Research problems, contributions and scientific novelty

After the thorough review of the current SPC detectors for color imaging, I list some research problems to be solved and present our attempts to address them. Thus, I describe our contribution to the *automation, electronics, electrical engineering and space technologies* discipline, especially in the field of front-end electronics for pixelated hybrid SPC radiation detectors. I also highlight the scientific novelty of the research.

Problem 1 Typically, the input stage of a discriminator is built with a differential amplifier, operating in an open loop with high but finite gain or positive feedback. However, the amplified difference is relatively

low and the overall discriminator response time is extended for signals just above the threshold. For monoenergetic imaging, the discrimination threshold is set between the noise and the expected energy of the detected photons. Due to the charge sharing (especially in small pixel systems), not all the charges generated by a photon are collected in a single pixel. Instead, they blur into neighboring pixels, yielding pulses corresponding to the proportionally lower energy. In order to detect them correctly, the threshold needs to be lowered toward noise. The ability to detect quickly the lowest possible charges above the discriminator threshold may to some extent allow the effective detection with a slightly greater distance from the noise level.

Contribution 1 A **low-power** continuous-time discriminator **with the significant reduction of an unwanted relationship between the reaction delay and the signal over threshold difference** was designed, using a negative impedance converter. This allows detection of all the CSA pulses exceeding the threshold with nearly the same speed, regardless of the peak height over the threshold voltage. This improves the detector count rate and the detecting efficiency of small energy portions (e.g. resulting from charge sharing) [1]. To our best knowledge, this is **the first application of a negative impedance converter in a discriminator**.

Problem 2 A comparator is the simplest A/D converter and is a common building block of more complex converters. As a basic component of a flash converter, it is replicated dozens of times in the converter, and is one of the most power-hungry components in the SAR. Changing the operating mode from continuous-time to discrete-time (dynamic) guarantees tremendous power savings. Reducing the transistors size the comparator is composed of speeds up its operation limiting the parasitic capacitance. It positively affects the area occupancy, yet it compromises the voltage offset. All the parameters relate to each other by nonlinear relationships, which must be optimized in the design process, depending on the specifications. The starting point of the design is also not so obvious.

Contribution 2 A comprehensive design study of a two-stage latched dynamic comparator in the 28 nm CMOS was prepared. It can help other designers to find a satisfactory starting point and the optimization direction, taking into account the required parameters (e.g. area occupancy, power consumption, speed, noise, offset, etc.). [3]

Problem 3 The common method of the dynamic comparator offset compensation is attaching the calibration capacitors. It slows down the discharge of the comparator node, thus influencing its speed. On the other hand, the time-domain compensation method presented by [66] in a flash ADC does not degrade the comparator speed. However, the control of the clock buffers delay is achieved with a matrix of capacitors, which take up a lot of area.

Contribution 3 A novel way to control the time-domain offset compensation method through the voltage regulation was proposed [4], **implemented and tested in the SAR ADC chip** [2].

Problem 4 The input stage of the detector's readout channel must be optimized in terms of gain, speed, noise, power consumption, area occupied, and DC voltage level. These requirements vary for different designs. The architecture of the cascoded inverter is very promising, providing high gain with the low power consumption and the low area occupancy. The challenge, however, is to establish the right size and polarity of the cascode. Model-based hand calculations are inaccurate (especially in new technologies) and each time analog parametric simulations are long.

Contribution 4 More reliable results can be provided by the g_m/I_D method. It is based on the data tables obtained from simple DC sweep simulations of several transistors in a given technology. In addition, such data in conjunction with numerical calculation tools can ensure the optimal selection of the desired parameters, taking into account the given requirements.

A tool for the cascoded-inverter-based CSA design optimization, providing all the required transistors widths and biasing voltages, corresponding to the requested specification was developed, **basing on the g_m/I_D method and the particle swarm optimization (PSO) algorithm**. It was fed with the Taiwan Semiconductor Manufacturing Company (TSMC) 28 nm CMOS transistors data and the result was **verified via analog simulations** [6]. The proper operation of the CSA designed with this tool was **evidenced in a 100-channel ASIC** [7].

Problem 5 Except for some designs without a clearly defined technology, all solutions described in State of the art are based on older, albeit mature, technology nodes, i.e. 40 nm and above. Thus, the same functional blocks occupy more area, limit the spatial resolution, and also operate more slowly (limiting the counting speed). However, switching to a newer technology is not sufficient — especially since newer technologies also manifest weaknesses in analog circuits, as described in Motivation. Thus, new methods of the pulse processing are in demand. The goal is to overcome the drawbacks of SPC detectors relative to integrating detectors that allow the fast signal processing. The SPC detectors should also be characterized by a small size and the low power consumption.

Contribution 5 The energy measurement capability in a pixel of a detector designed in the TSMC 28 nm technology by a multi-discriminator approach, and by an in-pixel SAR ADC was verified. Finally, **a new pulse generator-based circuit** was developed [5]. Its main advantage is the simultaneous peak amplitude conversion into digital word and capacitor discharge — **it combines the A/D converter and the reset circuit reducing the area occupancy**. Thanks to the small step, **the energy measurement resolution is high, and the CSA discharge is precise for the wide energy range** (compared to switch reset or click-clack). Thanks to the **asynchronous architecture**, it does not require a clock. Thus, (**the power consumption resulting from switching is reduced**. The need for challenging distribution of this signal throughout the chip is eliminated. Also, **the noisy digital signal is not present throughout the chip during the operation of sensitive analog circuits**. The developed circuit is also **much faster** (**several GHz**, compared to tens of MHz reported in State of the art), therefore **the CSA discharge is quick, positively affecting the achievable count rate**.

To the best of our knowledge, this is **the first solution based on an asynchronous pulse generator that discharges the CSA only after all the charge has been collected** (without adversely affecting the collection process) and **operating at GHz speeds**. It is also **one of the few such projects realized in the 28 nm technology**.

The circuit was **verified in a multi-channel ASIC**. The final solution is built with an optimized cascoded-inverter-based CSA [6], an asynchronous reset circuit [2], a dynamic comparator with time-domain offset compensation [2]–[4] and a continuous discriminator [1], combining all the work performed during the PhD studies.

Chapter 2

Application Specific Integrated Circuits for Ionizing Radiation Energy Measurement

In this project, three approaches were undertaken towards the low-power, low-area precise energy measurement in a modern sub-micrometer technology — the CMOS 28 nm. The two of them were implemented in fabricated and measured prototype ASICs. These three concepts, shown in Fig. 2.1, are as follows:

1. Energy measurement with multiple continues-time bandwidth-extended discriminators (Fig. 2.1a)
   Publications: [1]

2. Energy measurement with in-pixel synchronous differential SAR ADC (Fig. 2.1b)
   Publications: [2]–[4]

3. Energy measurement with an asynchronous pulse generator-based ADC (Fig. 2.1c)
   Publications: [5]–[7].

2.1 Energy measurement with multiple continues-time bandwidth-extended discriminators

At the first attempt to design a multiple energy recognizing channel, the simplest architecture was assumed. It was based on multiple discriminators continuously comparing the CSA output with individual thresholds. This project was mainly to evaluate the capabilities of the TSMC 28 nm technology, then newly available at the AGH University, and to estimate the performance of a readout channel design in it.

In an ideal discriminator, the input signal crossing a threshold causes in instantaneous reaction. In a practical circuit, the bandwidth and gain are finite, forming a relationship between the propagation delay and the input signal level [15], [67], [68]. The higher the difference between the input voltage and the threshold voltage, the quicker the discriminator response.

In [1] (Chapter 3.1), a symmetrical OTA is used as a discriminator core (see Fig. 2 in [1]). Its input NMOS transistors are loaded with the diode-connected PMOS transistors of a low small-signal resistance, i.e. $\frac{1}{g_m}$. The bandwidth is limited by the time constant of the second stage high-impedance output node. It is

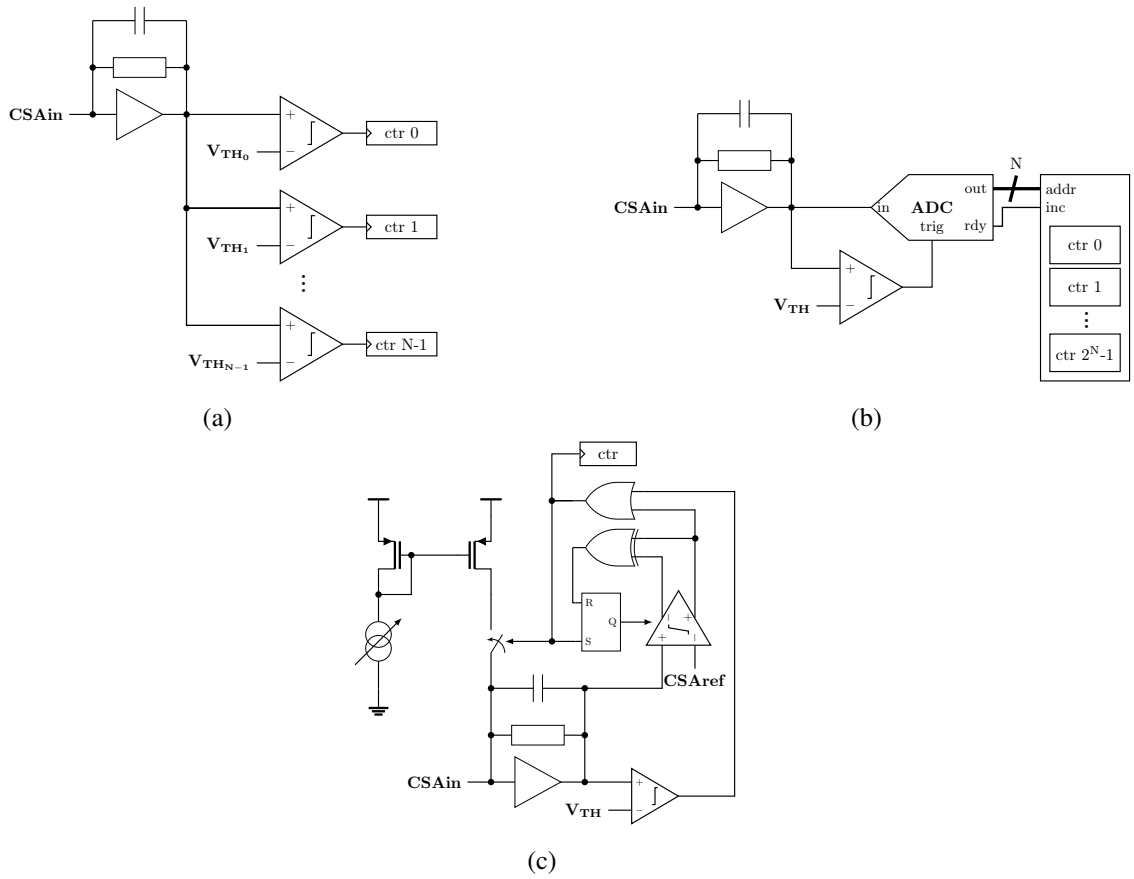


Figure 2.1: Simplified schematics of in-pixel energy measurement solutions for radiation detector front-end electronics: (a) multiple discriminators, (b) in-pixel ADC, (c) asynchronous pulse generator-based ADC.

a product of the transistors M6 and M8 output resistance r_O and their parasitic capacitances C_{DS} and C_{DB}. In general, the high r_O has a beneficial effect on the discriminator gain. Yet, in this case, the capacitances are an undesired effect of the MOS physical realization, affecting the circuit bandwidth.

A very common analog active circuit, mainly employed in oscillators and comparators, is a pair of cross-coupled MOSFETs, forming a negative resistance. Basing on it, a negative impedance converter (NIC), providing negative capacitance, can be designed as well [69], [70]. Such a circuit is implemented in the developed discriminator, compensating for the output node parasitic capacitance.

The final circuit (Fig. 9 in [1]), at a schematic level, consumes 1.0 µW when the output is *off* (the input signal remains below the threshold) and 3.8 µW when is *on*. The discriminator is capable of working with the CSA-like pulses of up to 1.25 GHz and should not occupy more than 15 μm^2 of silicon area. The propagation delay remains almost flat over the entire input signal voltage range and amounts to 0.5 ns, which is a significant improvement when compared to the circuit without a NIC (see Fig. 8 in [1]).

Although the presented circuit is fast and relatively small, each attempt to improve the resolution of the energy measurements by one level involves disadvantageous results: a linear increase of the static power dissipation and diminishing the available pixel area. For this reason, as described in Chapter 1.1.3, multi-discriminator-based channels which offer the resolution better than 4 levels are rather not common. Instead, the 2 level ones are quite popular.

While multi-discriminator-based high-resolution energy measurement systems are rather inefficient, a single fast continuous-time discriminator is the right choice for the CSA output monitoring. Such a discriminator provides a trigger signal for the better power- and area-optimized converters, whenever a pulse is detected.

2.2 Energy measurement with in-pixel synchronous differential SAR ADC

2.2.1 SAR ADC ASIC

So as to improve the energy resolution, 255 discrimination levels were selected. Realized only with the discriminator from [1], such a solution requires 255 discriminators, dissipating at least 255 µW of total static power at idle. Moreover, it occupies around 3.8 mm^2, while the common pixel size varies from 50 µm × 50 µm to 500 µm × 500 µm.

To achieve the intended goal, the pulse amplitude was measured at its peak, and converted by the ADC. The SAR architecture was frequently used in many applications in the last decade, mainly due to its excellent power efficiency [71]–[74], and for that reason it has also been chosen for this project.

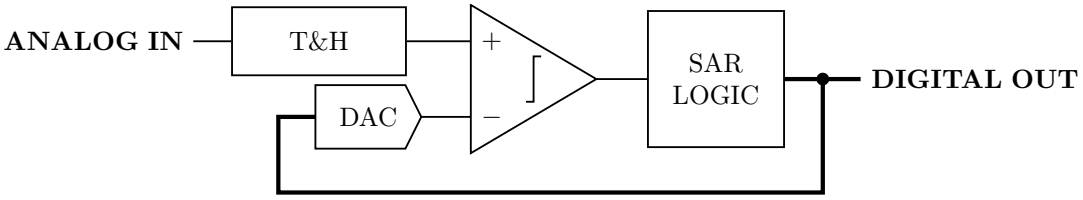


Figure 2.2: Simplified schematic of a single-ended SAR ADC.

Fig. 2.2 presents a basic SAR ADC which consists of: a track-and-hold (T&H) circuit, a DAC, a comparator and SAR logic. When the conversion starts, the T&H stops tracking the analog input and stores its last value unchanged until the end of conversion. At subsequent steps, the converter searches for the best digital representation of the analog input. At the first step, only the most significant bit (MSB) of the DAC is set. Basing on the comparison result, the SAR logic prepares the next DAC configuration. If the result is *low*, it means that the MSB is too high and the held analog value must be approximated by the lower digital word. Therefore, the MSB is cleared for the remaining conversion. However, if the result is *high*, it means that the analog input exceeds 50 % of the maximum DAC value and the MSB remains set until the end of conversion. In either case, the next bit is set and the whole process is repeated for all the DAC bits. Hence, the DAC resolution defines the SAR ADC resolution and also the number of steps in a single conversion. After the last step, involving the LSB, the digital result is ready.

In [2] (Chapter 3.2), the design and the measurement results of the 8-bit SAR ADC fabricated in the TSMC 28 nm CMOS are presented. The power consumption largely depends on the DAC architecture. So to reduce it, a switched-capacitor array was implemented. It is composed of custom metal-oxide-metal (MOM) capacitors of the unit capacitance 0.54 fF, switched by inverters. This approach simplifies the T&H design. It is reduced to the switches only, as the capacitive DAC stores the analog value by itself. Moreover, a differential architecture which suppresses the common-mode component was applied in order to make

the sensitive analog part less vulnerable to noisy digital signals. Since the comparison did not have to be performed continuously, but only in specified moments, to save power, a dynamic comparator was used. The SAR logic was synthesized using the *Verilog* hardware description language (HDL). The schematic of the ADC designed is presented in Fig. 2 in [2].

The ADC is synchronous and driven by the external 100 MHz clock signal. The maximum allowable sampling frequency is 10 MS/s. However, to ensure higher linearity, the tracking phase of the T&H was extended by one clock cycle, thus reducing the sampling frequency to 9.1 MS/s According to the measurements of 8 chips, the average effective number of bits (ENOB) for the input signals up to 100 kHz is slightly above 7 bits, and then it starts to degrade (see Fig. 9 (a) in [2]).

The average absolute values of integral nonlinearity (INL) and differential nonlinearity (DNL) are below 0.5 bits and 0.3 bits, respectively. The whole ADC consumes 45 µW of power and occupies the silicon area of 30 µm × 60 µm. The results are significantly better than it was previously estimated for the multi-discriminator-based method. Therefore, this ADC is applicable for the in-pixel energy measurement system.

2.2.2 Dynamic comparator

A decisive component of the SAR ADC is a comparator. It has to perform as many operations in a single conversion as many bits of resolution the converter has. Since the result is checked by the SAR logic at specified moments, there is no need for the comparator to be active all the time. A dynamic comparator is then the right choice for this application, since it only draws current during the comparison phase and dissipates no static power when idle. The architecture proposed by [75] was selected with additional improvements described in [3], regarding its well-balanced main parameters. The transistor level schematic is presented in Fig. 1 in [3].

In [3] (Chapter 3.3), a thorough study of the design procedure is presented. It is the detailed analysis of how the bias and each transistor dimensioning impact the final circuit parameters, such as: maximum preamplifier gain, input-referred noise, mismatch-induced voltage offset, propagation delay, probability of error due to metastability, node capacitances, energy per conversion, and approximated area occupation.

Basing on the SAR ADC requirements and the performed analyses, the comparator was designed. Its transistor sizing and main parameters presented in Table I and Table II in [3]. The final circuit occupies the 5 µm × 5 µm area, consumes 17.1 fJ for a single comparison with 250 ps of the propagation delay, and allows working with a 4 GHz clock signal.

2.2.3 Time-domain offset compensation

Imperfections of the semiconductor fabrication process result in a mismatch of the designed components. An example is an undesired difference between node capacitances of the symmetrical preamplifier structure, which causes the comparator voltage offset.

A common method to overcome this issue is attaching small calibrating capacitors to the node with smaller capacitance. This, however, degrades the comparison speed, slowing down the whole circuit. An interesting alternative is the time-domain offset calibration, which introduces a time lag before triggering

the faster node, instead of slowing down its slope [66]. The time shift is provided by two parallel digital buffers with the regulated propagation speed, controlling the preamplifier switches.

In [4] (Chapter 3.4), basing on the proposed solution, the time-domain offset calibration was implemented to the designed dynamic comparator. Additionally, the area-consuming capacitor array for the buffer speed control was replaced with the supply voltage-based control. In Fig. 3 in [4] there is the proposed control circuit with the waveforms it provides.

The voltage value which cancels the offset is defined as the one resulting in the longest reaction time of the comparator being driven with equal inputs (see Fig. 5 in [4]). The achieved calibration range is ±15 mV.

The voltage-controlled time-domain offset calibration circuit was applied to the dynamic comparator and placed in the SAR ADC.

2.3 Energy measurement with asynchronous pulse generator-based ADC

2.3.1 Pulse reset with A/D conversion

To guarantee the accurate energy measurement by the ADC connected to the CSA output, the voltage has to be stable for the entire conversion time. Thus, the high discharge constant of the CSA feedback must be ensured. However, this compromises the available count rate, limiting a possibility to work with a high flux beam. Still, when the conversion is complete, the stable CSA output is no longer necessary, so it can be pulled down to the baseline. There are several reported methods to do so, e.g. *switch reset* [56] or *click-clack* [31], still with imperfections while working with a wide energy range system.

In [5] (Chapter 3.5), these reset circuits are briefly described, indicating an issue of the precise return to the baseline in a wide range of the CSA amplitudes. As an alternative, an asynchronous loop was proposed, providing the fast and accurate discharge of the feedback capacitors by the small current pulses injection. The actual CSA output is compared to the desired DC voltage by the dynamic comparator, and the calibration is provided by the time-domain offset calibration circuit. The schematic of the circuit and the waveform illustrating its operation principle are presented in Fig. 3 and Fig. 4 in [5], respectively. The layout, excluding the calibration DAC, occupies only 12 µm × 14.5 µm (see Fig. 5 in [5]). The circuit was simulated with the energies up to 200 keV. Depending on the energy and the discharging current, the return-to-baseline time equaled from 440 ns at 200 keV with the lowest current down to 50 ns at 60 keV with the highest current.

Since the feedback capacitor is discharged with the current pulses of constant intensity, the number of discharging loop iterations is directly proportional to the initial voltage on the capacitor, and thus to the energy of a detected photon. Therefore, counting the iterations number in a digital counter, the energy-to-digital conversion is provided with no additional ADC circuit. Moreover, thanks to the approximately constant voltage on the discharging current source, the conversion exhibits high linearity (Fig. 8 in [5]).

In comparison with the solutions discussed in 1.1.3, which also use the pulse generator but based on an additional capacitor or charge-coupled device (CCD)-like approach, this design incorporates the CSA as an input stage. It is asynchronous, and thanks to the regulated trigger delay, it is activated only when the charge collection on the CSA capacitor is finished. All the above-mentioned features have the following implications:

- Thanks to the CSA use, the noise of proceeding stages is reduced by the CSA gain and the measurement is independent from the sensor capacitance.
- Thanks to the activation only after the charge collection is completed, it does not affect the collecting process.
- Thanks to the asynchronous architecture:
  - there is no power consumption from switching,
  - challenging distribution of the clock signal throughout the chip is unnecessary,
  - no noisy digital signal is present during the sensitive analog circuits operation,
  - the converter is fully automatic,
  - the frequency of the discharging loop is much higher (several GHz, compared to tens of MHz reported in State of the art),
  - discharging the CSA feedback is quicker, positively affecting the available count rate.
- Thanks to the small step, the energy measurement resolution is high, and the CSA discharge is precise throughout the entire wide energy range (compared to, switch reset or click-clack).

Additionally, thanks to the current DAC and the time-domain offset calibration in the comparator, the proposed method allows for the effective mitigation of the process, voltage and temperature (PVT) influence.

2.3.2 Automated design of cascoded-inverter-based CSA

The energy measurement accuracy depends not only on the converter itself, but, first of all, on the charge sensitive amplifier which is the very first functional block dealing with the charge delivered from a sensor. Thus, the CSA core parameters like gain, bandwidth, noise, and DC level are of high importance as they are responsible for reliable signal processing. Still, the power consumption and area occupation have to meet the pixel design requirements as well. These parameters often contrapose, leading to many trade-offs. In such a case, it is recommended to apply an optimization algorithm so as to find the best solution [76]–[78].

Calculating circuit parameters, especially of modern sub-micron technologies, basing on the transistor square-law model is inaccurate. More adequate estimation is provided by the g_m/I_D method which offers the single transistor model valid in all the operation regions. Moreover, the base calculations on actual transistor properties are extracted from simulations of an actual device [79].

The very common CSA core architecture is the folded cascode common source amplifier which requires two current sources for biasing [28], [30]. An inverter-based amplifier has the higher gain-bandwidth product (GBW) at the same bias current, taking advantage of the PMOS and NMOS transconductance simultaneously. However, it is very PVT sensitive, so an appropriate architecture must be used to minimize this effect. A double cascoded structure seems to be a promising choice.

In [6] (Chapter 3.6), a design process of the cascoded-inverter-based CSA core is described, implementing the g_m/I_D method and the PSO algorithm. The circuit to be optimized (Fig. 1 in [6]) was unambiguously

described with a set of equations (Eq. 1). The appropriate formulas for the parameters evaluation were provided as well (Eq. 2). The tool prepared in *Matlab*, was based on the simulation results of a few transistors from the TSMC 28 nm technology. This tool was able to find the optimal transistors widths and biases in less than 3 minutes. The results are presented in Table I in [6]. The circuit was then positively verified in a simulation program with integrated circuit emphasis (SPICE). In Table II in [6] there is a comparison of the required parameters, the predicted values and those obtained from the simulations. The CSA core achieves 500 V/V gain, the 3.7 MHz bandwidth and the 71 e^- ENC, consuming 2.2 µW of power from a 1.1 V supply.

Most importantly, in case of a new project, even in another technology, it is sufficient to provide the tool with new requirement values and simulation results in order to obtain the new CSA design in a few minutes.

2.3.3 REMIC

The final outcome of the conducted research is the prototype Radiation Energy Measuring Integrated Circuit (REMIC), comprising all the functional blocks presented so far, except the SAR ADC. The design and measurement results are presented in [7] (Chapter 3.7).

The REMIC is fabricated in the TSMC 28 nm CMOS. It has 100 pixels of 50 µm × 50 µm in size (Fig. 2 in [7]). A single channel (Fig. 3 in [7]) contains the optimized cascoded-inverter-based CSA, the continuous-time discriminator, the pulse generator-based converter, the Krummenacher feedback to compensate for sensor leakage current, and a counter. A switch reset and the click-clack are added to compare the proposed pulse generator-based method in terms of the CSA reset capability. The ADC includes the dynamic comparator with the time-domain offset compensation, this time realized with the capacitively loaded delay line.

There are two possible CSA gain configurations: 40 µV/e^- and 20 µV/e^-, allowing for the energy measurement up to 55 keV (12.4 ke^-) and 110 keV (24.8 ke^-), respectively, assuming the CdTe sensor. Depending on the reset method, the REMIC is able to work in a classical SPC mode (with the switch, the click-clack or the Krummenacher feedback alone) or in a spectroscopic mode (with the pulse generator-based ADC). In the first case, the 12-bit pixel counter counts the discriminator pulses, and in the other it counts the pulse generator loop iterations. The examples of the conversion results are shown in Fig. 9 in [7].

Fig. 11 in [7] presents the CSA pulses with different reset methods and different input energies. It evidences the stable and predictable behavior of the pulse generator-based method, in comparison to the switch and the click-clack, whose undershot values are energy-dependent. Moreover, in the proposed method, the undershot can be regulated by the internal comparator offset change.

The total measured static power consumption per pixel is only 6.2 µW. The dynamic power consumption depends on the input pulse frequency. It stays below 10 µW/pixel up to 50 kHz. At the maximum measured frequency, i.e. around 360 kHz, it amounts to 18 µW/pixel (Fig. 12 in [7]). The measurement was performed using an internal switched-capacitor calibrating circuit controlled by a square wave signal, resulting in bipolar input current pulses, thus degrading the maximum count rate. According to the waveforms presented in Fig. 11 in [7], the REMIC can work with the equally distributed input pulses of frequency 1 MHz, resulting in 0.4 Gc/(s mm^2). The preliminary noise estimation revealed the ENC of 70 e^-, basing on the assumption that 10 %–90 % of the threshold scan counts covered 4σ.

The proposed solution meets the CT detector requirements in terms of the spatial resolution and the allowable energy range (see Table 1.1). Even though the estimated count rate at high energies is lower than assumed, the ASIC with the attached sensor could work with even higher intensities. Now, the count rate is lowered due to two factors: the bipolar nature of the calibration method, and the additional CSA load. The latter results from an analog multiplexer and a buffer which drives the output pad.

The ability to perform the 12-bit energy measurement in such a short time with the exceptionally low power consumption promotes the REMIC for the CT applications. It also opens possibilities for further development.

Chapter 3

Publication Series — Full Texts

Table 3.1: My detailed individual contribution to each publication in the series.

Publication	Corresp. Author	Pct. Contrib.	Detailed Contribution
[1] Piotr Kaczmarczyk and Piotr Kmon, "Continuous-time discriminator design in CMOS 28 nm process," in *Proceedings of 26th International Conference "Mixed Design of Integrated Circuits and Systems" MIXDES*, Rzeszów, 2019, pp. 186–189. DOI: 10.23919/MIXDES.2019.8787153	Yes	60 %	• schematic level design of the discriminator • research and verification of possible improvement blocks • final design proposition • data analysis and processing • primary paper version preparation and further co-editing
[2] Piotr Kaczmarczyk and Piotr Kmon, "8 b 10 MS/s differential SAR ADC in 28 nm CMOS for precise energy measurement," *Journal of Instrumentation*, vol. 17, no. 03, p. C03027, 2022. DOI: 10.1088/1748-0221/17/03/C03027	Yes	80 %	• schematic and layout level design of the core of the SAR ADC ASIC • printed circuit board (PCB) design and assembling • ASICs wire bonding • measurement setup preparation, including software development (*LabVIEW*, *LabVIEW FPGA*) • measurements, data collection, analysis, and processing in Matlab • primary paper version preparation and further co-editing

[3] Piotr Kaczmarczyk and Piotr Kmon, "Dynamic comparator design in 28 nm CMOS," *International Journal of Microelectronics and Computer Science*, vol. 9, no. 4, pp. 149–154, 2018, [Online]. Available: https://ijmcs.dmcs.pl/vol.-9-no.-4, ISSN: 2080-8755	Yes	80 %	• schematic level design of the comparator • analysis of the key parameters dependency on particular transistors dimensioning and circuit biasing • final design proposition • data analysis and processing • primary paper version preparation and further co-editing
[4] Piotr Kaczmarczyk and Piotr Kmon, "Projekt dynamicznego komparatora z korekcją napięcia niezrównoważenia w dziedzinie czasu (design of a dynamic comparator with time-domain offset calibration)," *Przegląd Elektrotechniczny*, vol. 96, no. 12, pp. 121–124, 2020. DOI: 10.15199/48.2020.12.23	Yes	80 %	• schematic level design of the comparator • design verification throughout simulations • data analysis and processing • Primary paper version preparation and further co-editing
[5] Piotr Kaczmarczyk and Piotr Kmon, "Automated, adaptive, fast reset circuit for wide-energy range detector front-end," *Journal of Instrumentation*, vol. 18, no. 03, p. C03010, 2023, ISSN: 1748–0221. DOI: 10.1088/1748-0221/18/03/c03010	Yes	60 %	• circuit design at schematic and layout level • reset method implementation, improvement and verification throughout simulations • data processing • primary paper version preparation and further co-editing • corrections according to reviewers claims

[6] Piotr Kaczmarczyk, “Automatic design of a cascoded-inverter-based charge-sensitive amplifier using g_m/I_D technique and particle swarm optimization in 28 nm CMOS,” in *Proceedings of 30th International Conference "Mixed Design of Integrated Circuits and Systems" MIXDES*, Kraków, 2023	Yes	100 %	• transistor parameters extraction for g_m/I_D method • circuit and performance description with appropriate formulas • CSA specification preparation • optimization algorithm implementation in *Matlab* • design verification through SPICE simulation • paper preparation • corrections according to reviewers claims
[7] Piotr Kaczmarczyk and Piotr Kmon, “Fast asynchronous 12-bit in-pixel ADC for high spatial resolution multi-energy radiation detectors in CMOS 28 nm,” *IEEE Transactions on Circuits and Systems—Part II: Express Briefs*, 2023, sent for review	Yes	60 %	• ASIC core schematic and layout design • verification throughout simulations • PCB design and assembling • measurement setup development in *System Veriog* and *Python* (basing on a framework provided) • data collection, analysis and processing in *Matlab* • paper co-authoring

3.1 Continuous-Time Discriminator Design in CMOS 28 nm Process

[1] Piotr Kaczmarczyk and Piotr Kmon, “Continuous-time discriminator design in CMOS 28 nm process,” in *Proceedings of 26th International Conference "Mixed Design of Integrated Circuits and Systems" MIXDES*, Rzeszów, 2019, pp. 186–189. DOI: 10.23919/MIXDES.2019.8787153

3.2 8 b 10 MS/s differential SAR ADC in 28 nm CMOS for precise energy measurement

[2] Piotr Kaczmarczyk and Piotr Kmon, "8 b 10 MS/s differential SAR ADC in 28 nm CMOS for precise energy measurement," *Journal of Instrumentation*, vol. 17, no. 03, p. C03027, 2022. DOI: 10.1088/1748-0221/17/03/C03027

3.3 Dynamic Comparator Design in 28 nm CMOS

[3] Piotr Kaczmarczyk and Piotr Kmon, "Dynamic comparator design in 28 nm CMOS," *International Journal of Microelectronics and Computer Science*, vol. 9, no. 4, pp. 149–154, 2018, [Online]. Available: https://ijmcs.dmcs.pl/vol.-9-no.-4, ISSN: 2080-8755

3.4 Projekt dynamicznego komparatora z korekcją napięcia niezrównoważenia w dziedzinie czasu

(Design of a Dynamic Comparator with Time-Domain Offset Calibration)

[4] Piotr Kaczmarczyk and Piotr Kmon, "Projekt dynamicznego komparatora z korekcją napięcia niezrównoważenia w dziedzinie czasu (design of a dynamic comparator with time-domain offset calibration)," *Przegląd Elektrotechniczny*, vol. 96, no. 12, pp. 121–124, 2020. DOI: 10.15199/48.2020.12.23

3.5 Automated, adaptive, fast reset circuit for wide-energy range detector front-end

[5] Piotr Kaczmarczyk and Piotr Kmon, "Automated, adaptive, fast reset circuit for wide-energy range detector front-end," *Journal of Instrumentation*, vol. 18, no. 03, p. C03010, 2023, ISSN: 1748–0221. DOI: 10.1088/1748-0221/18/03/c03010

3.6 Automatic Design of a Cascoded-Inverter-Based Charge-Sensitive Amplifier Using g_m/I_D Technique and Particle Swarm Optimization in 28 nm CMOS

[6] Piotr Kaczmarczyk, “Automatic design of a cascoded-inverter-based charge-sensitive amplifier using g_m/I_D technique and particle swarm optimization in 28 nm CMOS,” in *Proceedings of 30th International Conference "Mixed Design of Integrated Circuits and Systems" MIXDES*, Kraków, 2023

3.7 Fast Asynchronous 12-bit In-Pixel ADC for High Spatial Resolution Multi-Energy Radiation Detectors in CMOS 28 nm

[7] Piotr Kaczmarczyk and Piotr Kmon, "Fast asynchronous 12-bit in-pixel ADC for high spatial resolution multi-energy radiation detectors in CMOS 28 nm," *IEEE Transactions on Circuits and Systems—Part II: Express Briefs*, 2023, sent for review

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[1] P. Kaczmarczyk and P. Kmon, "Continuous-time discriminator design in CMOS 28 nm process," in *Proceedings of 26th International Conference "Mixed Design of Integrated Circuits and Systems" MIXDES*, Rzeszów, 2019, pp. 186–189. DOI: 10.23919/MIXDES.2019.8787153.

[2] P. Kaczmarczyk and P. Kmon, "8 b 10 MS/s differential SAR ADC in 28 nm CMOS for precise energy measurement," *Journal of Instrumentation*, vol. 17, no. 03, p. C03027, 2022. DOI: 10.1088/1748-0221/17/03/C03027.

[3] P. Kaczmarczyk and P. Kmon, "Dynamic comparator design in 28 nm CMOS," *International Journal of Microelectronics and Computer Science*, vol. 9, no. 4, pp. 149–154, 2018, [Online]. Available: https://ijmcs.dmcs.pl/vol.-9-no.-4, ISSN: 2080-8755.

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[7] P. Kaczmarczyk and P. Kmon, "Fast asynchronous 12-bit in-pixel ADC for high spatial resolution multi-energy radiation detectors in CMOS 28 nm," *IEEE Transactions on Circuits and Systems—Part II: Express Briefs*, 2023, sent for review.

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