Journal of Applied Physics ARTICLE scitation.org/journal/jap

Multi-bit MRAM storage cells utilizing serially connected perpendicular magnetic tunnel junctions

Cite as: J. Appl. Phys. **125**, 223907 (2019); doi: 10.1063/1.5097748
Submitted: 28 March 2019 · Accepted: 24 May 2019 ·
Published Online: 14 June 2019

View Online Export Citation CrossMark

Piotr Rzeszut,[1,a)] Witold Skowroński,[1] Sławomir Ziętek,[1] Jerzy Wrona,[2] and Tomasz Stobiecki[1,3]

AFFILIATIONS

[1]Department of Electronics, AGH University of Science and Technology, Al. Mickiewicza 30, 30-059 Kraków, Poland
[2]Singulus Technologies, Kahl am Main 63796, Germany
[3]Faculty of Physics and Applied Computer Science, AGH University of Science and Technology, Al. Mickiewicza 30, 30-059 Kraków, Poland

[a)]**Electronic mail:** piotrva@agh.edu.pl

ABSTRACT

Serial connection of multiple memory cells using perpendicular magnetic tunnel junctions (pMTJs) is proposed as a way to increase magnetic random access memory (MRAM) storage density. A multibit storage element is designed using pMTJs fabricated on a single wafer stack, with serial connections realized using top-to-bottom vias. The tunneling magnetoresistance effect above 130%, current induced magnetization switching in zero external magnetic field, and stability diagram analysis of single, two-bit, and three-bit cells are presented together with thermal stability. The proposed design is easy to manufacture and can lead to an increased capacity of future MRAM devices.

Published under license by AIP Publishing. https://doi.org/10.1063/1.5097748

I. INTRODUCTION

Spin transfer torque magnetoresistive random access memories (STT-MRAMs) have numerous advantages over existing storage technologies, including theoretically unlimited endurance, high read and write speeds, and ionizing-cosmic-radiation resistance.[1,2] However, state-of-the-art memories have limited capacity due to the fact that the current density needed to switch a cell (typically made of a single magnetic tunnel junction) requires relatively large transistors.[3,4] Such an obstacle can be overcome using the architecture that incorporates a multibit cell driven by a single transistor.

To date, very few practical implementations of multibit MRAM cells have been presented.[5,6] This is mainly due to the fact that efforts were made to produce a single storage element capable of being stable in more than two states or to produce multiple storage elements on top of each other.[7–9] Both of these approaches are very challenging to manufacture.

In this work, an alternative approach is proposed—perpendicular magnetic tunnel junctions (pMTJs)[10–12] are connected electrically in series and a multistate behavior is observed that leads to a multibit storage capability. Theoretical explanation as well as experimental results (including the working three-bit cell) is presented. In addition, such an approach can be implemented to design and fabricate an artificial synapse for a neuromorphic computing scheme.[9,13–17]

II. PRINCIPLES OF OPERATION

The discussed pMTJs consist of a top free layer (FL), a MgO tunnel barrier, and a bottom reference layer (RL), which is magnetically pinned to the synthetic ferromagnet (SyF).[18] In the proposed serial connection of pMTJs in a storage cell, the top contact of the first element is connected to the bottom contact of the next element (head-to-tail), as shown in the inset of Fig. 1. This results in the charge current flowing through all the cells involved in the same direction. Connections can be made using metallization and vias or any other suitable techniques.

The behavior of the presented arrangement of storage elements can be predicted by analyzing characteristics of two pMTJs connected (Fig. 1). If both elements are in the parallel (P) state, the lowest resistance is observed (1). When a positive voltage is applied [which corresponds to the current flow that favors antiparallel (AP) state], the current increases, until it reaches a critical value, which

Published under license by AIP Publishing.

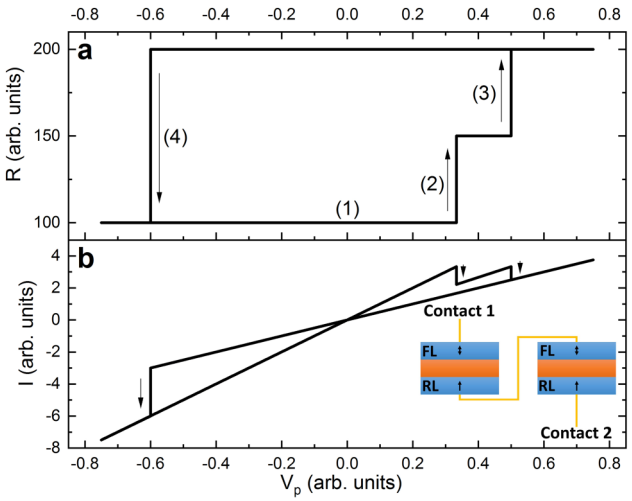

FIG. 1. Theoretically predicted (a) resistance and (b) current vs voltage applied to a storage cell consisting of two serially connected pMTJs. Inset: schematic of serial connection of two pMTJs.

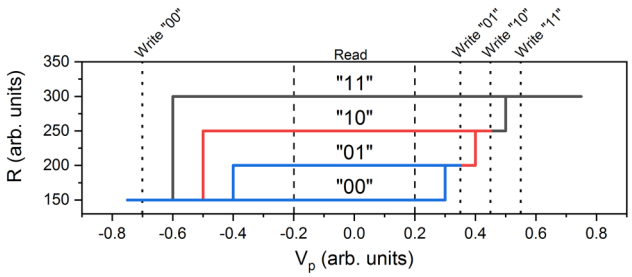

FIG. 2. Theoretically predicted resistance vs voltage applied to the proposed two-bit cell. Possible mapping between resistance and binary value as well as proposed voltages to write and read the cell is presented on the plot. Different colors represent the behavior of the cell after different writing voltages application.

results in the current induced magnetization switching (CIMS) (2). As one of the elements switches to the AP state, with constant voltage applied, the current decreases. This prevents the remaining element of the cell from switching, as the current drops below the critical value. By further increasing the voltage, the critical current is reached again, and the second pMTJ switches to the AP state (3).

By reversing the current polarization, the switching to the P state is achieved. In this case, as soon as the critical current is reached, one of the elements switches to the P state (4). With constant voltage applied, the current rises above the critical value, causing the other element to switch to the P state.

The above mechanism works also for more than two elements, and similar reasoning can be carried out. For the serial pMTJs connection utilizing the presented mechanism, $N+1$ stable resistance states would be observed for N elements connected, resulting in storage ability of $\log_2(N+1)$ bits. This is because there is no possibility to individually determine states of all incorporated storage elements; as ideally, they are characterized by the same resistance—only the number of elements in P and AP states may be determined, based on the two-point resistance measurement.

The storage cell capable of storing two bits of data would, therefore, consist of three serially connected storage elements. The predicted resistance vs voltage characteristics of such a storage cell are presented in Fig. 2. Voltages for writing different states, as well as reading the cell, can be defined based on the characteristics obtained for a single pMTJ. Note that in the proposed cell configuration, writing smaller bit value (smaller resistance) than the existing state requires clearing the state to "00" (the lowest resistance) and writing a new value.

A similar solution was suggested by Raymenants *et al.*;[6] however, with a different arrangement of subsequent elements, which are connected in opposite directions (head-to-head and tail-to-tail). Such a multilevel cell, though, needs application of variable external magnetic fields to have an ability to be written with any desired state, what is not the case for our design, where the read–write process is much simpler. On the other hand, our solution has by design a limited number of stable states to $N+1$.

A similar mechanism was also suggested by Zhang *et al.*,[13] with elements fabricated on top of each other; however, due to experimental difficulties, only two working elements connected in series were fabricated.

In our work, these drawbacks of other designs are eliminated, and the presented arrangement is ready to be manufactured using an unmodified fabrication process.

III. EXPERIMENT

Multilayer of the following structure: buffer/Co(0.5)–Pt(0.2) based SyF/W(0.25)/CoFeB(1)/MgO(0.89)/CoFeB(1.3)/W(0.3)/CoFeB(0.5)/MgO(0.75)/capping layers (thickness in nanometers) patterned into pillars of around 130 nm diameter were used as the pMTJ basic cell. The details of the deposition and fabrication processes are presented in Refs. 19 and 20. Elements were equipped with $100 \times 100\,\mu m^2$ Al(20)/Au(30) contact pads that enable both individual pMTJ characterization as well as measurement of the elements connected in series forming a multibit cell. The schematics of the multilayer stack, a fabricated pMTJ pillar, and a micrograph of a two-bit (three pMTJs in series) cell are presented in Fig. 3. In order to determine the ability of a single element to act as a memory device, two types of characterization were performed: a stability diagram[19] and thermal stability[21] measurements.

The stability diagram was determined as follows: pMTJ resistance (R) vs voltage pulse amplitude (V_p) measurements were repeated with different external magnetic field (H) applied. The voltage pulse length was set to 10 ms. Each point on the stability diagram corresponds to the transition from the P to AP state or the AP to P state, depending on the initial magnetization configuration. The thermal stability was determined from the R vs H measurement repeated around hundred times with a magnetic field changing in 1 s long magnetic field steps of 80 A/m.

Published under license by AIP Publishing.

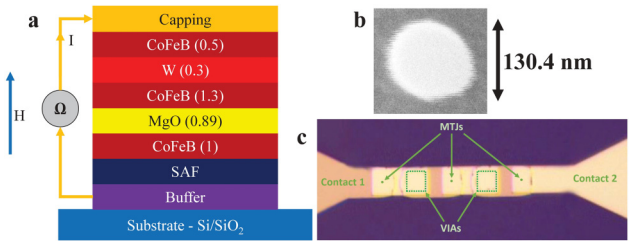

FIG. 3. (a) pMTJ layer structure, "SAF" denotes synthetic antiferromagnet, *H* denotes external magnetic field direction, *I* denotes current direction, Ω denotes the sourcemeter or the cell driving circuit. (b) Scanning electron microscope image of a single pMTJ. (c) Micrograph of three serially connected pMTJs.

IV. RESULTS AND DISCUSSION

A. Single pMTJ characterization

An example of the $R(V_p)$ loop and the stability diagram are presented in Fig. 4. The TMR ratio of 135% and the resistance area (RA) product of 21.6 $\Omega\,\mu m^2$ were measured. These values, however, are influenced by series resistance of vias and contacts, which could not be eliminated due to two-wire measurement; in fact, the TMR ratio of the element is higher.[20] In the absence of an external magnetic field, the P to AP transition occurs for the voltage of around 0.25 V (corresponding to the critical current density of 2.00 MA/cm^2), whereas the AP to P switching is measured for $V_p = -0.15$ V (corresponding to $J_{crit} = -0.54\,MA/cm^2$). Multiple $R(H)$ measurements, performed on the same pMTJ, allowed one to obtain the switching probability vs H using the analysis described

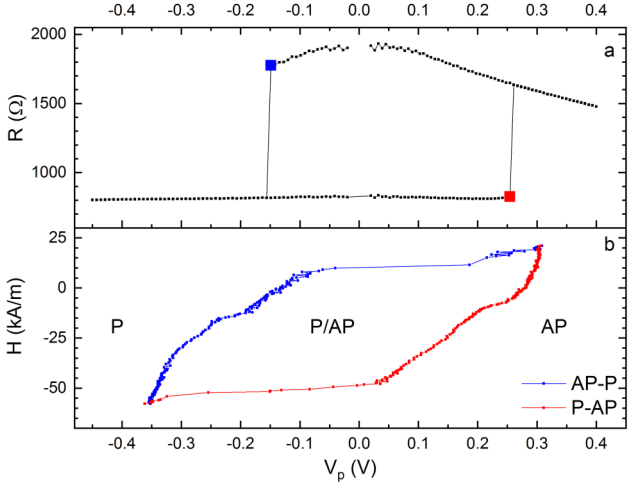

FIG. 4. (a) Representative *R-V* loop of a single pMTJ, with switching voltages from P to AP (red) and from AP to P (blue) marked using big squares, measured without external magnetic field. (b) A stability diagram with marked regions where P, AP, or both of the states are stable.

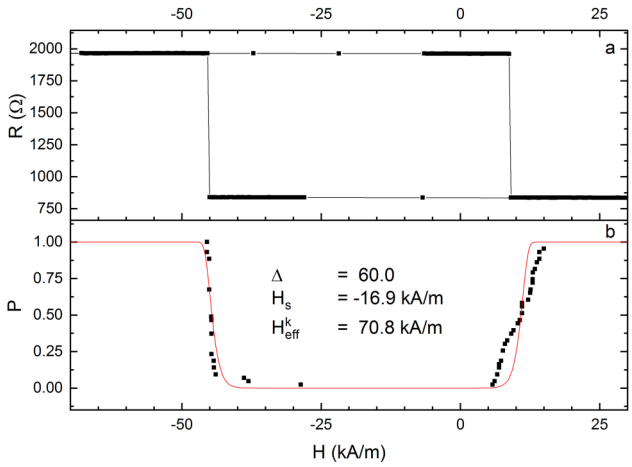

FIG. 5. (a) Representative *R-H* loop of a single pMTJ. (b) Calculated switching probability (black points) and theoretical fit based on Eq. (1).

in Ref. 21 with the following equation:

$$P(\tau) = 1 - \exp\left[-\frac{\tau}{\tau_0}\exp\left\{-\Delta\left(1 - \frac{|H - H_s|}{H_k^{eff}}\right)\right\}\right]. \quad (1)$$

In Eq. (1), τ denotes the magnetic field step duration (in this study, $\tau = 1$ s), τ_0 denotes the inverse of the attempt frequency (in this work it is assumed to be 1 ns), Δ denotes the thermal stability, H_s denotes shift field, and H_k^{eff} denotes the effective magnetic anisotropy field.

The best fit of Eq. (1) to the experimental switching probability resulted in $\Delta = 60$, which together with a capability of the pMTJ of being stable in both P and AP states in the absence of an external magnetic field proves that the cell is suitable to be used as a memory device (Fig. 5).

B. Two-bit storage cell

Next, we move on to the two-bit cell consisting of three pMTJs connected in series. $R(V_p)$ measurement of such a system is presented in Fig. 6(a)—initially, the two-bit cell is in the low resistance state. The application of the positive voltage of around 0.37 V (corresponding to a single pMTJ switching from P to AP state) results in the transition to higher resistance state, which is denoted as "01." Further increase of voltage to around 0.67 V causes a second pMTJ transition to a higher resistance state—thus "10" state is written. Finally, after the application of 0.80 V, all three pMTJs are in the AP state, which is denoted as the "11" state. A negative voltage of −1.15 V switches all pMTJs back to the P state. The behavior described in Sec. II was confirmed—four stable states can be defined and binary numbers can be assigned to them:

- All elements in the AP state—11.
- One element in P state and two in the AP state—10.
- Two elements in AP state and one in the P state—01.
- All elements in the P state—00.

Published under license by AIP Publishing.

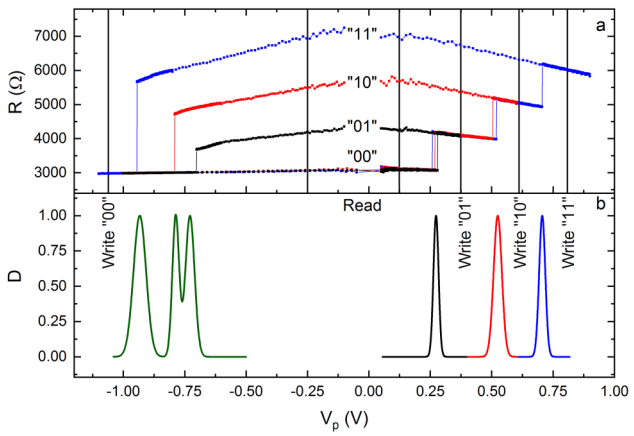

FIG. 6. (a) CIMS measurement of the two-bit memory cell. The proposed binary coding is also presented. (b) Switching voltages distribution, with regions for writing, and safe readout presented.

By repeating *R-V* measurement of the two-bit cell around hundred times and calculating switching voltage distributions, writing voltages of particular states, as well as a region safe for reading the storage cell, can be defined [Fig. 6(b)].

The principle of operation, involving the current decreasing below the critical current after one element switching into the AP state, was confirmed (Fig. 7). Due to the nonideal manufacturing process, critical currents of all incorporated elements are nonequal, but this has no adverse effect on the process (Fig. 7, inset).

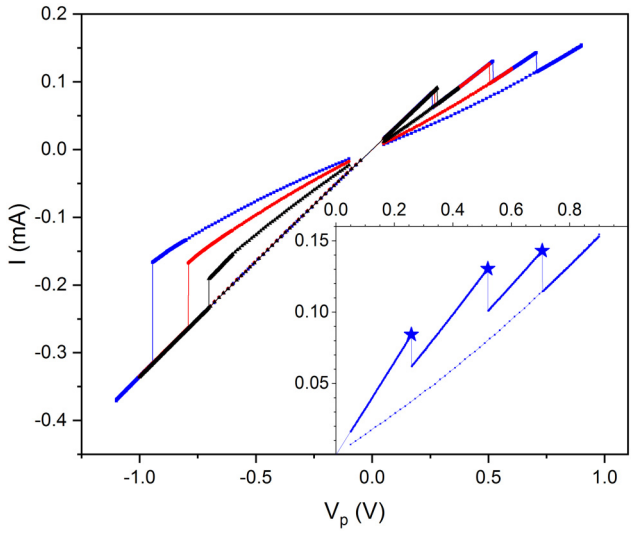

FIG. 7. Current changes during *R-V* measurement for the storage cell constructed of three storage elements. Inset: a close up of current in the CIMS measurement for writing the "11" cycle. Critical currents causing subsequent elements to switch to the AP state are marked with stars.

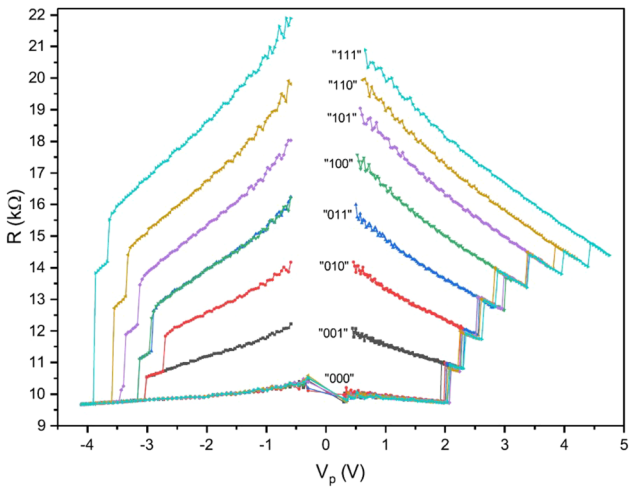

FIG. 8. *R-V* measurement of the three-bit cell consisting of seven pMTJs connected in series. The proposed binary coding is presented.

C. Three-bit storage cell

Finally, the proof-of-concept of the three-bit cell consisting of seven pMTJs connected in series is presented. As predicted, the cell exhibited eight stable states (Fig. 8). Due to the nonideal fabrication process, it was noted that regions for writing voltages of some of the states are very narrow because of variation of the switching voltage (related with the switching current distribution). The switching back to the "000" state was not ideal in the case, which may originate from a resistive behavior of the cell.[22] Nonetheless, the proposed architecture is valid for a multiple pMTJ that forms the multibit memory cell.

V. SUMMARY

In summary, we showed that a multibit memory cell can be successfully implemented using serially connected pMTJs. The state-of-the-art multilayer structure characterized by TMR of 135% and RA of $21.6\,\Omega\mu m^2$ was used to design two- and three-bit MRAM cells. The developed method of fabrication and driving multibit nonvolatile storage elements is a significant improvement in MRAM technology, as it allows one to store more data using the same area of the memory. This may be achieved by driving a multibit storage cell using a single transistor rated for the same current, as a single storage element (the critical current remains the same for any number of serially connected elements). Also, the fabrication process does not require significant changes compared to single storage element fabrication. The presented three-bit cell design requires around $26 \times 54\,\mu m^2$, most of which is occupied by vias and interconnections. The state-of-the-art CMOS technology enables fabrication of vias of around 100 nm, which could result in a cell size of around $1\,\mu m^2$. This method, however, exhibits some capacity limitations, mainly due to the variation of parameters of pMTJs, such as switching voltage, TMR ratio, or resistance of the individual element involved in a cell. It is noted that

Published under license by AIP Publishing.

contemporary STT-based MRAM operates at a nanosecond-long scale[23] and, therefore, the operation of the multibit cell at this time scale requires further study. In addition, the proposed solution may be utilized in the neuromorphic computing scheme as a multistate nonvolatile memory block.

ACKNOWLEDGMENTS

This work is supported by the Polish Ministry of Science and Higher Education Diamond Grant (No. 0048/DIA/2017/46) and the Polish National Centre for Research and Development (Grant No. LIDER/467/L-6/14/NCBR/2015).

T.S. acknowledges the SPINORBITRONICS project through the National Science Centre Poland under Grant No. 2016/23/B/ST3/01430.

The nanofabrication process was performed at the Academic Centre for Materials and Nanotechnology (ACMiN) of AGH University of Science and Technology.

REFERENCES

[1]A. D. Kent and D. C. Worledge, "A new spin on magnetic memories," Nat. Nanotechnol. **10**, 187 (2015).

[2]B. Dieny, R. Sousa, J. Herault, C. Papusoi, G. Prenat, U. Ebels, D. Houssameddine, B. Rodmacq, S. Auffret, L. Buda-Prejbeanu *et al.*, "Spin-transfer effect and its use in spintronic components," Int. J. Nanotechnol. **7**, 591–614 (2010).

[3]T. Kawahara, R. Takemura, K. Miura, J. Hayakawa, S. Ikeda, Y. Lee, R. Sasaki, Y. Goto, K. Ito, T. Meguro *et al.*, "2Mb spin-transfer torque RAM (SPRAM) with bit-by-bit bidirectional current write and parallelizing-direction current read," in *2007 IEEE International Solid-State Circuits Conference, ISSCC 2007, Digest of Technical Papers* (IEEE, 2007), pp. 480–617.

[4]S.-W. Chung, T. Kishi, J. Park, M. Yoshikawa, K. Park, T. Nagase, K. Sunouchi, H. Kanaya, G. Kim, K. Noma *et al.*, "4Gbit density STT-MRAM using perpendicular MTJ realized with compact cell structure," in *2016 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2016), pp. 27.1.1–27.1.4.

[5]W.-C. Jeong, B.-I. Lee, and S.-K. Joo, "Three level, six state multilevel magnetoresistive RAM (MRAM)," J. Appl. Phys. **85**, 4782–4784 (1999).

[6]E. Raymenants, A. Vaysset, D. Wan, M. Manfrini, O. Zografos, O. Bultynck, J. Doevenspeck, M. Heyns, I. P. Radu, and T. Devolder, "Chain of magnetic tunnel junctions as a spintronic memristor," J. Appl. Phys. **124**, 152116 (2018).

[7]K. Ju, and O. Allegranza, "Multibit cells schemes for toggle MRAM applications," IEEE Trans. Magn. **42**, 2730–2732 (2006).

[8]T. Ishigaki, T. Kawahara, R. Takemura, K. Ono, K. Ito, H. Matsuoka, and H. Ohno, "A multi-level-cell spin-transfer torque memory with series-stacked magnetotunnel junctions," in *2010 Symposium on VLSI Technology* (IEEE, 2010), pp. 47–48.

[9]S. Lequeux, J. Sampaio, V. Cros, K. Yakushiji, A. Fukushima, R. Matsumoto, H. Kubota, S. Yuasa, and J. Grollier, "A magnetic synapse: Multilevel spin-torque memristor with perpendicular anisotropy," Sci. Rep. **6**, 31510 (2016).

[10]T. Kishi, H. Yoda, T. Kai, T. Nagase, E. Kitagawa, M. Yoshikawa, K. Nishiyama, T. Daibou, M. Nagamine, M. Amano *et al.*, "Lower-current and fast switching of a perpendicular TMR for high speed and high density spin-transfer-torque MRAM," in *2008 IEEE International Electron Devices Meeting* (IEEE, 2008), pp. 1–4.

[11]S. Ikeda, K. Miura, H. Yamamoto, K. Mizunuma, H. Gan, M. Endo, S. Kanai, J. Hayakawa, F. Matsukura, and H. Ohno, "A perpendicular-anisotropy CoFeB–MgO magnetic tunnel junction," Nat. Mater. **9**, 721 (2010).

[12]H. Kubota, S. Ishibashi, T. Saruya, T. Nozaki, A. Fukushima, K. Yakushiji, K. Ando, Y. Suzuki, and S. Yuasa, "Enhancement of perpendicular magnetic anisotropy in FeB free layers using a thin MgO cap layer," J. Appl. Phys. **111**, 07C723 (2012).

[13]D. Zhang, L. Zeng, K. Cao, M. Wang, S. Peng, Y. Zhang, Y. Zhang, J.-O. Klein, Y. Wang, and W. Zhao, "All spin artificial neural networks based on compound spintronic synapse and neuron," IEEE Trans. Biomed. Circuits Syst. **10**, 828–836 (2016).

[14]J. Torrejon, M. Riou, F. A. Araujo, S. Tsunegi, G. Khalsa, D. Querlioz, P. Bortolotti, V. Cros, K. Yakushiji, A. Fukushima *et al.*, "Neuromorphic computing with nanoscale spintronic oscillators," Nature **547**, 428 (2017).

[15]C. Sung, H. Hwang, and I. K. Yoo, "Perspective: A review on memristive hardware for neuromorphic computation," J. Appl. Phys. **124**, 151903 (2018).

[16]O. Sulymenko, O. Prokopenko, I. Lisenkov, J. Åkerman, V. Tyberkevych, A. N. Slavin, and R. Khymyn, "Ultra-fast logic devices using artificial "neurons" based on antiferromagnetic pulse generators," J. Appl. Phys. **124**, 152115 (2018).

[17]S. Fukami and H. Ohno, "Perspective: Spintronic synapse for artificial neural network," J. Appl. Phys. **124**, 151904 (2018).

[18]D. Worledge, G. Hu, D. W. Abraham, J. Sun, P. Trouilloud, J. Nowak, S. Brown, M. Gaidis, E. O'Sullivan, and R. Robertazzi, "Spin torque switching of perpendicular Ta/CoFeB/MgO-based magnetic tunnel junctions," Appl. Phys. Lett. **98**, 022501 (2011).

[19]W. Skowroński, M. Czapkiewicz, S. Ziętek, J. Chęciński, M. Frankowski, P. Rzeszut, and J. Wrona, "Understanding stability diagram of perpendicular magnetic tunnel junctions," Sci. Rep. **7**, 10172 (2017).

[20]W. Skowroński, S. Łazarski, P. Rzeszut, S. Ziętek, J. Chęciński, and J. Wrona, "Influence of a composite free layer structure on thermal stability of perpendicular magnetic tunnel junction," J. Appl. Phys. **124**, 063903 (2018).

[21]H. Sato, M. Yamanouchi, K. Miura, S. Ikeda, R. Koizumi, F. Matsukura, and H. Ohno, "CoFeB thickness dependence of thermal stability factor in CoFeB/MgO perpendicular magnetic tunnel junctions," IEEE Magn. Lett. **3**, 3000204 (2012).

[22]Y. Zhang, W. Cai, W. Kang, J. Yang, E. Deng, Y.-G. Zhang, W. Zhao, and D. Ravelosona, "Demonstration of multi-state memory device combining resistive and magnetic switching behaviors," IEEE Electron Device Lett. **39**, 684–687 (2018).

[23]T. Andre, S. M. Alam, D. Gogl, J. Barkatullah, J. Qi, H. Lin, X. Zhang, W. Meadows, F. Neumeyer, G. Viot *et al.*, "ST-MRAM fundamentals, challenges, and outlook," in *2017 IEEE International Memory Workshop (IMW)* (IEEE, 2017), pp. 1–4.

Published under license by AIP Publishing.