AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

FIELD OF SCIENCE: ENGINEERING AND TECHNOLOGY

SCIENTIFIC DISCIPLINE: AUTOMATION, ELECTRONIC AND ELECTRICAL ENGINEERING

DOCTORAL THESIS

Switched capacitor resonant converter for control of voltage sharing on series-connected capacitors

Author: mgr inż. Jakub Hachlowski

First supervisor: prof. dr hab. inż. Robert Stala
Assisting supervisor: dr inż. Andrzej Mondzik

Completed in: AGH University of Science and Technology; The Faculty of Electrical Engineering, Automatics, Computer Science and Biomedical Engineering; Department of Power Electronics and Energy Control Systems

Krakow, 2022

AKADEMIA GÓRNICZO-HUTNICZA IM. STANISŁAWA STASZICA W KRAKOWIE

DZIEDZINA: NAUK INŻYNIERYJNO-TECHNICZNYCH

DYSCYPLINA: AUTOMATYKA, ELEKTRONIKA I ELEKTROTECHNIKA

ROZPRAWA DOKTORSKA

Przekształtnik rezonansowy z przełączanym kondensatorem do kontroli napięć w gałęzi szeregowo połączonych kondensatorów

Autor: mgr inż. Jakub Hachlowski

Promotor rozprawy: prof. dr hab. inż. Robert Stala
Promotor pomocniczy: dr inż. Andrzej Mondzik

Praca wykonana: Akademia Górniczo-Hutnicza im. Stanisława Staszica w Krakowie; Wydział Elektrotechniki, Automatyki, Informatyki i Inżynierii Biomedycznej; Katedra Energoelektroniki i Automatyki Systemów Przetwarzania Energii

Kraków, 2022

Abstract

Nowadays, the price of the electrical energy that is produced from fossil fuels is constantly increasing. Moreover, the natural environment is also affected as greenhouse gasses are polluting our surroundings. For many years, there has been a significant growth of interest in alternative energy sources such as sun, wind, and geothermal heat. Together with the technological progress of semiconductor devices, this has caused the rapid development of various power electronics systems for energy conversion. The multilevel neutral-point-clamped inverters are one of these research topics. This topology provides an efficient DC-AC energy conversion and enables passive circuit components such as output filters to be minimized. However, it has a number of disadvantages one of which is the DC-link capacitors becoming imbalanced, which negatively affects the quality of the converted output energy.

This dissertation provides a review of the research that has been published on the matter of voltage equalization using banks of series-connected capacitors and battery cells. Additionally, a novel topology is proposed in the thesis that is of a resonant switched capacitor type. The principle of the operation of the switched capacitor active balancing circuit (SCABC) is also presented. The work presents the mathematical expressions for the dependencies of a circuit. The possible operation modes of the converter are presented, together with an approach for its design in terms of the required components, sizing, and ratings. The sources of a circuit`s power losses are elaborated, and its efficiency is described using equations. Moreover, the basis of the converter control is described as well.

In order to prove the proposed converter concept, a simulation model in MATLAB®/Simulink® was developed. Moreover, the approach to designing the experimental setup is described and the setup that was built is presented. The results that were recorded reveal the circuit`s imperfections, and therefore, the author proposes improvements of the topology. The further research that is presented focuses on the ability of SCABC to control the voltages of the capacitive voltage divider, which forms the DC-link for the seven-level NPC inverter. Two cases of the connection of the DC power supply were investigated. In the first case, a complete DC-link was supplied and the operation of the balancer was controlled by closed-loop control system. Simulations of various scenarios were performed

and the results are presented. In the second case, only the middle capacitor of the DC-link was supplied, and therefore, the balancer not only maintained the voltage balance, but also boosted the supply voltage threefold. This case was studied *via* simulations of the circuit, as well as *via* laboratory experiments. Details of the development of the laboratory setup are presented as well. The results that were recorded for both cases are given. Moreover, the efficiency of a circuit was also investigated.

The final goal of this dissertation was to investigate the capability of SCABC to compensate the ripple second harmonic power, which propagates to the DC part of the subsystem. The focus of the research that was undertaken was on developing dedicated control algorithms for two possible configurations of a power conversion system: an SCABC with a seven-level NPC inverter and an SCABC with a five-level NPC inverter.

Streszczenie

W obecnych czasach cena energii elektrycznej wytwarzanej z paliw kopalnych stale rośnie. Co więcej, zwiększone na nią zapotrzebowanie wpływa niekorzystnie na środowisko naturalne, powodując emisję gazów cieplarnianych i dalsze jej skutki. Od wielu lat obserwuje się znaczny wzrost zainteresowania alternatywnymi źródłami energii, takimi jak energia promieniowania słonecznego, wiatr i ciepło geotermalne. Wraz z postępem technologicznym w dziedzinie komponentów półprzewodnikowych, spowodowało to szybki rozwój różnych topologii przekształtników energoelektronicznych. Jednym z aktualnych tematów badawczych są wielopoziomowe falowniki z poziomowaniem diodowym. Topologia ta zapewnia efektywną konwersję energii generowanej przy napięciu i prądzie stałym (DC) na energię AC i pozwala na minimalizację elementów obwodów pasywnych, takich jak filtr wyjściowy. Układ ten ma jednak szereg wad, a jedną z nich jest niezrównoważenie napięcia kondensatorów po stronie stałoprądowej. Nierównowaga ta wpływa negatywnie na jakość przetwarzanej energii wyjściowej i może doprowadzić do uszkodzenia układu ze względu na zwiększenie napięcia na wyłączonych elementach półprzewodnikowych powyżej wartości znamionowych.

Niniejsza praca przedstawia przegląd badań opublikowanych na temat wyrównywania napięcia w gałęzi szeregowo połączonych kondensatorów i ogniw bateryjnych. Autor proponuje nową topologię jaką jest rezonansowy przekształtnik z przełączanym kondensatorem, nazywany w pracy Switched Capacitor Active Balancing Circuit (SCABC). W pracy zamieszczono koncepcję działania tego układu w różnych jego wariantach oraz zaprezentowano badania analityczne. Przedstawiono możliwe tryby pracy przekształtnika oraz podejście do jego projektowania w zakresie doboru parametrów jego komponentów. Omówiono także źródła strat mocy w obwodzie oraz opisano sprawność za pomocą równań. Ponadto opisano podstawy sterowania przekształtnikiem.

Aby dowieść poprawności pracy proponowanej koncepcji przekształtnika, opracowano model symulacyjny w programie MATLAB®/Simulink®. Ponadto, opisano podejście do projektowania układu eksperymentalnego i przedstawiono zbudowany układ. Uzyskane wyniki ujawniły niedoskonałości układu, w związku z czym autor proponuje ulepszenie topologii. Dalsze prezentowane badania

koncentrują się na zdolności SCABC do kontroli wartości napięć pojemnościowego dzielnika napięcia, tworzącego wejście napięć stałych dla siedmiopoziomowego falownika NPC. Przeprowadzono badania dwóch przypadków podłączenia źródła energii DC. W pierwszym z nich zasilane jest cała szyna DC, a przekształtnik pracuje sterowany przez zamknięty układ sterowania. Przeprowadzono symulacje różnych scenariuszy pracy i przedstawiono wyniki. W drugim przypadku zasilany jest tylko środkowy kondensator obwodu pośredniego, więc SCABC nie tylko utrzymuje równowagę napięciową, ale także trzykrotnie zwiększa napięcie zasilania. Badania tego przypadku są przeprowadzane za pomocą symulacji obwodu oraz eksperymentów laboratoryjnych. Szczegóły dotyczące budowy zestawu laboratoryjnego są przedstawione czytelnikowi pracy. Podane są tu wyniki zarejestrowane dla obu wymienionych przypadków. Ponadto badana była sprawność energetyczna obwodu.

Jednym z celów pracy było zbadanie zdolności SCABC do kompensacji tętnień drugiej harmonicznej napięcia wyjściowego falownika, które propagują się do części stałoprądowej podsystemu. Podjęte badania koncentrują się na opracowaniu dedykowanych algorytmów sterowania dla dwóch możliwych konfiguracji przekształtnika: SCABC z siedmiopoziomowym falownikiem NPC oraz SCABC z pięciopoziomowym falownikiem NPC mostkowym, który wykorzystuje gałęzie trójpoziomowe.

Acknowledgements

I would like to thank all of the individuals who have contributed to my work. This dissertation would not have been possible without you.

Firstly, I would like to thank my supervisor, prof. dr hab. inż. Robert Stala, for his advice and guidance. His support throughout the last five years cannot be overestimated. Special thanks go to my assisting supervisor, dr inż. Andrzej Mondzik, for his support and the tips for preparing the experimental setups.

I would also like to express my appreciation to the R&D staff of SMA Magnetics Sp. z o.o. for their friendship and encouragement, and to the company itself for allowing me to complete the measurements in their power electronics laboratory.

Finally, my sincere gratitude goes to my family for helping me through these five busy years. I would like to especially thank my wife, Aneta, and my daughters, Tola and Sara, for their patience and the comfort they have given to me in the final phase of preparing this work.

Thank you!

Kuba

List of publications

During the research that was conducted for this dissertation, the selected findings and results have been published and are in common use. They are, however, the outcome of the Author`s work with no third person involved. Cross-references are provided where applicable.

[P.1] Hachlowski Jakub, Stala Robert. “A Novel Converter for Voltage Balance in Series-Connected Capacitors and Batteries”; Power Electronics and Drives 2018;3 (38):65–74

[P.2] Hachlowski, Jakub and Robert Stala. “DC-link Voltage Balancing Converter with Resonant Switched-Capacitor Circuit for Four-Level and Six-Level NPC Inverter.” 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe) (2019): P.1-P.10.

[P.3] Stala, R.; Hachlowski, J.; Penczek, A. NPC Seven-Level Single-Phase Inverter with DC-Link Voltage Balancing, Input Voltage Boosting, and AC Power Decoupling. Energies 2022, 15(10), 3729;

[P.4] Patent applications at The Patent Office of the Republic of Poland:

1. P.435563 - Circuit for controlling voltages on series-connected capacitors or batteries
2. P.435562 - Circuit for increasing the input voltage of a four-level NPC inverter powered from a single DC voltage source
3. P.435564 - Circuit for reducing the variable component in the input DC voltage of a three-level NPC inverter powered from a single energy source
4. P.435565 - Circuit for converting the energy of two independent DC voltage sources by a four-level NPC inverter

Nomenclature

AC	Alternating current
DC	Direct current
NPC	Neutral-point clamped
SCABC	Switched capacitor active balancing circuit
PV	Photovoltaic
MPPT	Maximum power point tracker
PD-PWM	Phase disposition pulse-width modulation
THD	Total harmonic distortion
SCVD	Switched capacitor voltage doubler
R_{DS_on}	Transistor`s on-state resistance
GaN	Gallium Nitride
C_{oss}	Transistor`s output capacitance
SC	Switched capacitor converter
SoC	System on a chip
G	Voltage gain
E_{on}, E_{off}	Energy of transistors single switching process: turn-on, turn-off
f_{SW}	Switching frequency of a converter
f_{RES}	Resonant frequency
ZCS	Zero-current switching
ZVS	Zero-voltage switching
ResSC	Resonant, switched capacitor converter
C_x	Capacitor x
L	Inductance
ω	Angular frequency
u_{CS}, $u_{CC,}$ u_{CD}	Voltage across capacitor: switched, charged, discharged
u_{Cmax}, u_{Cmin}	Maximum and minimum capacitor voltage
u_{IN}, u_{OUT}	Input and output voltage
T_{Sx}	Time interval of switching stage x
I_{Sxm}	Amplitude of current in switching stage x

r	Characteristic impedance of the series resonant circuit
i_{sx}	Resonant branch current during switching stage x
T	Full switching cycle of the converter
t_{SI}	Switched capacitor charging time
ts_{II}	Switched capacitor discharging time
td	Dead-time
ΔP_{ST}, ΔP_{SD}, ΔP_C, ΔP_{LW}, ΔP_{LC},	Power losses: transistor conduction losses, reverse diodes losses, switched capacitor losses, resonant choke winding losses, resonant choke core losses
R_{ESR}	Equivalent series resistance of capacitor
R_W	Resistance of inductor`s winding
η	Efficiency
k, α, β	Steinmetz coefficients
Seven-level inverter	A single-phase inverter composed of two legs with four voltage levels
Five-level inverter	A single-phase inverter composed of two legs with three voltage levels

TABLE OF CONTENTS

1. Introduction

This chapter presents the motivation and an overview of the research topics discussed in this dissertation. The main body of the work presents the design, simulation modelling, control, and implementation of a Switched Capacitor Active Balancing Converter (SCABC). The following sections discuss the sources of voltage imbalances in banks of series-connected capacitors, especially in multilevel inverters. The importance of eliminating these problems is discussed. The chapter also presents the current technological approach for eliminating voltage imbalances as well as the development and implementation of high-efficiency resonant switched capacitor converters.

1.1. Overview

In recent years, the demand for electric energy has been constantly increasing at an average of ca. 2% per year. However, due to COVID-19 pandemic, this trend decreased in 2020 [1.1]. The past decades have also been a period of a constant increase in the average global temperature [1.2]-[1.3].

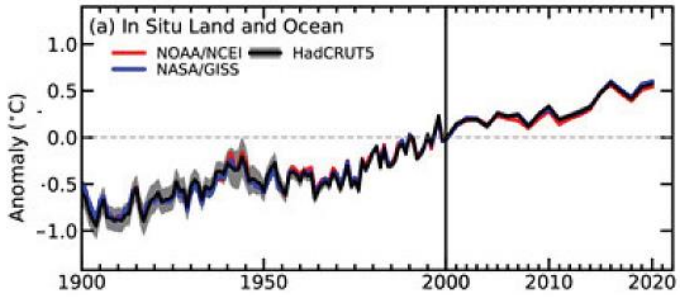


Figure 1.1: Observed globally averaged combined land and ocean surface temperature anomaly 1850-2020 [1.3].

The scientific community has found evidence that this is caused by human activity that is associated with using fossil fuels, which emit greenhouse gasses such as carbon dioxide. The extensive use of resources could lead to shortages as the estimated oil reserves globally is approximately 1490 billion barrels of which a significant percentage are located in areas with volatile political and social environments [1.4]

Hence, in recent years there has been a concerted effort to stop wasting these resources and to manage them more efficiently. New strategies and technologies are being developed in the area of clean and renewable energy. In 2020, it was

estimated that 29% [1.5] of global energy consumption was provided by renewable energy sources. This is the highest recorded value to date. The majority of these are provided by modern renewable energy sources such as PV cells and wind turbines. According to [1.6], there are already 28 countries in which the primary energy supply is provided in more than 50% by renewable energy sources. These facts translate into an increased demand for power conversion devices. Most of today's appliances would not operate without the appropriate power conversion, which is determined by the characteristics of the receiver, the efficient use of the power source, and the storage and transfer of electrical energy. The power conversion stage is a necessity for the majority of modern home appliances as well as for industrial applications. Power electronics are widely used in small, portable devices with power levels of a fraction of watt, as well as in large-scale industrial machinery reaching power of mega and giga watts.

Special attention should be paid to the field of power generation using the energy from the sun, the so-called photovoltaic (PV) systems. In 2021, it was estimated that the energy that was delivered by PV systems increased by 22% year-to-year, which translates into 140[GW] of peak power in PV generators. It was assessed that the total PV peak power equalled 950[GW] for the year 2021 and this is expected double by the end of 2025 [1.7].

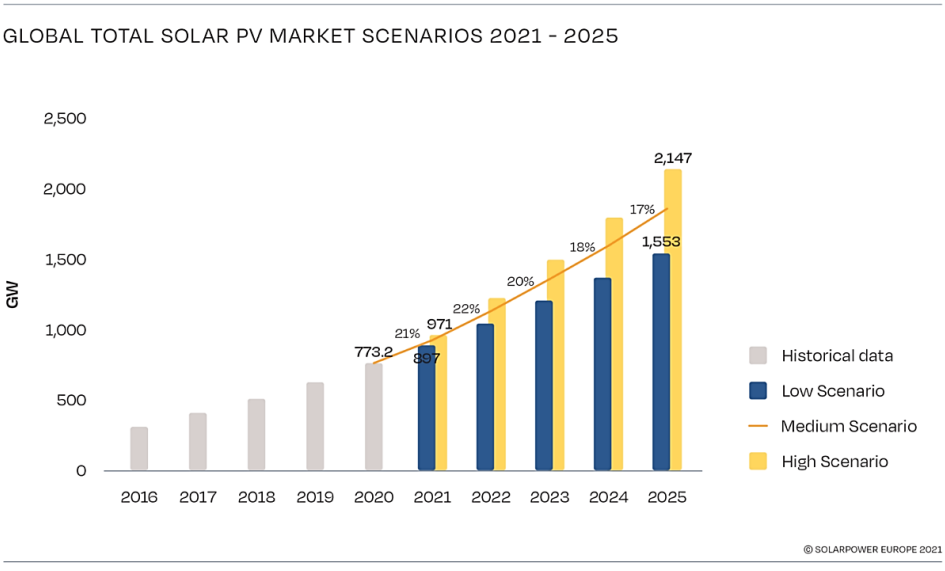


Figure 1.2: Market projections put the global solar sector comfortably within the Terawatt scale by 2022, and under optimal conditions, it could reach 2[TW] by 2025 [1.7].

In the past two years (2020-2022), the number of small residential PV systems has been decreasing in favour of industrial and utility-scale high power systems, which have reached about 2[GW] of installed power [1.9].

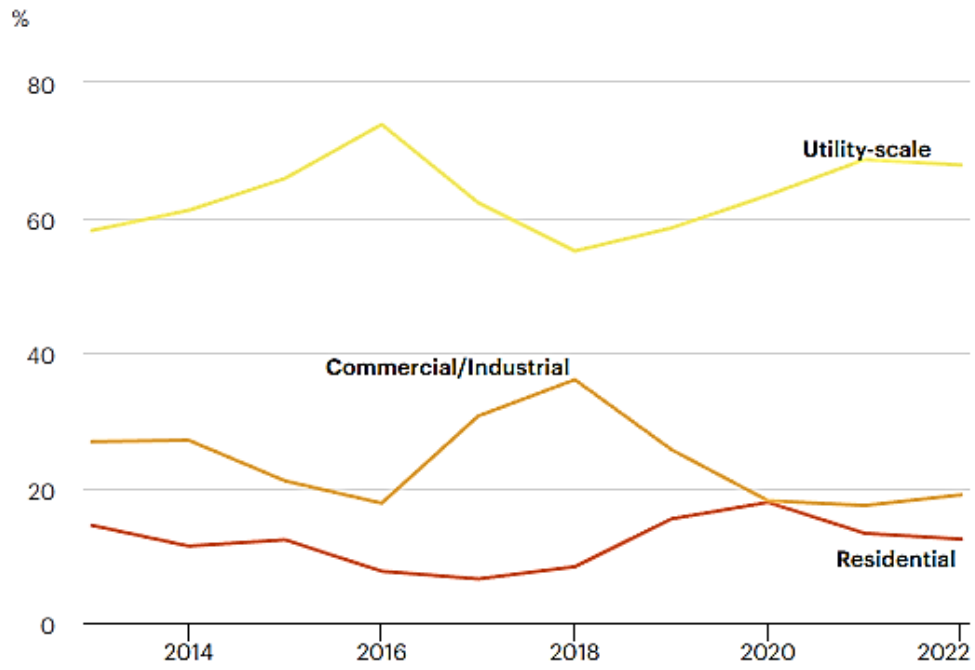


Figure 1.3: Share of solar PV net capacity that was added by the application segment from 2013-2022 [1.8].

To convert such a high amount of power, multilevel inverters are often used [1.10]-[1.11]. The Neutral-Point-Clamped type has especially increased in popularity [1.12]. The topology, however, is also suitable for low-power, single-phase PV systems [1.13]-[1.17]. With the appropriate control or additional circuit components, it can even eliminate the DC-DC conversion stage, thus providing MPPT functionality [1.18]-[1.19], integrate with battery energy storage [1.20] and attenuate common-mode leakage current [1.21]. A generalized three-level NPC inverter scheme is presented in Figure 1.4. It is supplied by a capacitive voltage divider with voltages that are equal to half of the DC link voltage on each capacitor. This topology permits semiconductor switches with half of the operation voltage to be used compared to a regular two-level inverter with the same output voltage. This is quite advantageous when the inverter is being connected with a medium-voltage grid [1.22]-[1.23] and when a high degree of efficiency and compact inverter's size are desired for maintaining a high power density [1.24]. Increasing the number of inverter levels is possible and even five-level NPC inverters have been widely studied [1.25]-[1.30]. With the increasing number of levels *n*, the voltage across

a single inverter transistor drops even lower: U_{dc}/n, and the output power quality rises, which permits the volume of the output filter stage to be decreased. However, the circuit becomes more complicated due to the number of semiconductor components as well as the necessary control algorithm for its correct operation. The research indicates that balancing the DC-link voltage is one of the main problems of this topology. For a single-phase NPC inverter with more than three levels, it is a circuit`s nature to cause a DC-link imbalance when it is being controlled using PD-PWM method. An imbalanced DC-link is the cause for incorrect operation of an inverter. The output waveforms that are generated get distorted, which causes an increased THD that resulted in a lower power quality. Moreover, the maximum allowable voltage on specific transistors could be exceeded thus causing the failure of a component. The effects of an imbalance of the DC-link capacitors in multilevel NPC inverters are assumed to be adverse.

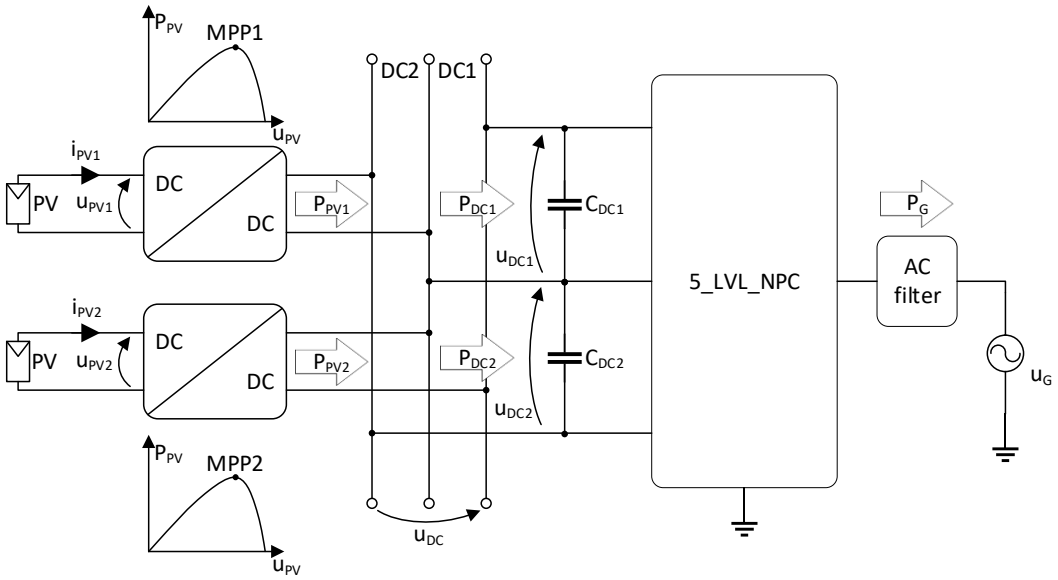


Figure 1.4: General block diagram of a multistring PV system with a split dual DC bus that is supplied by distributed generators, and is operating under different maximal power point values (MPP).

1.2. Dissertation objectives and structure

The objective of this dissertation was to conduct research on the Switched Capacitor Active Balancing Converter (SCABC): the principle of its operation, the applicable control algorithms, and applicability as a subpart of a modular power conversion system. The mathematical equations for the circuit description are presented. The topology was verified for its ability to balance the voltage on three

series-connected capacitors. A control system was developed, and an experimental setup was built to prove the concept.

The improved SCABC was connected to a seven-level NPC inverter and was able to balance the DC-link voltages efficiently. This protected the NPC inverter against an imbalanced state. The simulation results are also presented. Furthermore, the concept went beyond the active balancing. The analysed converter permitted some useful functions that are associated with energy conversion to be identified. The SCABC in an adequate configuration and with the adapted control algorithm was verified to perform the following operations:

1. Stepping up the input voltage in front of an NPC inverter that was composed of four-level legs. This eliminates the requirement for using a DC-DC boost converter in a conversion system.
2. DC-link voltage balancing in a circuit that was composed of three series-connected capacitors.
3. Decoupling a DC source power in a DC-AC system with a four-level NPC inverter. The case was verified *via* simulations. An improved control method for mitigating the double grid frequency component in a DC energy source was developed. The simulation and experimental results are presented.

The objectives of the dissertation were as follows:

1. To review and analyse the topologies that have been developed for controlling the voltage of series-connected capacitors and energy cells.
2. To develop and analyse an SCABC: its operating principle, operation modes, and the basis of the control.
3. To develop simulation models and investigate them in selected operation modes.
4. To develop the control algorithms as well as to select circuit components for an SCABC experimental device.
5. To design and develop an experimental setup for selected configurations of an SCABC with an NPC inverter.
6. To conduct the experimental research using the setup that was developed.

The dissertation is composed of seven chapters. Chapter 1 gives a brief overview of the motivation and objectives of the research that was undertaken.

The various areas in which the power converters of interest are used are discussed. A review of the research on voltage balancing techniques for series-connected energy storage elements is also presented. Additionally, the trending technology of the Gallium Nitride semiconductors is introduced.

Chapter 2 introduces switched capacitor converters. The basic topologies are presented together with their properties. The advantages of embedding resonant components, and thus the operation mode to a circuit, are described. Finally, the topology of a switched capacitor voltage doubler (SCVD) is presented as a simple example of a resonant technique that is introduced into power electronic converters.

Chapter 3 focuses on the concept of an SCABC. The principle of its operation is discussed and is supported with circuit representative equations and waveforms. The possible operation modes and the basis of control are presented as well. The sources of power losses in the circuit are also described in this chapter.

In chapter 4, development of the SCABC simulation model is presented. The simulation details are given, and the results for the various operation modes that prove the converter concept are presented. The approach for designing the experimental setup is described and the test results that were recorded are given. The pros and cons of the topology are discussed. An improved converter topology is then introduced.

Chapter 5 presents the research on the balancer that was connected to a seven-level single-phase NPC inverter. Two configurations with different the DC power source connections were investigated. For each of them, a specific control algorithm was developed, and the results of the simulation study are presented. What is more, for the case with the DC voltage boosting, the details of the development of the experimental setup are described and the results of the laboratory tests are presented.

Chapter 6 introduces the problem of ripple second harmonic power propagating into the DC power supply of a DC-AC conversion system. An SCABC with a dedicated control algorithm can perform the AC power component decoupling. Two configurations are presented: one with a seven- and one with a five-level NPC inverter. For the first, the simulation and experimental results are presented. For the second, the results of the simulation study are given.

Chapter 7 presents the conclusions of the research and details possible future work in this area of research.

1.3. The problem of voltage sharing in series-connected capacitors and batteries.

The input stage of a multilevel NPC inverter is a capacitive voltage divider. Thus, the DC-link is formed by series-connected capacitors in a number equal to *n*-1, where *n* is the number of inverter voltage levels in a single branch, which makes the problem of voltage sharing in series-connected capacitors important for multilevel inverters. In practical applications, the state of a DC-link imbalance can have a dynamic nature – either periodic or temporary – or be permanently triggered. This is dictated by the amount of energy that is being delivered to as well as what is being drawn from each of the capacitors at a given time. In other words, the stored energy balance between series-connected capacitors describes the kind and depth of the voltage imbalance. The main causes for a voltage imbalance in a voltage divider that supplies an NPC inverter are:

1. Its control method and the associated PWM pattern as well as the limited precision of digital technology: quantisation errors, the accuracy of analogue-to-digital converters, measurement errors, and the propagation times for different digital signals.
2. There can also be deviations in the properties of the components of the same type that are used in an inverter. These can be caused by a tolerance for parameters such as turn-on resistance, R_{DS_on} or the turn-on and turn-off times of the semiconductors, a change in a component's parameters due to ageing effects, e.g., dielectric layer degradation in capacitors
3. An unequal power delivery to each of the capacitors when it is supplied from alternative sources operating in different instantaneous power points or multiphase, interleaved DC-DC converters using coupled inductors that are operating in different conduction modes.
4. The dynamic states that are caused by a change in the energy flow, e.g., in the changeover in an electric drive from the driving to breaking mode; the three-phase grid imbalance when the inverter is connected with these components.

There are various methods that are recognised for voltage equalisation. One of them is based on the natural ability [1.25], [1.30]-[1.37] of an NPC inverter to balance the DC-link voltages by introducing an adequate switching pattern and the

so-called Passive Balance Booster circuit, which is an RLC type, and is connected to the AC output and the neutral point of the DC-link. As the research has shown, this is an effective method that has a number of advantages such as not requiring voltage measurements, the balancing process independence on the load, and their occurrence also in the idle mode. However, even though no special control is needed over the process, in order to enhance the performance of such a solution, a dedicated PWM pattern should be introduced to provide the best voltage equalising results. Additionally, the auxiliary components are bulky and can introduce supplementary power losses.

Another method for DC-link voltage balancing, which has been studied extensively for NPC inverters, is the use of a special control [1.38]-[1.43]. The general approach is to control the neutral point (NP) voltage by varying the direction of the current flowing into the NP. This can be achieved by either using space-vector or carrier-based modulation, where the correct selection of the redundant vector space settles the NP voltage to its midpoint. Because this solution is software based, it is often seen as being favourable. However, it has limitations at low power factor loads and high modulation depths [1.44]-[1.47] or sacrifices the output power`s harmonics performance when those limitations are overcome [1.48].

To achieve the voltage balance for an NPC`s input capacitive divider, an external balancing circuit can be introduced. Much research has been conducted that has resulted various solutions and topologies. In [1.49] and [1.50] four-level, two-quadrant DC-DC converters are presented. Both are able to operate in buck or boost mode, thereby ensuring a correct power supply for a four-level NPC inverter and also balancing its input capacitors by exchanging their energy. The research that is presented in [1.51] also proposes a DC-DC boost converter connected with a four-level NPC inverter. That approach, however, is different. The introduced circuit operates as an input stage and boosts the input voltage, thus feeding specific capacitors of the DC-link. Because there are multiple switching states, supplying two or three capacitors at the same time is also possible. In [1.52], a DC-DC converter for active voltage balancing on a four-level DC-link is discussed. It was built as two three-level chopper circuits and according to the work, its application was limited to the DC-DC conversion stage in between two NPC inverters working in a back-to-back configuration. The balancing circuit presented in [1.53] was designed to cooperate with a five-level NPC inverter that was built as two

unidirectional and complementary choppers, which were connected *via* a coupled inductor, and operated as a bidirectional half-bridge converter. The balancing ability was limited to maintaining the DC-link`s midpoint voltage level, not that of each of the capacitors.

Flying-capacitor topology has also been proposed for voltage balancing. Research in [1.54] and [1.55] presents similar chopper-based solutions. With the flying capacitor introduced, the voltage rating of the semiconductors that were used was lower, which minimised the converter`s volume and power losses. Balancing was achieved successfully in the dynamic ride-through states of the inverter.

Another group of balancing converters is formed by switched capacitor topologies. The study conducted in [1.56] presents a balancer for a five-level capacitive divider. The solution, however, is easily scalable for a different number of levels. Despite the proposed optimisation of the circuit, it required a substantial number of semiconductor switches – eighteen for the proposed solution – and its inrush current was limited by the resistance. This led to high power losses and poor efficiency. A similar solution was proposed in [1.57] with the added ability of the converter to boost the voltage being supplied by the DC source. The work presented in [1.58] also focused on the switched capacitor topology. The investigated converter enabled the capacitors` voltages on the four-level DC-link to be balanced while simultaneously boosting the input voltage. This could be advantageous when the power is supplied directly from PV arrays. However, current charging the capacitors is not limited by any means, which could lead to its significant amplitude in a deep imbalance state or during the pre-charging of a DC-link. Several papers have documented the use of the resonant switched capacitor technique to increase efficiency and eliminate inrush currents. Such a balancer connected to a five-level NPC inverter [1.59] consisted of two resonant branches. The balancing was only possible between two upper or lower capacitors. The authors of [1.60] proposed a single resonant cell converter that was able to balance the voltage of three series-connected capacitors. The number of semiconductor switches was relatively high (ten). The circuit, however, had self-balancing characteristics and could operate using two simple control methods. A balancer for four series-connected supercapacitors was investigated in [1.61]. It used a resonant tank that was formed by a switched capacitor, inductor, and transformer. During the equalising process, energy flowed through the voltage multiplier and was distributed to specific

supercapacitors, which kept their voltages equal. In [1.62], the same research team adapted this topology to equalise the voltages on series-connected battery cells. The area of voltage balancing in battery systems has plenty of research. Switched-capacitor equalising circuits for these systems were presented in [1.63]-[1.66].

1.4. GaN transistors

In many cases, the active voltage balancers for series-connected capacitors that have been proposed in the literature require a significant number of semiconductor switches. This fact leads to the conclusion that the overall performance of a circuit will be highly dependent on the performance of the transistors themselves. The wide bandgap semiconductors like Gallium Nitride (GaN) outperform the silicone ones in many applications. Their higher breakdown field enables components with a thinner drift layer to be manufactured. Thus, the GaN components have a low R_{DS_on} resistance. Because a high electron mobility will further improve this parameter, GaN transistors are preferred in high voltage applications (<600V) and because of their low parasitic capacitance, they have a very good high frequency switching behaviour with low C_{oss} losses [1.67]-[1.68]. As can be derived from equation (3.17), the dead-time that must be introduced in the control signals that are necessary for the turn-over of the transistors affects the current amplitude and thus the efficiency of a converter. Taking this fact into account, fast switching GaN semiconductors are preferable for the topology that is presented in this dissertation.

2. The switched capacitor converter

The DC-DC power electronics converters of a switched capacitor (SC) type are topologies that have been known in the field for many years. Moreover, they are still gaining popularity as the energy density in the modern foil- and ceramic-type capacitors is higher than in inductive elements, maintaining low power losses [2.1]. This type has a number of advantages such as:

1. High voltage gain.
2. Simplicity of topology: the converter consists only of the number of semiconductor switches, which is dependent on the topology, and capacitors.
3. Simple control.
4. Low volume as a result of the inductiveless design and the possibility to function as a highly integrated SoC device [2.2-2.5].

On the other hand, SC power converters have large current stresses and switching turn-on losses due to their hard switching operation, which can be a source of electromagnetic interference [2.6]-[2.8].

2.1. Basics of SC converter topologies

In the literature, a substantial number of power-electronics SC converter topologies have been introduced in recent years. The majority of converter circuits are based on the basic concepts such as Dickson, Fibonacci, or series-parallel that originated from microelectronics [2.2]-[2.5]. The topologies are so-called charge pump converter types, where electric charge packets are transferred from the power supply to the load with the certain voltage gain through a chain of capacitors.

No matter the topology, SC converters are characterised by the number of cells that they require. Each cell is composed of a capacitor and semiconductor switches. Depending on the single cell topology, it can be an addition, doubler, in-phase, or inverse phase type. Basic SC cells are presented in Fig. 2.1. When connected together, the cells comprise a complete converter with a voltage gain that corresponds to the number of individual cells. The energy transfer during the SC operation state can either be from:

1. The power supply to the capacitor (converter`s output).
2. Between the capacitors (cell to cell).
3. Capacitor to the load (converter`s output).

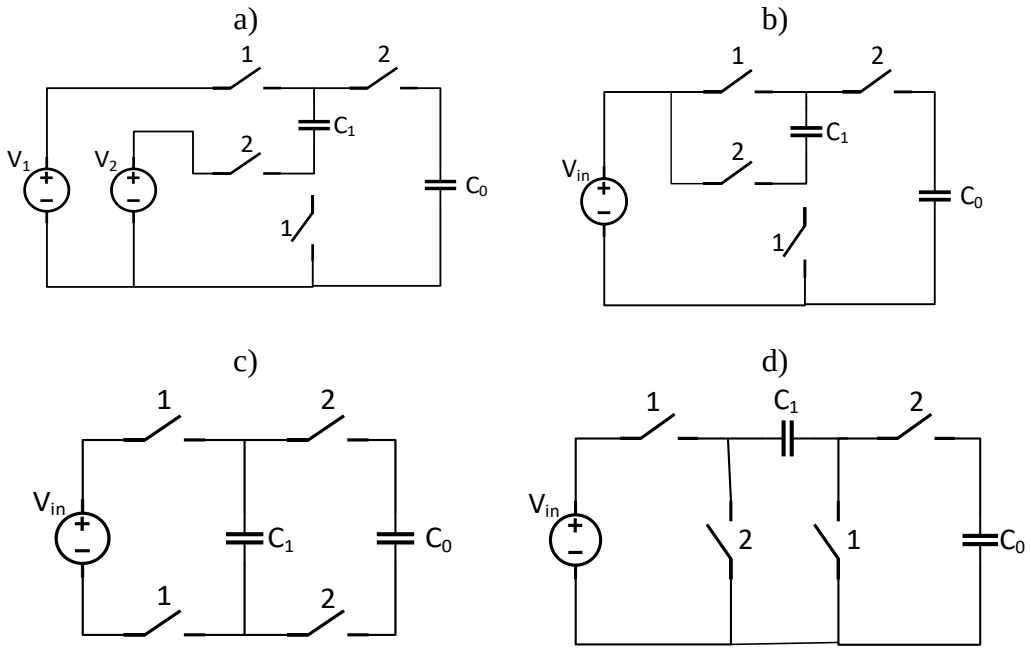


Figure 2.1: Basic cells for SC converters; (a) voltage addition, (b) voltage doubler, (c) in-phase, (d) inverse phase.

The topologies of Dickson and Fibonacci converters are presented in Figure 2.2, and an idealised voltage gain for *N*-cell converter is given by equations (2.1) and (2.2), respectively:

$$G = N + 1 \tag{2.1}$$

$$G = F_{N+1}; \quad \text{where } F_0 = F_1 = 1; \;\; F_i = F_{1-1} + F_{1-2}\, for\, i > 1 \tag{2.2}$$

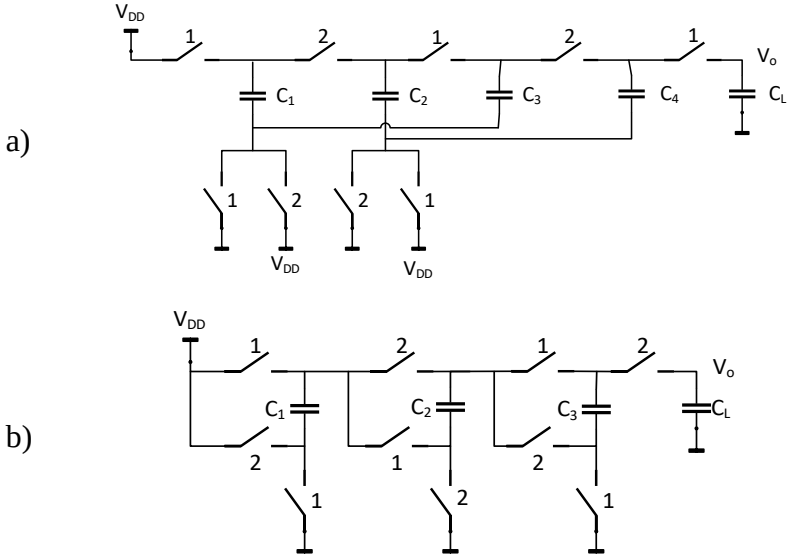


Figure 2.2: a) Schematic diagram of a four-stage Dickson CP (*N* = 4, *G* = 5) b) Schematic diagram of a three-stage Fibonacci CP (*N* = 3, *G* = 5).

The Fibonacci converter is a series of connected voltage addition cells. On the other hand, the Dickson topology is a ladder-type converter, however, for a voltage gain of a 1:2 ratio, it simplifies to a voltage doubler cell. In order to function, both circuits need to be fed by two, non-overlapping signals that control the transistor switches. In the Dickson`s converter (Figure 2.2a), each switched capacitor is charged up to the voltage of the preceding cell and is then boosted with the supply voltage $V_{DD}$. Then, the summed-up voltage is fed to the next stage. With the circuit`s parasites neglected, the voltage increment of each stage is V_{DD}, thus the resulting gain of a complete circuit depends on the number of cells as shown in equation (2.1).

For comparison, a Fibonacci SC can achieve the same gain with fewer cells. This type of converter is a two-phase SC and has the highest gain for a given number of capacitors [2.10]. The voltage on each SC capacitor is the summation of the voltage on the previous two cells, hence, the voltage on each SC follows a Fibonacci series. The j-th Fibonacci number, for $j \geq 1$ can be expressed as:

$$Fj = \frac{\varphi^{\,j} - (1 - \varphi)^j}{\sqrt{5}} = \{1,1,2,3,5,8,13, \dots\} \tag{2.3}$$

where φ is the golden ratio

$$\varphi = \frac{1 + \sqrt{5}}{2} = 1{,}6180 \dots \tag{2.4}$$

Because the presented topologies are circuits of an RC (resistance-capacitance) nature, the R component significantly affects the performance and efficiency of a converter. Many studies have discussed the issue and proposed various limits and boundaries for the operating modes [2.9], [2.11]-[2.12]. On the other hand, the resistance of the cell also affects its time constant and thus the parameter β [2.9].

$$\beta_i = \frac{T_i}{R_i C_i} \tag{2.5}$$

The parameter β value describes the SC charging characteristic. The possible charging current waveforms are presented in Figure 2.3. As β increases, so does the capacitor`s charging current. For β much greater than unity, the current is in the shape of a spike and of great magnitude. This results in a decrease in efficiency and causes component stresses in hard-switched SC converters, which is their main disadvantage.

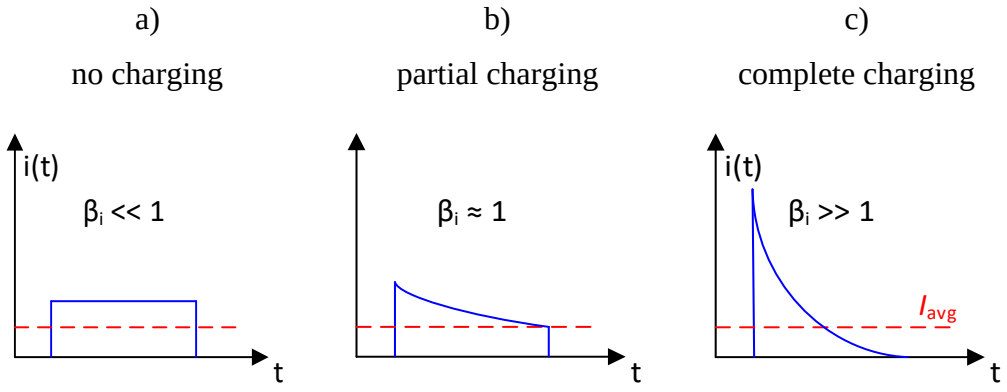


Figure 2.3: Charging current waveforms for a hard switched SC converter for different values of β_i.

2.2. Resonant SC converter (ResSC) and the principle of its operation

One of the recent trends in the area of power electronics is to increase the switching frequency of power converters, which enables smaller passive components to be used and thus reduces the overall size of a device. Increasing the operational frequency, however, leads to higher switching losses of the semiconductor switches, which can be described as:

$$P_S = (E_{ON} + E_{OFF}) f_{SW} \tag{2.6}$$

where E_{ON} and E_{OFF} is the energy of a single transistor`s turn-on and turn-off, respectively, while f_{SW} is the switching frequency. If changes in the voltage ($U(t)$) and current ($I(t)$) are assumed to be linear, the turn-off process of a semiconductor can be presented as in Figure 2.4.

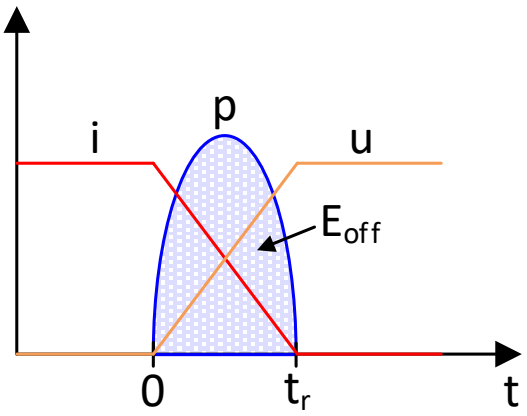


Figure 2.4: Idealised turn-off process of a transistor with linearised changes in current and voltage.

The energy of a single turn-off can be expressed by the formula:

$$E_{OFF} = \int_0^{t_s} u_T i_T dt = \int_0^{t_s} p dt \tag{2.7}$$

where time $0 \div t_s$ is the duration of the turn-off process and p is the instantaneous power. If the switchover of a transistor occurs in zero voltage (ZVS) or zero current (ZCS) conditions, the process is performed with zero energy and thus no power losses occur.

By introducing a low-volume inductor into a circuit, an SC can operate in resonance, which ensures zero current switching (ZCS). This makes it possible to significantly reduce switching power losses, improve the overall converter efficiency [2.13]-[2.14], and limit the inrush currents in the converter circuits. Depending on the application and the expected output power, a ResSC converter can be based on various semiconductor devices such as Si MOSFETs, IGBTs, SiC MOSFETs, and GaN but also on thyristors [2.15]. The issues with optimising an SC converter have been widely investigated in [2.16]-[2.21]. In the case of the resonant type of SC converter in which the current waveforms are of a pulse nature, the efficiency will be dependent on the ohmic losses and also on the parameters of the switched, resonant *LC* branch of the converter and its operational frequency. This will be addressed in Section 3.6 of this dissertation for the proposed topology.

2.3. Switched capacitor converters in power electronics: the voltage doubler

One of the basic topologies that is based on the ResSC idea is a voltage doubler [2.22]. The converter is presented in Figure 2.5 and provides a voltage gain close to two, thereby maintaining a high level of efficiency and a graceful design.

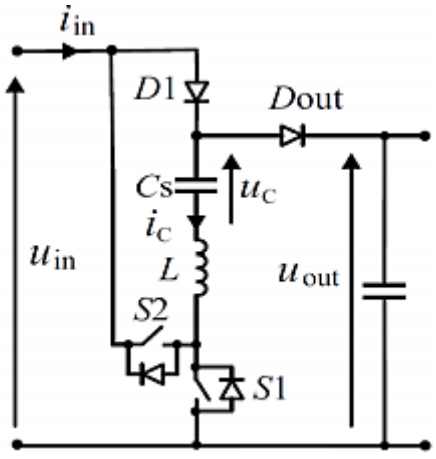


Figure 2.5: An SC voltage doubler converter [2.22].

The resonant switched capacitor voltage doubler`s (SCVD) resonant branch is formed by the switched capacitor *Cs* and the inductance *L*. The characteristic impedance of this series *LC* circuit and its angular frequency are given as:

$$\rho = \omega L = \sqrt{\frac{L}{Cs}}\ ;\ \omega = \sqrt{\frac{1}{LCs}} \tag{2.8}$$

The operational cycle of an SCVD consists of two stages. In the first stage (Ts_I), the switched capacitor is charged and in the second (Ts_{II}), it is discharged. The full cycle is presented in Figure 2.6.

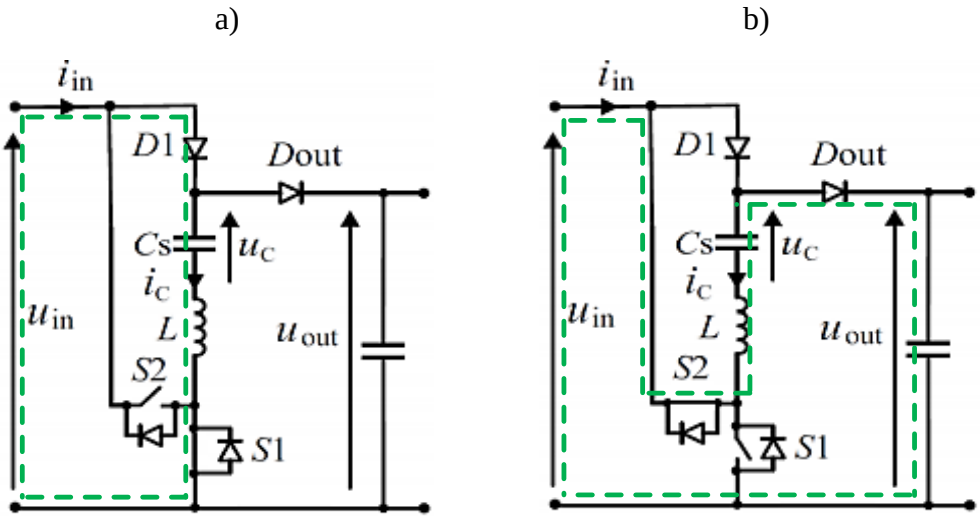


Figure 2.6: The concept of the operation of an SC voltage multiplier (SCVM).

The SCVM charging stage occurs in the time interval Ts_I

$$T_{SI} = \frac{\pi}{\omega_{SI}} = \pi\sqrt{LC_S} \tag{2.9}$$

When the switch S_1 is on and the current flows through this diode D_1, the capacitor C_S, the inductor L, and the switch S_1 itself. The current i_{SI} path is illustrated in Figure 2.6a and its waveform is described by (2.10) similarly as for SCVM converters presented in [2.15]

$$i_{SI}(t) = \frac{U_{IN} - U_{Cmin}}{\rho} sin\omega t = I_{SIm} sin\omega t \tag{2.10}$$

where U_{IN} is the supply voltage (assumed constant), U_{Cmin} is the minimum voltage across the capacitor C_S, ρ is the characteristic impedance of the series LC circuit,

ω is an angular resonant frequency of the series LC circuit, L is the resonant inductance, and I_{SIm} is the current amplitude.

Voltage across the switched capacitor C_S is given by the following equation:

$$u_{CSI}(t) = U_{in} - (U_{in} + U_{Cmin})cos\omega t \tag{2.11}$$

In the second time interval (Ts_{II}) of the energy exchange cycle, the capacitor Cs discharges while the output capacitor C_{out} charges. Therefore, the energy transfer occurs. The current path goes through the switch S_2, the inductor L, the capacitor C_S, the output diode D_{out}, and finally through the output capacitor. The current and voltage during the time interval Ts_{II} are represented by equations (2.12) and (2.13).

$$i_{SII}(t) = \frac{U_{IN} - U_{OUT} - U_{Cmax}}{\rho} sin\omega t = I_{SIIm} sin\omega t \tag{2.12}$$

where U_{Cmax} is the maximum voltage across the capacitor C_s that is reached at the end of its charging process, and Is_{IIm} represents the discharging current amplitude. The duration of Ts_{II} is equal to Ts_I (2.9)

$$u_{CSiI}(t) = U_{OUT} - U_{IN} + (U_{IN} - U_{OUT} + U_{Cmax})cos\omega t \tag{2.13}$$

Figure 2.7 presents idealised waveforms of the input current of SCVM, which corresponds with the stages of the operation presented in Figure 2.6.

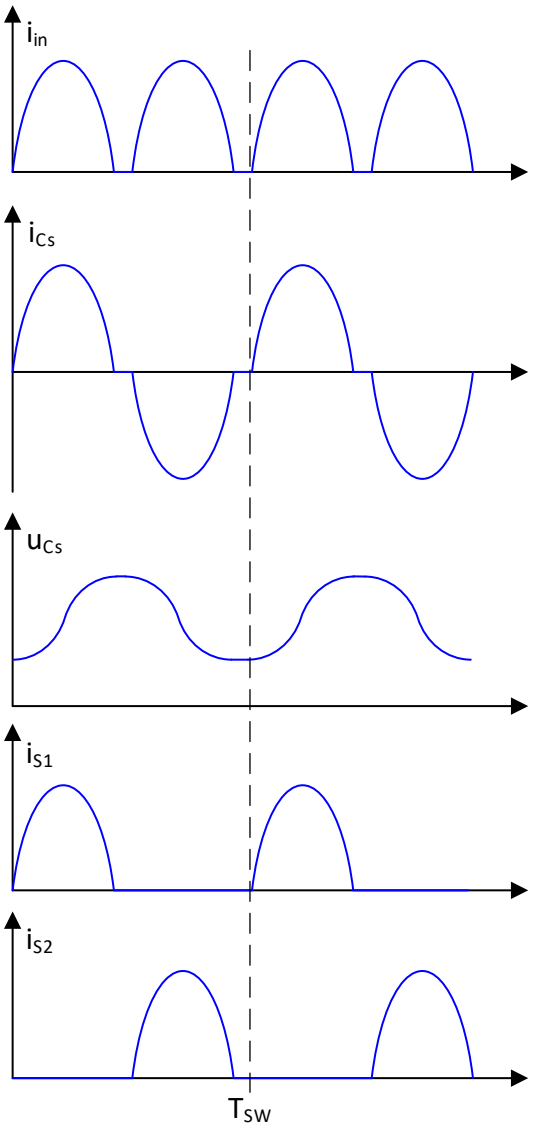


Figure 2.7: Idealised waveforms of the input current of SCVD.

For the theoretical consideration of the SCVD, no voltage drops across diodes and resistances can be assumed. In the case of the sinusoidal currents during charging and discharging stages, the maximum voltage on the switched capacitor u_{cmax} equals:

$$u_{CSI}(T_{SI}) = U_{Cmax} = 2u_{CD} - U_{Cmin} \tag{2.14}$$

at the end of charging the capacitor C_S and (2.13):

$$uU_{Cmin} = U_{CSII}(T_{SII}) = 2(U_{OUT} - U_{IN}) - U_{Cmax} \tag{2.15}$$

at the end of discharging *Cs*. From (2.13) and (2.15), it follows that the output voltage:

$$U_{OUT} = 2U_{IN} \tag{2.16}$$

3. The Concept and Operating Principle of a Switched Capacitor Active Balancing Converter for Series-Connected Capacitors

The following sections describe the concept and operating principle of an SCABC circuit. Theoretical, idealised waveforms are presented together with the equations that describe the circuit's behaviour. Furthermore, all of the possible operating modes are discussed as well as the basics of the control, size of the circuit's components, and its efficiency.

3.1. The Converter

The proposed circuit is a resonant switched capacitor converter. It was built of seven semiconductor switches and the resonant *LC* branch that is formed by a switched capacitor C_S and a low volume inductor *L*. The topology of the converter is presented in Figure 3.1.

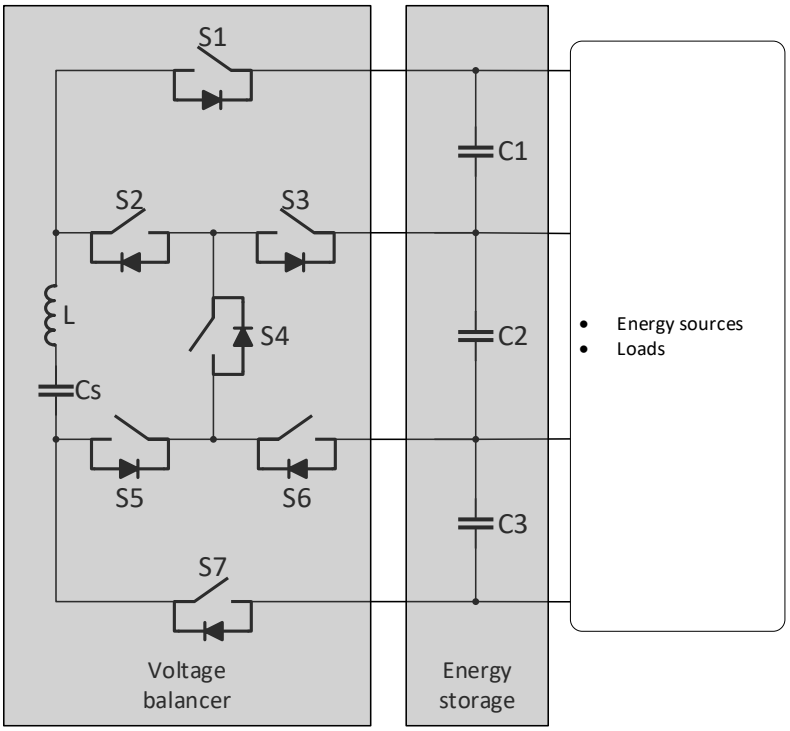


Figure 3.1: The switched capacitor-based balancer for three series-connected capacitors. C_1 to C_3 – series-connected capacitors, S_1 to S_7 – transistor switches, *L* and C_S – inductor and capacitor of the SC resonant branch.

The operating principle of an SCABC is based on two main stages and assumes that the overcharged capacitor will be discharged to the switched capacitor and in the next step the undercharged capacitor is charged with the energy that was stored

in the switched capacitor. In this way, the energy transfer is possible between any of the three capacitors in the series branch provided that the voltage on the discharged capacitor exceeds the voltage on the charged one. When the resonant inductor L is used, the inrush currents in C_S are limited and a resonance phenomenon occurs that causes the SCABC to operate in the zero-current switching (ZCS) mode, which improves the circuit`s efficiency. A hard switching operation, however, is also possible in the case of the investigated topology, which will be discussed in Section 3.4.

3.2. The operating principle

In order to provide the desired energy flow by the SCABC operation, the correct switching strategy for the semiconductor switches must be introduced, which will be discussed in Section 3.3. The operating principle of the balancer will be presented based on the analysis of its operations scenario when the C_1 capacitor is being discharged and the C_3 is being charged (as an example). For the following description of the circuit operation, it is assumed that:

1. The capacitor C_1 is charged with a higher voltage than capacitor C_2.
2. The switched capacitor C_S has no energy stored, and therefore, there is no voltage across it.
3. All of the circuit's components are free from parasitic resistances.

Figure 3.2 presents the path of current flow during the two stages of the balancing process.

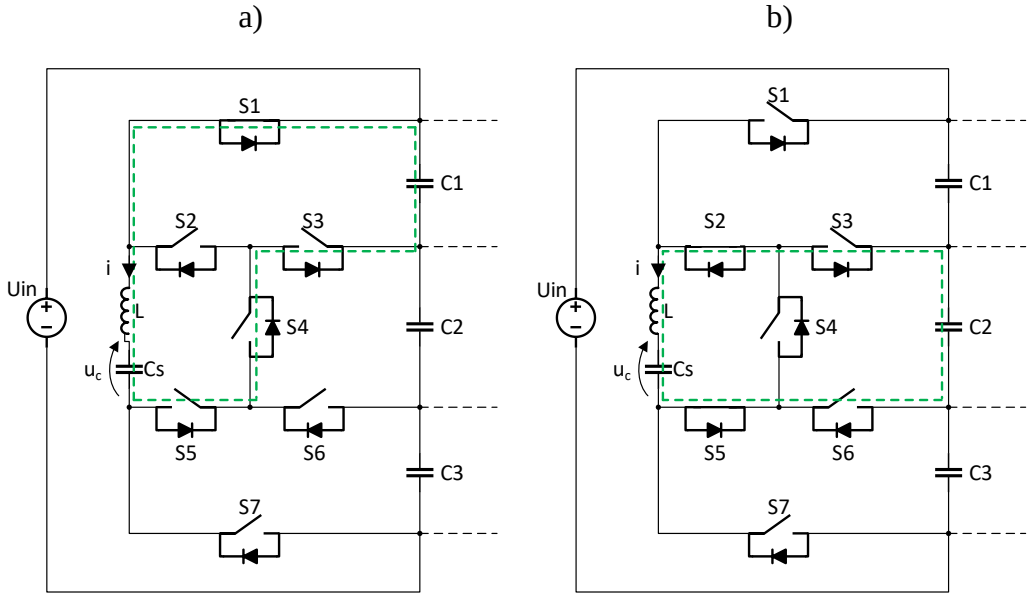


Figure 3.2: Paths for the current flow: the operation scenario when C_1 is discharged (a) and C_2 is charged (b).

Stage s_I: with transistor S_1 switched on, the energy that was stored in the capacitor C_1 is transferred to capacitor C_S. The current path is composed of the following components:

1. The transistor S_1.
2. The resonant branch L, C_S.
3. The reverse diodes of S_5, S_4, S_3.

Stage s_{II}: When Cs is fully charged, the S_1 switch is turned off while the S_2 and S_5 are turned on. The energy that was stored in Cs is transferred to capacitor C_2. The current path is closed *via*:

1. The S_2, and S_5 transistors
2. The resonant branch L, C_S.
3. The reverse diodes of S_3, S_6.

Figure 3.3 presents the operating cycle of the SCABC. The switching cycle of the converter (T) was divided into the following parts:

1. ts_I – the switched capacitor C_S charging time interval (stage s_I).
2. ts_{II} – the discharging time interval (stage s_{II}).
3. td – the time interval required for the transistors to be turned-off (dead-time).

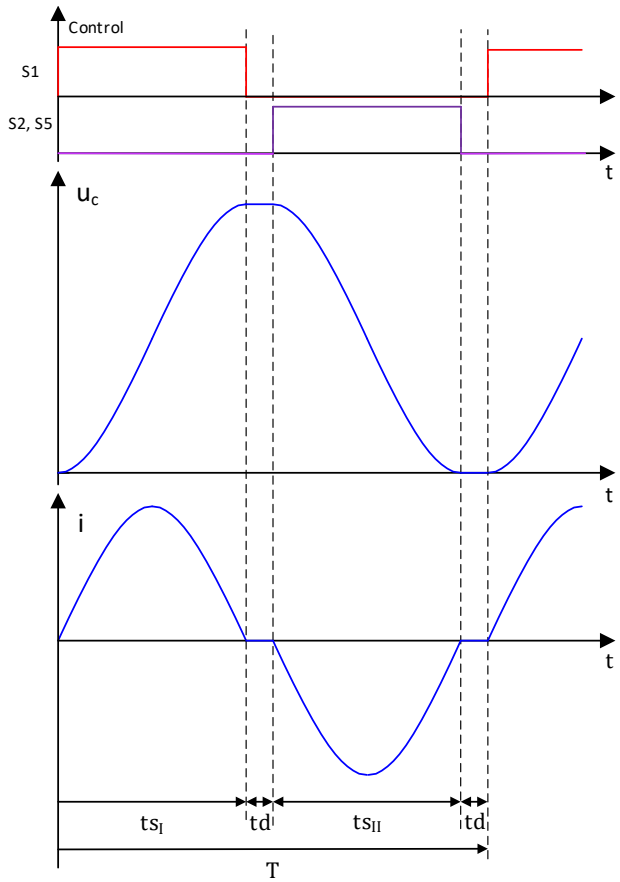


Figure 3.3: The operating cycles of the SCABC: control signals for the switches that were active in balancing from the C_1 to the C_2 capacitor, u_C – switched capacitor voltage, i – switched capacitor current.

The charging and discharging process of the switched capacitor occurs in the oscillatory LC circuit with the characteristic impedance and the angular resonant frequency that is given by:

$$\rho = \omega L = \sqrt{L/C}\ ;\ \omega = \sqrt{1/(LC)} \tag{3.1}$$

The charging current i_{SI} and the discharging current i_{SII} are as follows:

$$i_{SI}(t) = \frac{u_{CD} - u_{Cmin}}{\rho} sin\omega t = I_{SIm} sin\omega t \tag{3.2}$$

$$i_{SII}(t) = \frac{u_{Cmax} - u_{CC}}{\rho} sin\omega t = I_{SIIm} sin\omega t \tag{3.3}$$

where u_{CD} is the voltage on a discharged capacitor in the series branch, u_{CC} is the voltage on a charged capacitor in the series branch, u_{Cmin} and u_{Cmax} are minimum and maximum voltages on the switched capacitor, respectively, L is the inductance of the resonant circuit, and I_{SIm} and I_{SIIm} are the current amplitudes.

The voltages across the switched capacitors during the charging (u_{CSI}) and discharging (u_{CSII}) cycles are given by the equations as follows:

$$u_{CSI}(t) = u_{CD} - (u_{Cmin} - u_{CD}) cos\omega t \tag{3.4}$$

$$u_{CSI}(T_{SI}) = u_{Cmax} = 2u_{CD} - u_{Cmin} \tag{3.5}$$

$$u_{CSII}(t) = u_{CC} - (u_{Cmax} - u_{CC}) cos\omega t \tag{3.6}$$

$$u_{CSII}(T_{SII}) = u_{Cmin} = 2u_{CC} - u_{Cmax} \tag{3.7}$$

The transferred energy reaches its maximum value when the voltage of the switched capacitors decreases to zero during the discharging period:

$$u_{Cmin} = 0;\ u_{Cmax} = 2u_{CD} \tag{3.8}$$

after which, the energy W is drained from a discharged capacitor to charge a switched capacitor:

$$W = \frac{1}{2} C_S {u_{Cmax}}^2 = 2C_S {u_{CD}}^2 \tag{3.9}$$

From the fundamental definition of power and equation (3.9):

$$P = Wf\ ; \quad P = \frac{1}{2} C_S {u_{Cmax}}^2 f_{SW} \tag{3.10}$$

where f_{SW} is the switching frequency of the balancer:

$$f_{SW} = \frac{1}{T} = \frac{1}{t_{SI} + t_{SII} + 2t_d} \tag{3.11}$$

However, to maintain ZCS, the switching frequency f_{SW} must not be greater than the resonant frequency f_{RES} of the converter, which allows the current i decrease to zero:

$$f_{RES} = \frac{\omega}{2\pi} \tag{3.11}$$

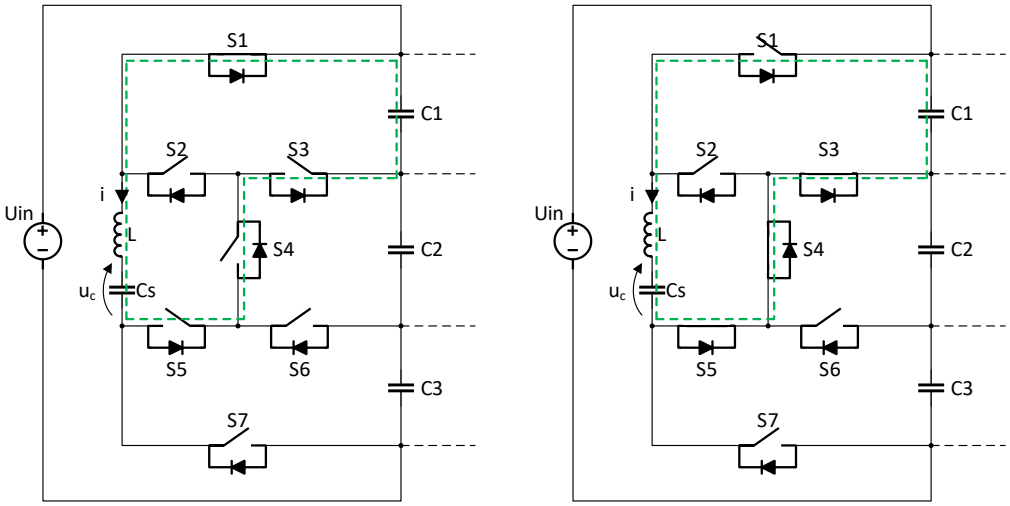
with ω given in (3.1).

From (3.10) and the above condition, it can be determined that the balancing process is performed with full power when the converter is operating with a frequency that is equal to the resonant frequency

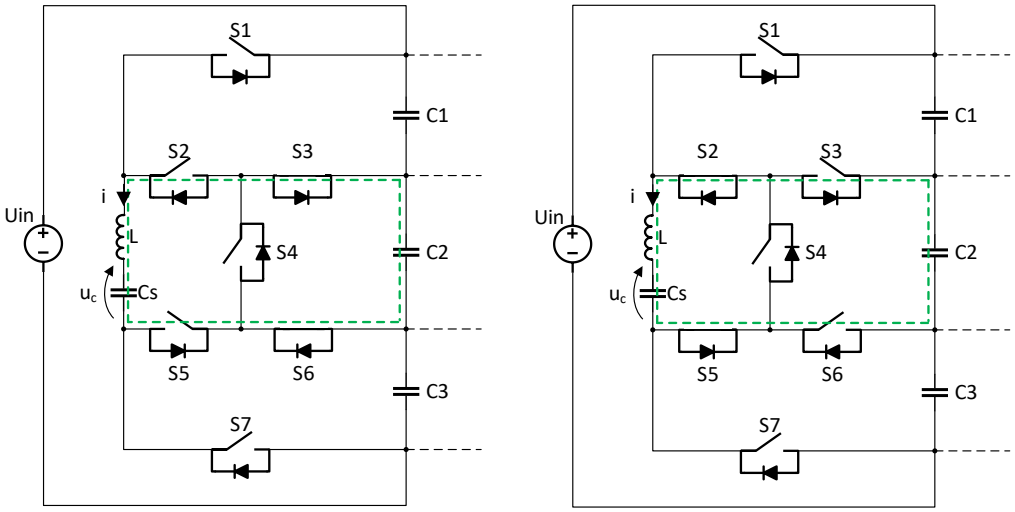
$$P = P_{MAX} \quad \text{when} \quad f_{SW} = f_{RES} \tag{3.12}$$

Figure 3.4 presents all of the possible scenarios of the charging and discharging of one of the series-connected capacitors.

a)



b)



c)

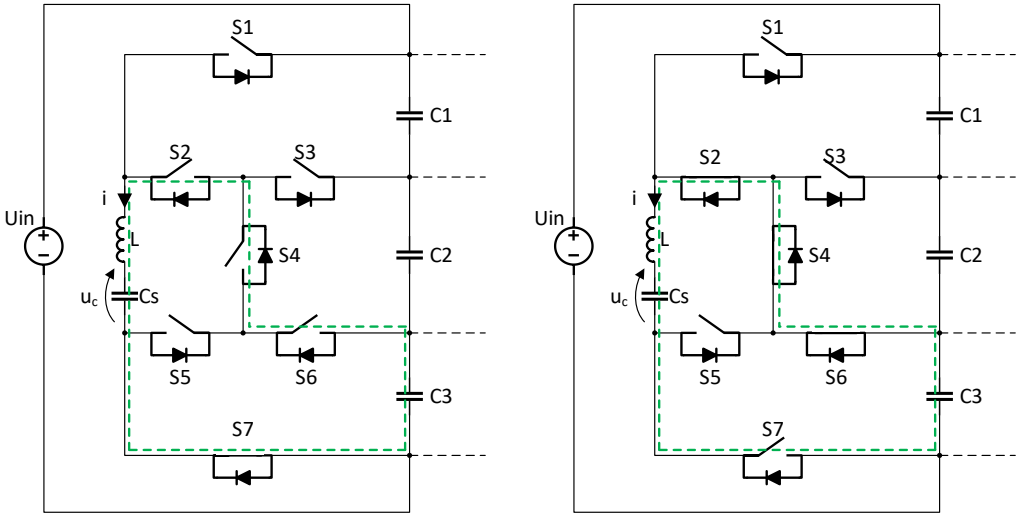


Figure 3.4: The operation scenario when a) discharging and charging C_1, b) discharging and charging C_2, c) discharging and charging C_3.

3.3. Basics of SCABC control.

Because the balancing process consists of two stages s_I and s_{II}, each requires its own control signal in order to turn the semiconductor switches on. However, because the stages are successive, those signals can be complementary, and therefore, they can be sourced from one generator. With the two pulse signals given, they must be correctly distributed in order to turn on the appropriate transistors. Table 3.1 presents the requirements for activating the switches depending on the operating mode.

Table 3.1: The active semiconductors for various balancing scenarios

-	Charging stage s_I		
Capacitor	C_1	C_2	C_3
Active switch	S_3, S_4, S_5	S_2, S_5	S_2, S_4, S_6
-	Discharging stage s_{II}		
Capacitor	C_1	C_2	C_3
Active switch	S_1	S_3, S_6	S_7

The concept of the core control system is presented in Figure 3.5. The converter can be used in various applications, which will be discussed in the further chapters of this dissertation. However, the baseline control always remains the same, and receives its commands from the master algorithm.

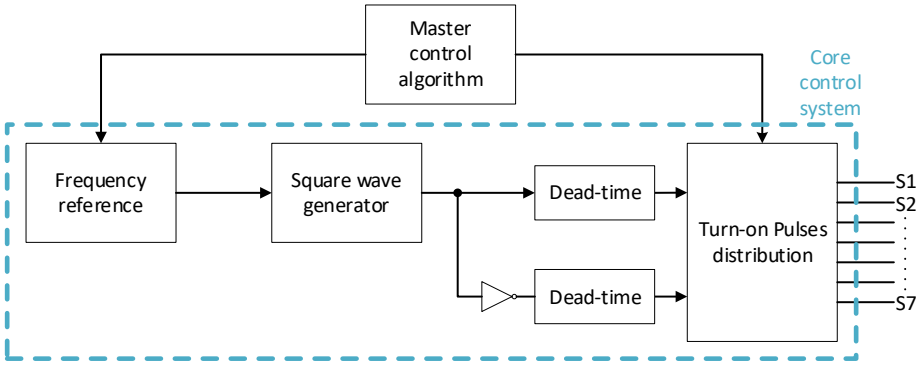


Figure 3.5: The core control system for the SCABC.

The Square wave generator produces the signal of the frequency that is given by the reference block, and is limited to $f_{SW} \leq f_{RES}$. Then, the signal is inverted, and two complementary waveforms are obtained. The dead time *dt* is added, thereby securing the correct turn-off of the transistor switches. The pulse distribution block is fed with the orders that the capacitors from the series branch (C_1 to C_3) are to be charged and discharged and delivers the gate signals as presented in Table 3.1.

Exemplary control waveforms are presented in Figure 3.3, driving transistors S_1, S_2, and S_5.

3.4. Special operating scenarios

Special operating scenarios can include:

1) The C_S capacitor being charged from two series-connected capacitors.

2) Hard switching.

As was given in equation (3.9), the energy that is transferred in the converter is strongly dependent on the voltage on the discharged capacitor u_{CD}. By introducing an appropriate switching pattern (different from the one presented in Table 3.1), it is possible to charge the switched capacitor C_S from two capacitors of a series-connected branch simultaneously. This results in increasing the discharge voltage u_{CD} and thus the energy that is transferred by the converter. Figure 3.6 illustrates the current path for the operating scenarios in which two capacitors from a series-connected branch are discharged simultaneously.

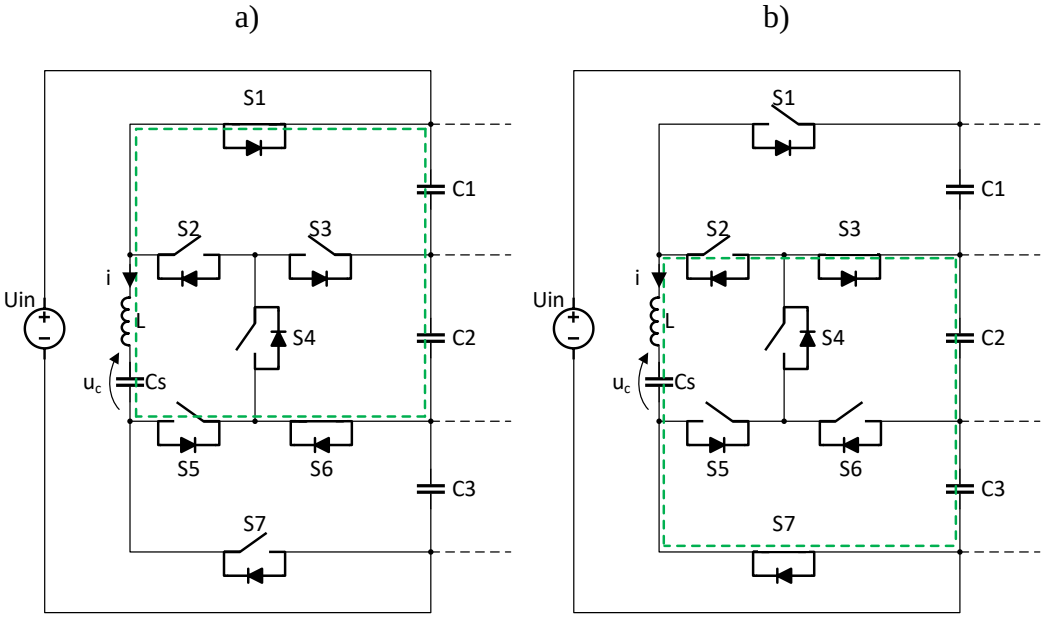


Figure 3.6: Discharging from two capacitors simultaneously: a) C_S charged from C_1 and C_2: active switches S_1, S_6; b) C_S charged from C_2 and C_3: active switches S_3, S_7.

On the other hand, increasing the u_{CD} by doubling the number of discharged capacitors leads to an increase in the amplitude of the charging current I_{Sim}, which can be derived from (3.2). This can cause increased stress or result in exceeding the limit values of the circuit`s components. To overcome this issue, a hard switching

operation can be used, but this sacrifices the efficiency of the SCABC by introducing switching losses in the transistors as described in Section 2.3.

Figure 3.7 presents the waveforms for a hard switching operating scenario. When the current monitoring stage is introduced into the control algorithm, the control signals for the switches can be disabled when the set current limit is exceeded. This maintains the current amplitudes within the safety limits. The path for current flowing in such an operating scenario is presented in Figure 3.8.

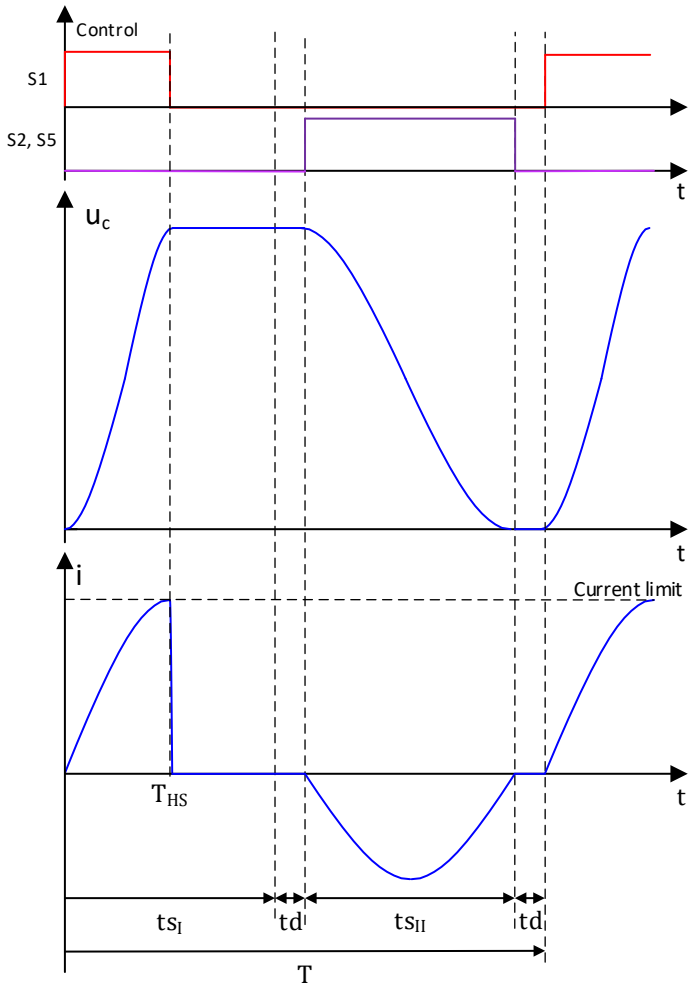


Figure 3.7: The operating cycle of the Switched Capacitor Active Balancing Converter with hard turn-off at time T_{HS}, which was caused by reaching the current limit.

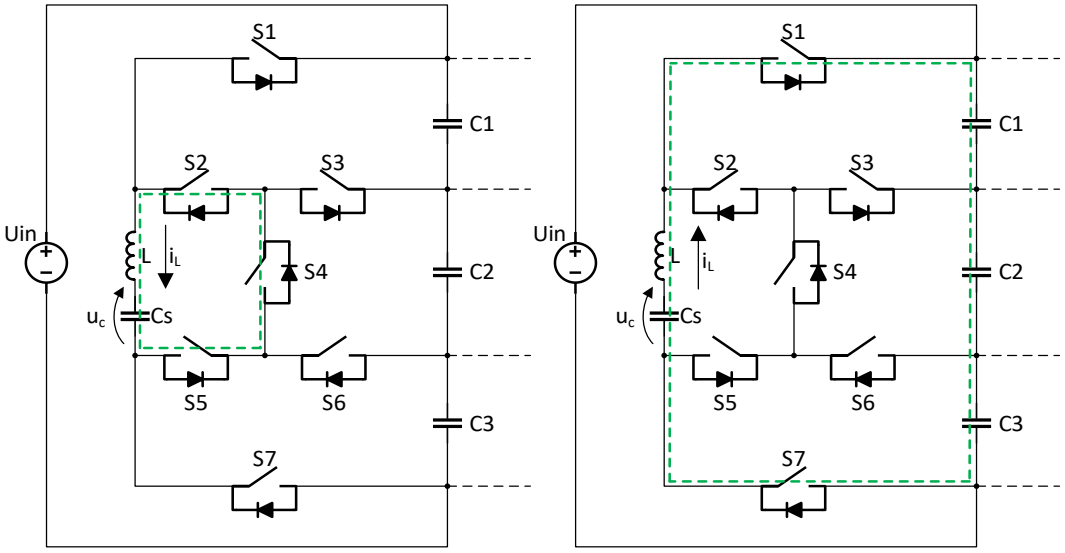


Figure 3.8: Current path after a hard turn off (diodes conduction).

3.5. Sizing of the SCABC components

The switched capacitor size can be determined based on an analysis of the energy that has been stored. With the operation at full power, the total energy of switched capacitor C_s is transferred to the selected capacitor in a series-connected branch. Taking (3.9), (3.10) and (3.11) into account, it can be derived that

$$C_S \geq \frac{P_{max}}{2{u_{CD}}^2 f_{SW}} = \frac{P_{max}}{2{u_{CD}}^2}(t_{SI} + t_d) \tag{3.13}$$

The desired charging time ($t_{SI} = \pi\sqrt{LC}$) will be achieved once the inductance of the choke is as follows:

$$L = \left(\frac{t_{SI}}{\pi}\right)^2 \frac{1}{C_S} = \frac{2{u_{CD}}^2 t_{SI}}{\pi^2 P_{max}\left(1 + \frac{t_d}{t_{SI}}\right)} \tag{3.14}$$

The maxima of the average value of a current is assumed to be present during stage s_I of the operation. Using (3.10) and I_{SI} from (3.2) and with $u_{Cmin} = 0$, it equals:

$$I_{SIAV} = \frac{P_{IN}}{U_{IN}} \Rightarrow I_{SIAV} = 2C_S u_{CD} f \tag{3.15}$$

The average value can be also derived from the time-dependent equation of stage s_I:

$$I_{SIAV} = \frac{1}{T}\int_0^{t_{SI}} I_{SIm}\, sin\omega t dt = 2C_S u_{CD} f = 2\frac{f}{\omega} I_{SIm} \tag{3.16}$$

To obtain the dependency of the energy of the inductor versus the converter`s power, the amplitude of the current in the choke must be known. By equating (3.15) with (3.16) and using (3.1), (3.13) and (3.14)

$$I_{SIm} = \pi \frac{P_{IN}}{2u_{CD}} \left(1 + \frac{t_d}{t_{SI}}\right) \tag{3.17}$$

Equation (3.17) provides the maximum current while a circuit is operating. The transistors that are used to build the converter must be able to withstand the current that is distributed to specific branches by considering its RMS and pulse values. By analysing the circuit (presented in Figure 3.2), it can be derived that the maximum voltage stress on the transistors is equal to 2/3 of the input DC voltage U_{IN}.

3.6. Power losses and efficiency of the circuit

This section presents an analysis of the sources of the power losses in the SCABC. The majority of the circuit`s losses were conduction losses, which were dependent on the current amplitude and how performant are the components of the circuit. The switching turn-off losses were nearly eliminated when the ZCS strategy was used and were transients on the parasitic elements of the semiconductors. Because of the high dynamics of the voltage balancing process, the efficiency considerations are simplified with the following assumptions:

1. The formulas were valid for a single balancing period, and therefore, for a given value of voltage across the capacitors of the balanced branch.
2. The formula represented the worst-case scenario in which the switched capacitor voltage u_{Cmin} and u_{CC} was zero, therefore, the amplitudes of the flowing currents were the highest possible.
3. The equations were formulated to indicate the impact of the circuit`s components and switching frequency on the overall converter efficiency rather than to provide a full description of the circuit`s performance. To determine this, a time-dependent equation had to be introduced.

Taking the above into consideration, the author did not calculate the circuit's efficiency in this dissertation using the model presented. However, the efficiency was measured in the experimental setup, where the balancing process dynamics was none because the balancer operated in the steady state as a constant output power voltage multiplier. A detailed description and results are presented in Section 5.3.3 of this dissertation.

3.6.1. Power losses in the SCABC

In the presented converter, the sources of power losses could be classified into four groups:

- Conduction losses
- Switching losses
- Losses associated with the core-based inductors
- Other losses where the electronic power supply and gate circuits were the main parts

1. Losses associated with the semiconductor components

Conduction losses:

The majority of power losses in the circuit were conduction losses associated with the on-state resistance R_{DS_on} of a transistor's channel and the forward voltage of the diodes. The conduction power losses of the switches were proportional to the squared RMS value of the current and are expressed as follows:

$$\begin{aligned} \Delta P_{ST} &= \frac{{I_{SIm}}^2}{2} m R_{DS\_on} \frac{t_{SI}}{T} + \frac{{I_{SIIm}}^2}{2} n R_{DS\_on} \frac{t_{SII}}{T} \\ &= \frac{R_{DS\_on}}{2T} \left(m {I_{SIm}}^2 t_{SI} + n {I_{SIIm}}^2 t_{SII} \right) \end{aligned} \tag{3.18}$$

where m and n were the number of conducting transistors in a charging and discharging cycle, respectively.

The power losses in the reverse diodes were proportional to the average value of the current

$$\Delta P_{SD} = \frac{2 I_{SIm}}{\pi} k U_D + \frac{2 I_{SIIm}}{\pi} l U_D \tag{3.19}$$

where k and l were the number of conducting diodes in the charging and discharging cycle, respectively.

Switching losses:

Because of the ZCS switching strategy that was used in the presented converter, the switching losses in the transistors were significantly reduced [3.1] and were limited only to losses that were associated with the charging characteristic capacitances of the device C_{gs}, C_{gd}, and C_{ds}. This part of the losses is called C_{oss} losses. The C_{oss} losses occurred in a transistor when the energy that was stored in

the output capacitance (C_{oss}) was dissipated in the transistor structure during the turn-on process. The energy was dependent on:

1. The transistor's parameters,
2. The voltage across the transistor,
3. The switching frequency,
4. The commutation processes.

The commutation process caused the removal of the Q_{oss} from the transistor's C_{oss} before it was turned-on. These zero-voltage switching (ZVS) conditions are created by the circuit operation and do not occur in some SC converters. The proposed converter for voltage balancing does not operate in the ZVS mode. However, when using GaN transistors, the converter`s efficiency will be marginally affected by the C_{oss} losses. GaNs with their very low C_{oss}, are a justified choice for an SCABC. Furthermore, with an operation frequency far below the tens or hundreds of [MHz] range, which seems to be the boundary for GaN devices, the C_{oss} losses are even more meaningless [3.5]-[3.6].

Because the converter operated in the ZCS mode, the reverse recovery losses (Q_{rr} losses) in the diodes were assumed not to be significant for the efficiency of the converter.

2. Power losses in the switched capacitor C_S

The conduction losses in a component were proportional to the input value of the RMS current with the assumption that the main source of the losses is the Equivalent Series Resistance (ESR) of the capacitor [3.2]

$$\Delta P_C = \frac{R_{ESR}}{2T}\left(I_{SIm}{}^2 t_{SI} + I_{SIIm}{}^2 t_{SII}\right) \tag{3.20}$$

3. Power losses in the resonant choke L

The power losses in this inductive component can be divided into winding and magnetic core losses. Winding losses are associated with the windings` resistance and are proportional to the value of the RMS current that is flowing through the inductor:

$$\Delta P_{LW} = \frac{R_W}{2T}\left(mI_{SIm}{}^2 t_{SI} + nI_{SIIm}{}^2 t_{SII}\right) \tag{3.20}$$

Core losses can be estimated using the Steinmetz equation:

$$\Delta P_{LC\_VOL} = k f^{\alpha} B_{MAX}{}^{\beta} \tag{3.21}$$

where ΔP_{LC} stands for the losses per core volume, f is the frequency of the magnetic flux swing, which is equal to the switching frequency of the converter, and B_{MAX} is the peak flux density. Factors k, α, and β are the so-called Steinmetz coefficients that are characteristic for a given magnetic material in a specified frequency range. By introducing the calculated B_{MAX} [3.3], the core`s physical characteristics and the effective permeability of the gapped core [3.4]

$$\Delta P_{LC} = k f^{\alpha} \left(\frac{\mu_E N \frac{I_{SIm} + I_{SIIm}}{2}}{l_C} \right)^{\beta} A l_C \tag{3.22}$$

$$\mu_E = \frac{\mu_R \mu_0}{1 + \frac{\mu_R l_G}{l_C}} \tag{3.23}$$

where μ_0 – effective permeability of the gapped core, μ_0 – free space permeability, μ_R – magnetic core permeability, N – number of turns, l_C – effective length of magnetic core, A – core cross-section, and l_G – air gap length.

3.6.2. The efficiency of the converter

In the previous section, the power losses were evaluated. These losses can be used to approximate a converter`s efficiency:

$$\eta \approx 1 - \frac{\Delta P_{ST} + \Delta P_{SD} + \Delta P_C + \Delta P_{LW} + \Delta P_{LC}}{P_{IN}} \tag{3.24}$$

Using equations (3.17) - (3.22) with the assumption that the time intervals t_{SI} and t_{SII} were equal as well as the amplitudes of current I_{SIm} and I_{SIIm}

$$\begin{aligned} \eta \approx 1 - \Bigg(& \frac{t_d + t_{SI}}{\partial_2 u_{CD}} \Big(\frac{\pi}{2} f (R_{ESR} \partial_1 + R_W \partial_1 \\ & + {I_{SIm}}^2 R_{DS\_on} t_{SI} (m + n) + 2 I_{SIm} U_D (k + l) \Big) \\ & + k f^{\alpha} \left(\frac{\mu_E N I_{SIm}}{l_C} \right)^{\beta} A l_C \Bigg) \end{aligned} \tag{3.25}$$

where $\partial_1 = t_{SI} + {I_{SIm}}^2 t_{SI} + {I_{SIm}}^2$; $\partial_2 = 2 I_{SIm} t_{SI}$.

There are essential conclusions that can be derived from the efficiency equation (3.25):

1. The discharged capacitor initial voltage has an impact on the efficiency of an SCABC: the higher it is, the better the efficiency
2. The efficiency is slightly decreased when the power increases because of the resistive losses,

3. The amplitude of the charging current (3.17) not only depends on the power but also on the relationship of the time intervals t_d and t_{SI} (dead-time and conduction time). Thus, for a high-efficiency design, the proportion of these time intervals should be minimized in order to limit the losses.

4. Switched Capacitor Active Balancing Converter simulation and experimental setup

This chapter describes the simulation and experimental research on the proposed topology that was used to prove the concept. The operating scenarios that were described in the previous sections were validated and the resulting waveforms are presented. Furthermore, a hardware design concept is discussed. The results are discussed as the chapter`s summary.

4.1. Simulation model description

To prove the concept of the proposed voltage balancing converter, a simulation model was developed. The power electronics package Specialized Power Systems in MATLAB®/Simulink® [4.1] was used to build and investigate the model. Because simplified models of the semiconductors were used, Simulink has the ability to verify the power electronics circuits quickly and easily, neglecting vastly complicated phenomena that can occur in real semiconductor components.

The model of the balancer is presented in Figure 4.1, while the parameters that were used in the simulation are presented in Table 4.1. The parameters of the parasitic components were arbitrary as the major purpose of simulation research was focused on proving the concept of the circuit`s topology and its control. A clamping diode, which was connected parallel to the switched capacitor, was introduced as a simple circuit protection. Such a setup prevents any negative voltage increase on the capacitor. It also determines the minimum initial voltage conditions and limits the circuit`s current dynamics and protects against overvoltage stresses.

Table 4.1: Simulation model parameters.

Switched capacitor	C_S	250[nF]
Inductance	L	5[μH]
DC-link capacitors	C_1,C_2,C_3	250[μF]
DC source	Uin	200[V]
Parasitic resistance	R_{PR}	80[mΩ]
Switching frequency	f_{SW}	125[kHz],60[kHz]
Dead-time	t_d	100[ns]
Transistors on-state resistance	R_{DS_on}	20[mΩ]

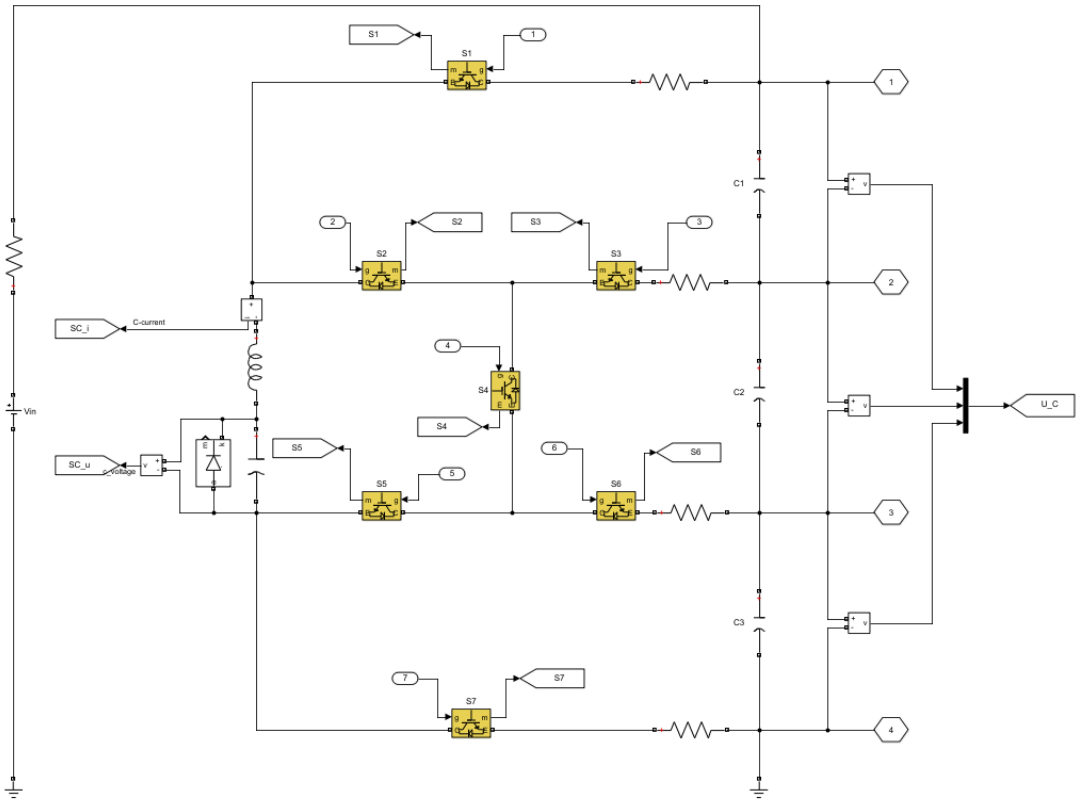


Figure 4.1: The power circuit of the balancer modelled in MATLAB®/Simulink®.

The control algorithm, which was briefly described in Section 3.3, was also developed in the simulation model. The schematic of the pulse distribution block is presented in Figure 4.2. Its input must be fed with the specific number of capacitors in the series-connected branch that is to be discharged and charged. From the functionality standpoint, it ensures that the operation mode only changes during a dead-time t_d, and therefore, no unexpected hard switching occurs due to a change in a block`s input signals. The change is also executed only after the energy exchange cycle has been completed, thus preventing a dead-lock in the balancer operation. The logic is based on two switch-case type functions, each of which is provided with a capacitor selection from the master control algorithm and redistributes the control signal to the transistor gates. Figure 4.3 presents an example for the redistribution of the control signal for when capacitor number two is being discharged. From Table 3.1, one can see that the active transistors in this case are S_3 and S_6, and therefore, in that manner, the control signal is fed to those transistors.

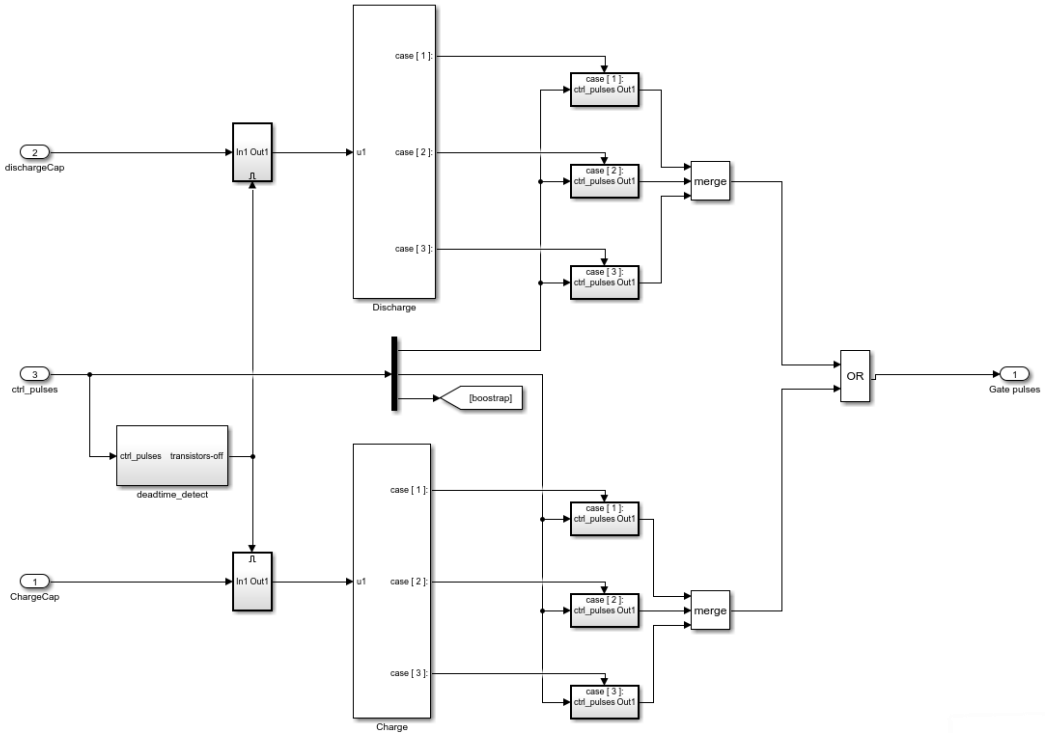


Figure 4.2: Turn-on pulse distribution algorithm.

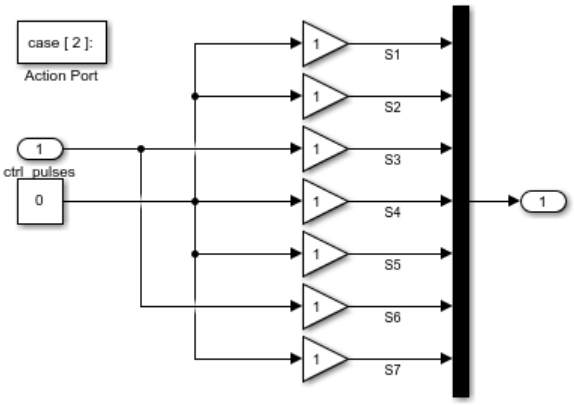


Figure 4.3: Turn-on signal redistribution: C_2 discharge.

4.2. Simulation results

The results of the simulation of the circuit are presented in several of the following figures. Figures 4.4 to 4.7 present the voltages of three, series-connected capacitors, the voltage and current of the switched capacitor, and the control signals. Figure 4.8 presents the voltage stress on the semiconductors in the selected operation mode. A complete collation of voltage stresses is presented in Table 4.2. An operation with a lower switching frequency was investigated. Figure 4.9 and Figure 4.10 present the results of this scenario with f_{SW} = 60[kHz] and its impact on the balancing process dynamics. Moreover, the special operating scenarios that

were described in Section 3.4 were simulated. Figure 4.11 presents a high-rate energy exchange operation, in which the switched capacitor is charged from two series-connected capacitors simultaneously. In Figure 4.12, the hard-switching operating scenario, in which the switched capacitor charging current was limited to 18[A], is presented. The initial voltages of the series-connected capacitors of the DC link were selected to meet the following author requirements:

1. The balancer would operate at full power (full discharge of the capacitor C_S) for a specific time interval.
2. The duration of the complete balancing would not be too long, and therefore, the clarity of the figures would not be diminished.

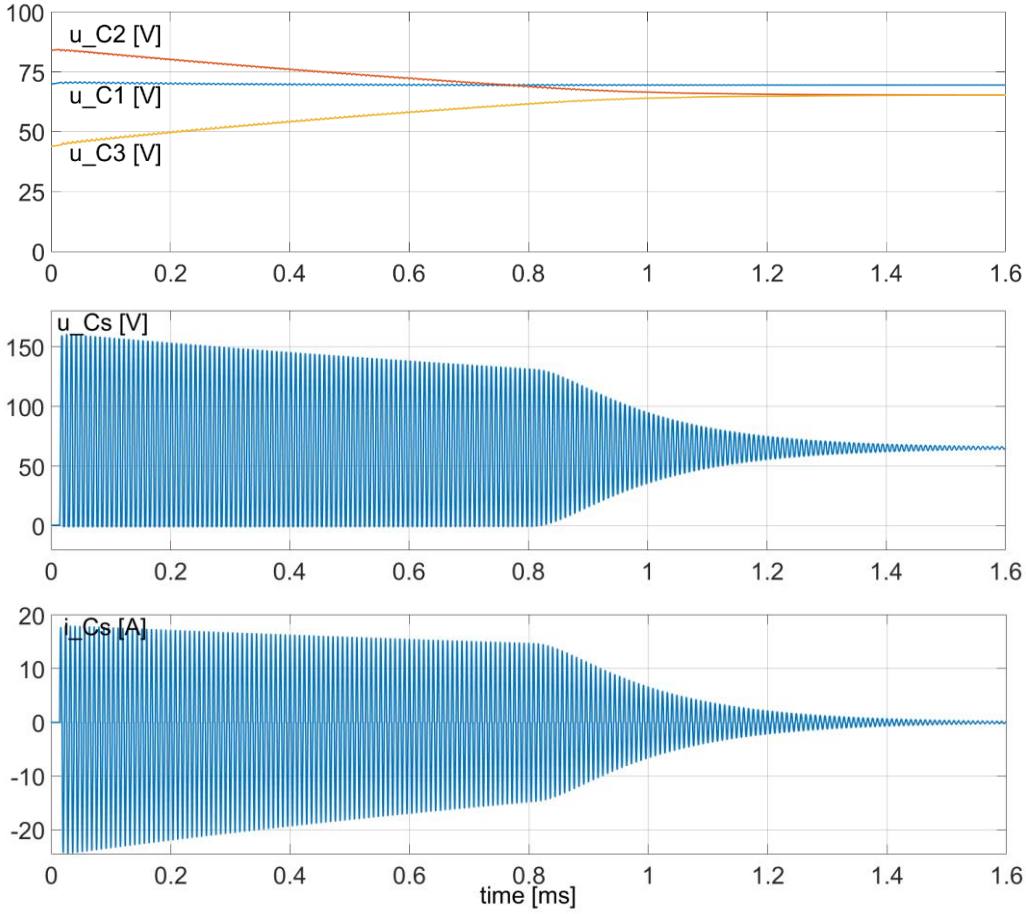


Figure 4.4: Energy transfer between the C_2 - $u(0)$=80[V] and C_3 - $u(0)$=40[V] capacitors in a series-connected branch. DC-link supply voltage 200[V]. Duration of the complete balancing process. Waveforms of the DC-link capacitors, switched capacitor voltage and current.

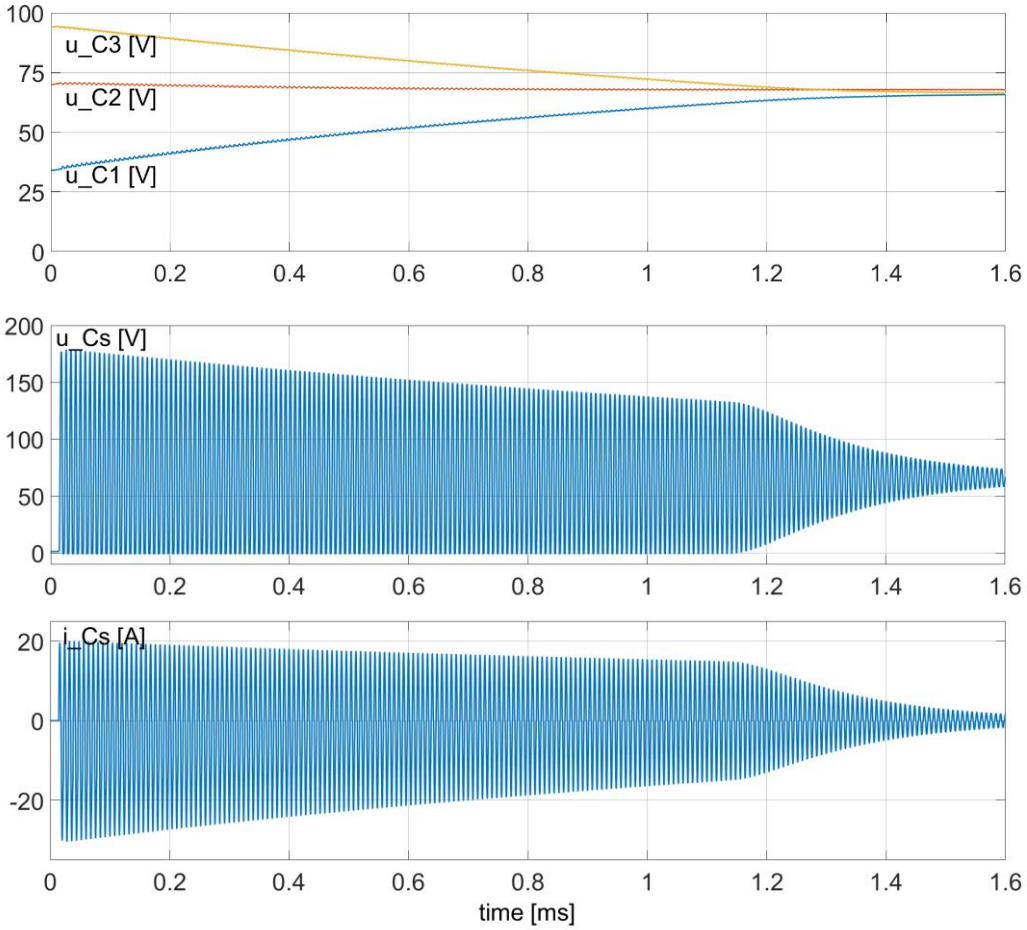


Figure 4.5: Energy transfer between the C_3 - $u(0)$=90[V] and C_1 - $u(0)$=30[V] capacitors in a series-connected branch. DC-link supply voltage 200[V]. Duration of the complete balancing process. Waveforms of the DC-link capacitors, switched capacitor voltage and current.

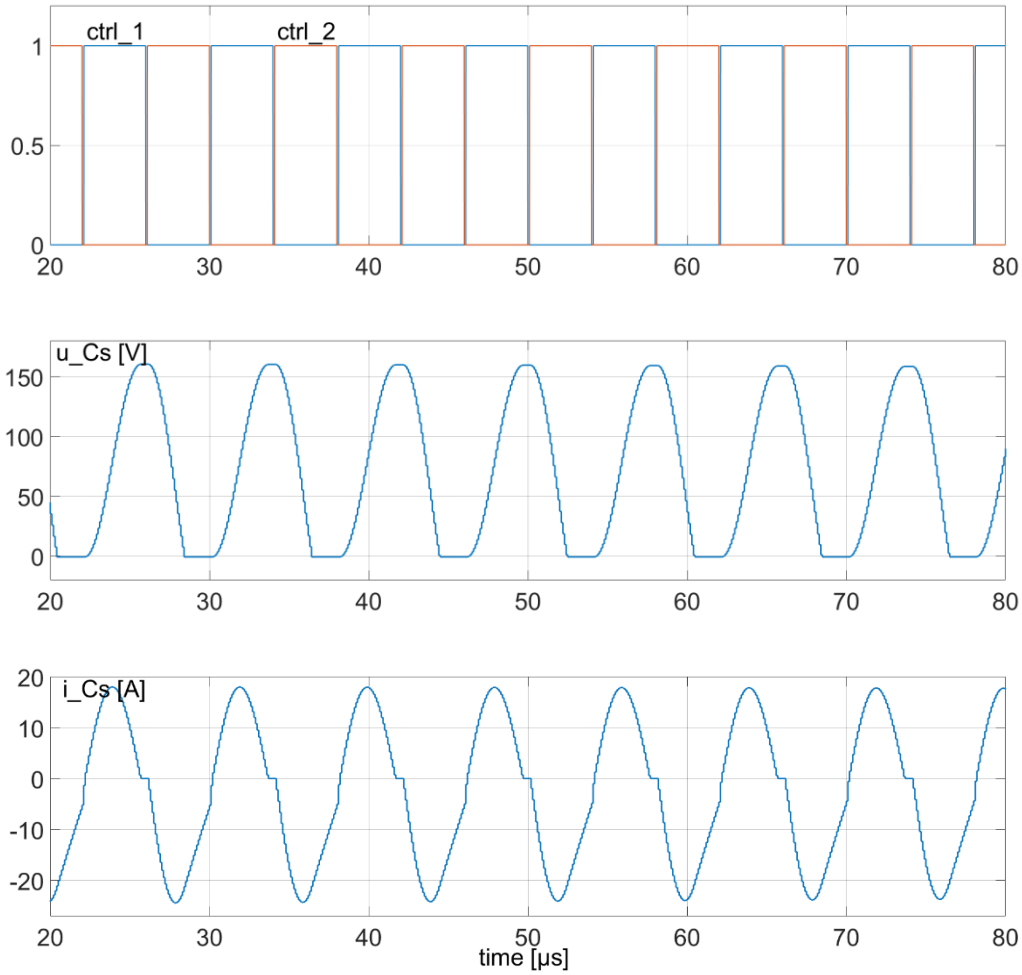


Figure 4.6 Energy transfer between the C_2 and C_3 capacitors in a series-connected branch. Initial voltages: $uC_2(0)$=80[V], $uC_3(0)$=40[V] DC-link supply voltage 200[V]. Duration 20-80[µs]. Waveforms of the control signals, switched capacitor voltage and current. A fragment of the operation with the maximum power limited by the full discharge of the switched capacitor.

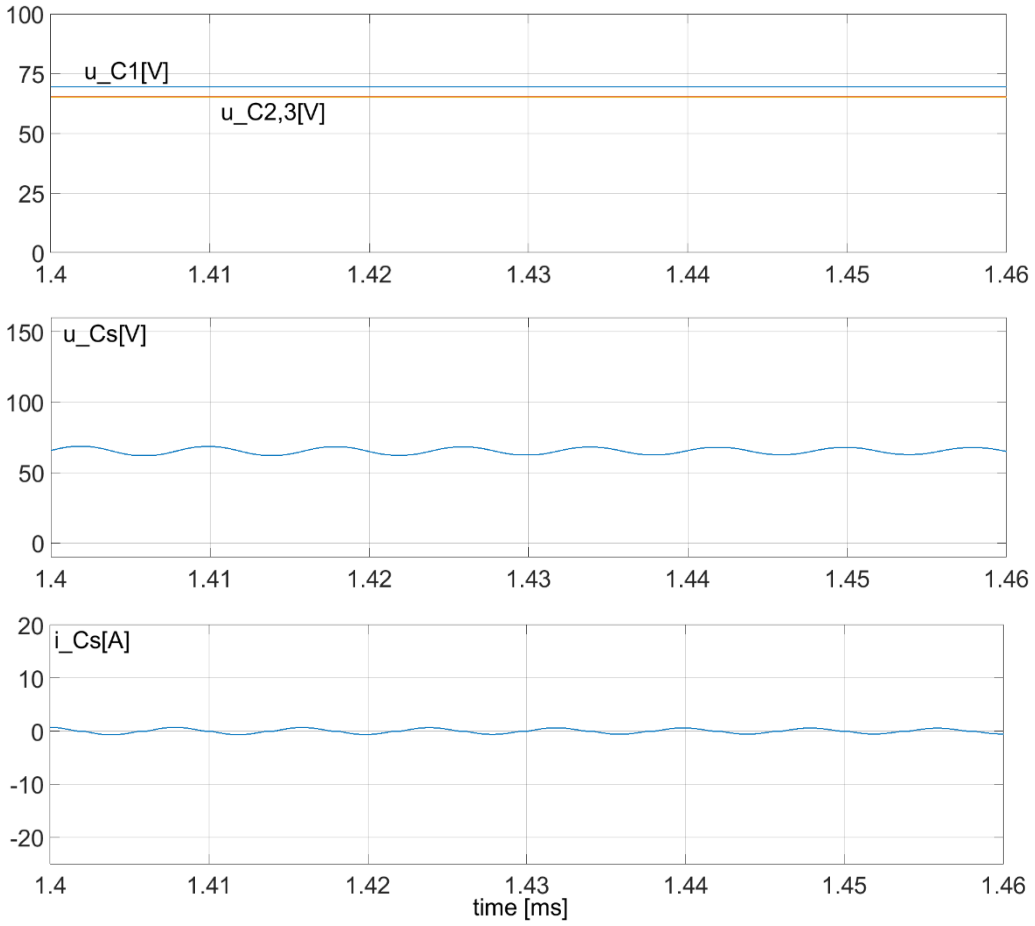
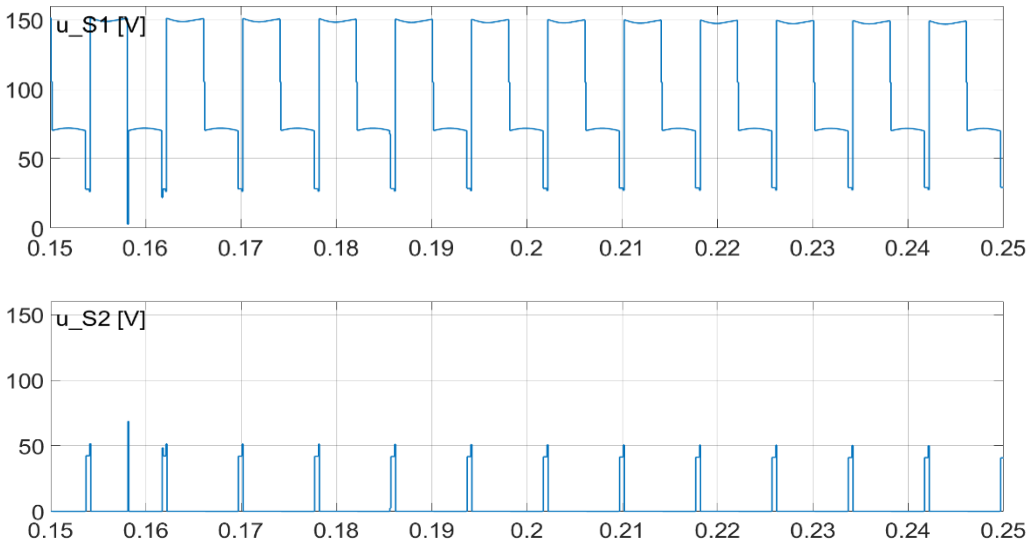


Figure 4.7: Energy transfer between the C_2 - $u(0)$=80[V] and C_3 - $u(0)$=40[V] capacitors in a series-connected branch. DC-link supply voltage 200[V]. Duration 1.4-1.46[ms]. Waveforms of the DC-link capacitors, switched capacitor voltage and current. A fragment of the operation with the voltages balanced – steady state.



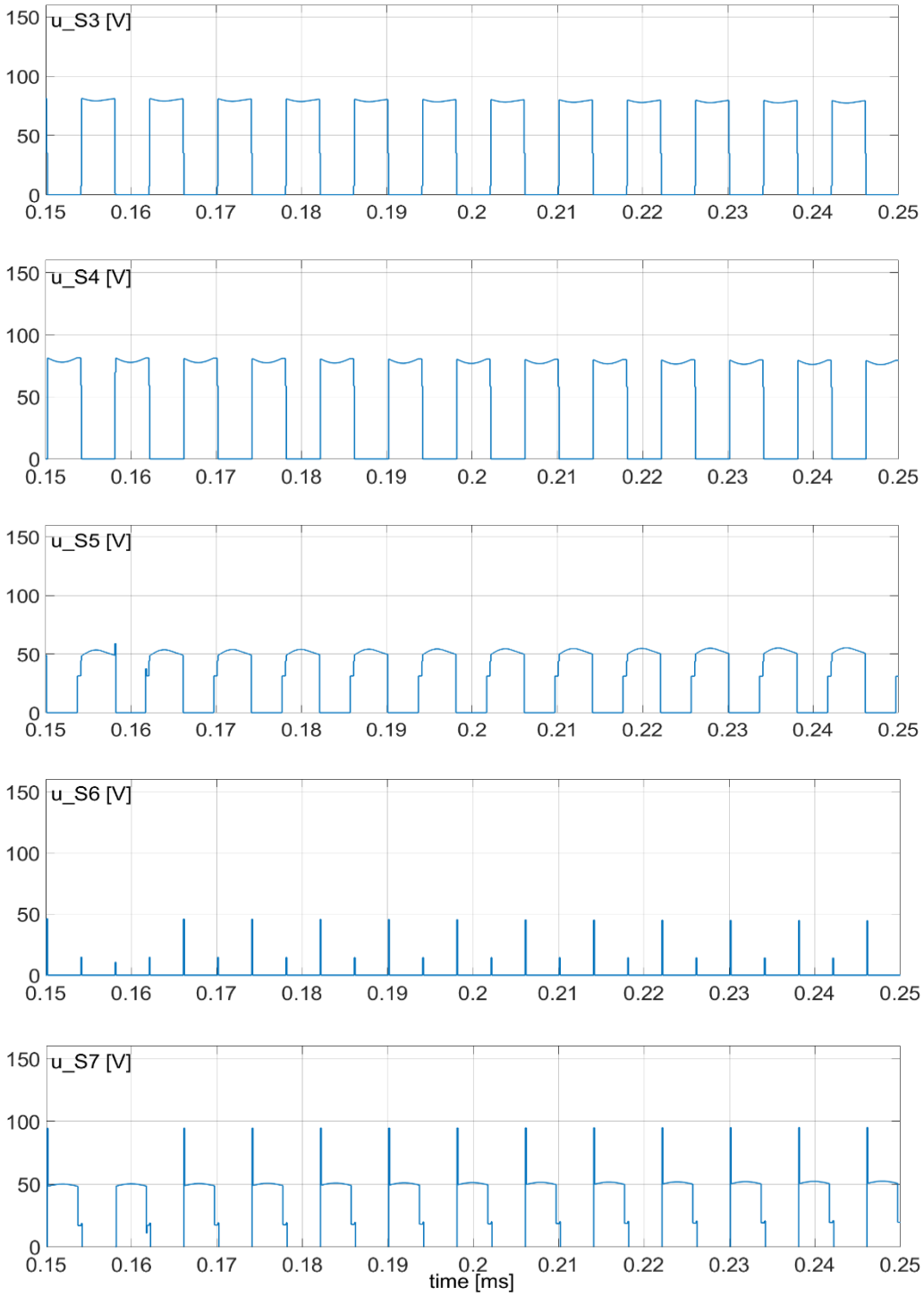


Figure 4.8: Voltage stress on the semiconductors S_1 to S_7. C_2 - $u(0)$=80[V] and the - $u(0)$=40[V] capacitors in a series-connected branch. DC-link supply voltage 200[V]. Duration 0.15-0.25[ms].

Table 4.2: Voltage stress[V] on the transistors for all of the possible operating scenarios. $u_{CD}(0)$=80[V], $u_{CC}(0)$=40[V] , DC-link supply voltage 200[V].

Discharged	C_1		C_2		C_3	
Charged	C_2	C_3	C_1	C_3	C_1	C_2
S_1	103	155	98	155	135	135
S_2	84	84	65	71	65	71
S_3	32	70	48	84	72	65
S_4	65	63	84	84	63	65
S_5	71	65	71	65	84	84
S_6	65	72	84	48	70	32
S_7	135	135	155	98	155	103

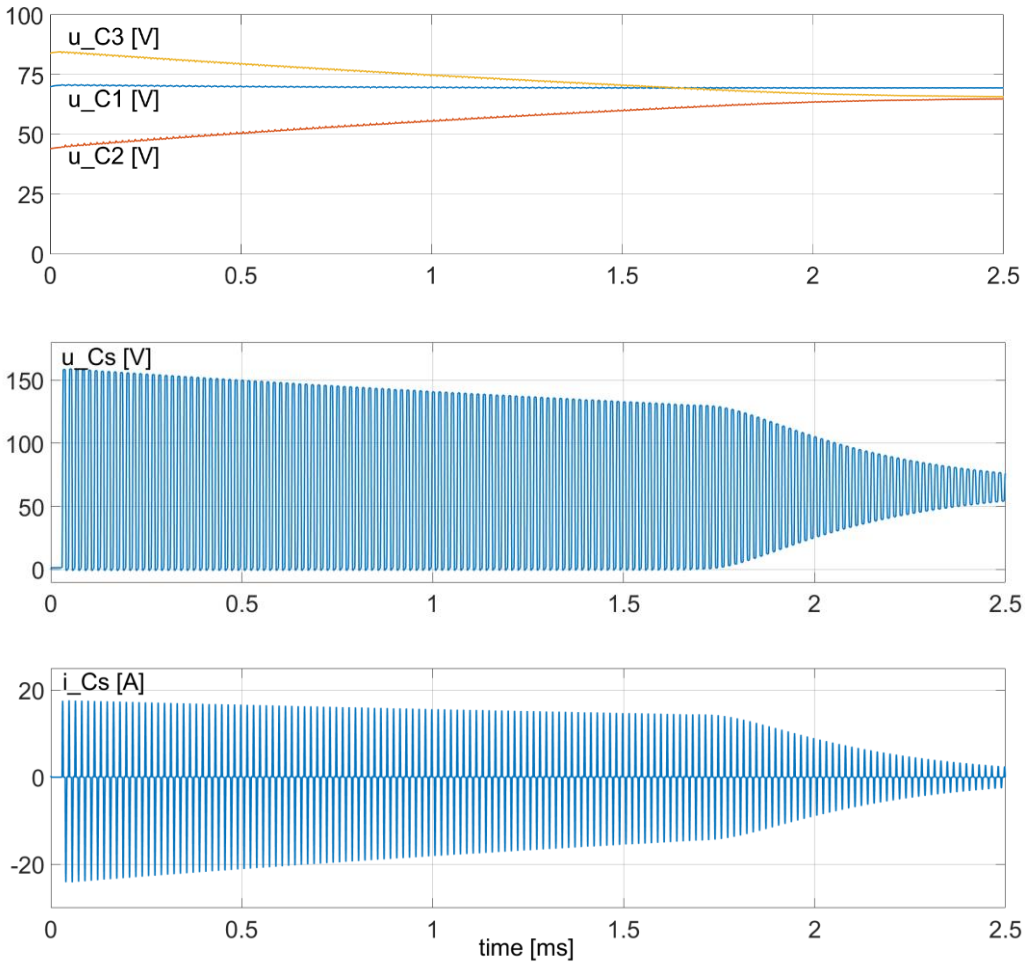


Figure 4.9: Energy transfer between the C_3 - $u(0)$=80[V] and C_2 - $u(0)$=40[V] capacitors in series-connected branch. DC-link supply voltage 200[V]. Switching frequency 60[kHz]. Duration of the complete balancing process. Waveforms of the DC-link capacitors, switched capacitor voltage and current.

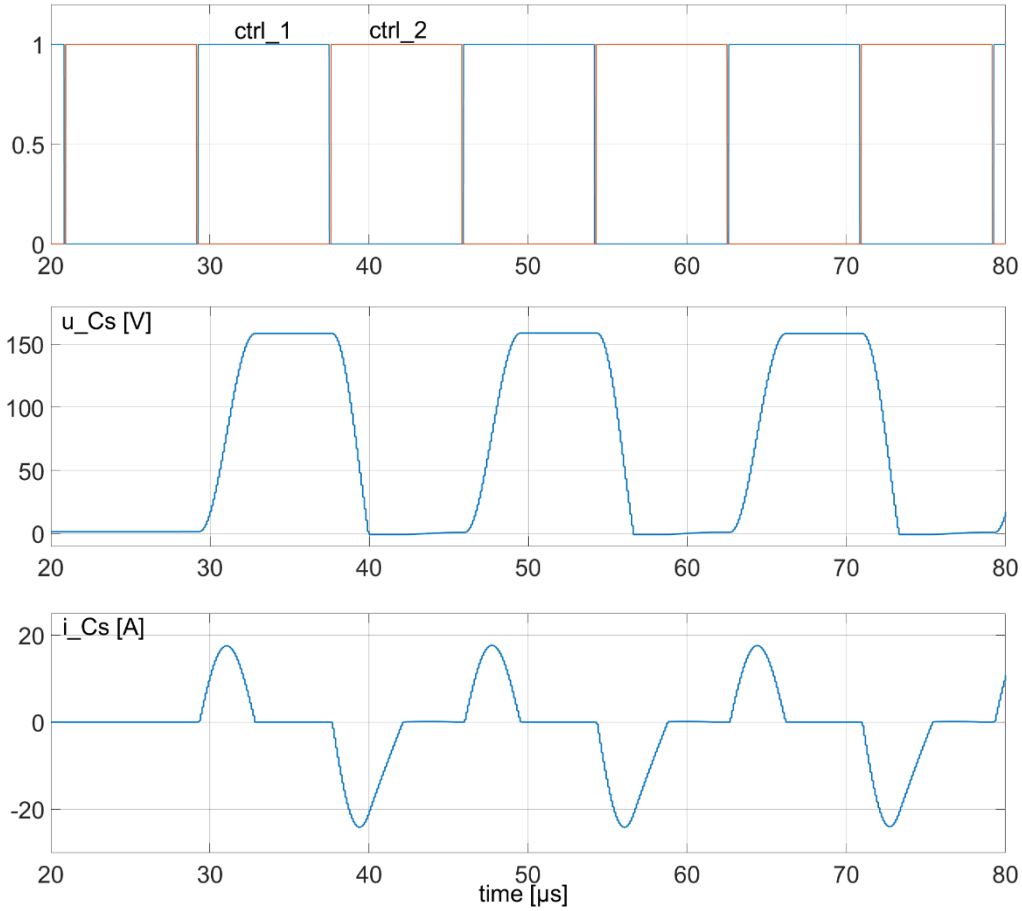


Figure 4.10: Energy transfer between the C_3 - $u(0)$=80[V] and C_2 - $u(0)$=40[V] capacitors in a series-connected branch. DC-link supply voltage 200[V]. Switching frequency 60[kHz]. Duration 60[µs]. Waveforms of the control signals, switched capacitor voltage and current. The fragment of operation with maximum power limited by the full discharge of the switched capacitor.

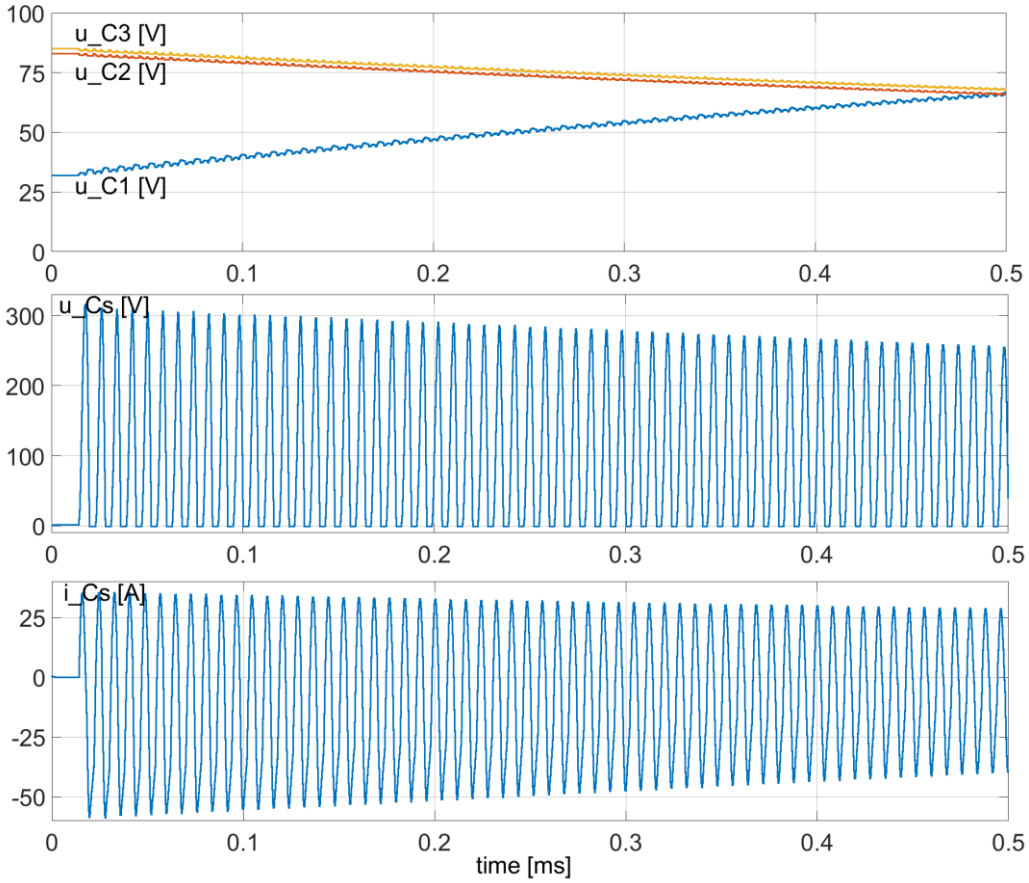


Figure 4.11: The high-rate energy transfer (discharge of two capacitors simultaneously) between the $C_{2,3}$ - $u(0)$=83;85[V], respectively, and C_1 - $u(0)$=32[V] capacitors in a series-connected branch. DC-link supply voltage 200[V]. Duration of the complete balancing process. Waveforms of the DC-link capacitors, switched capacitor voltage and current.

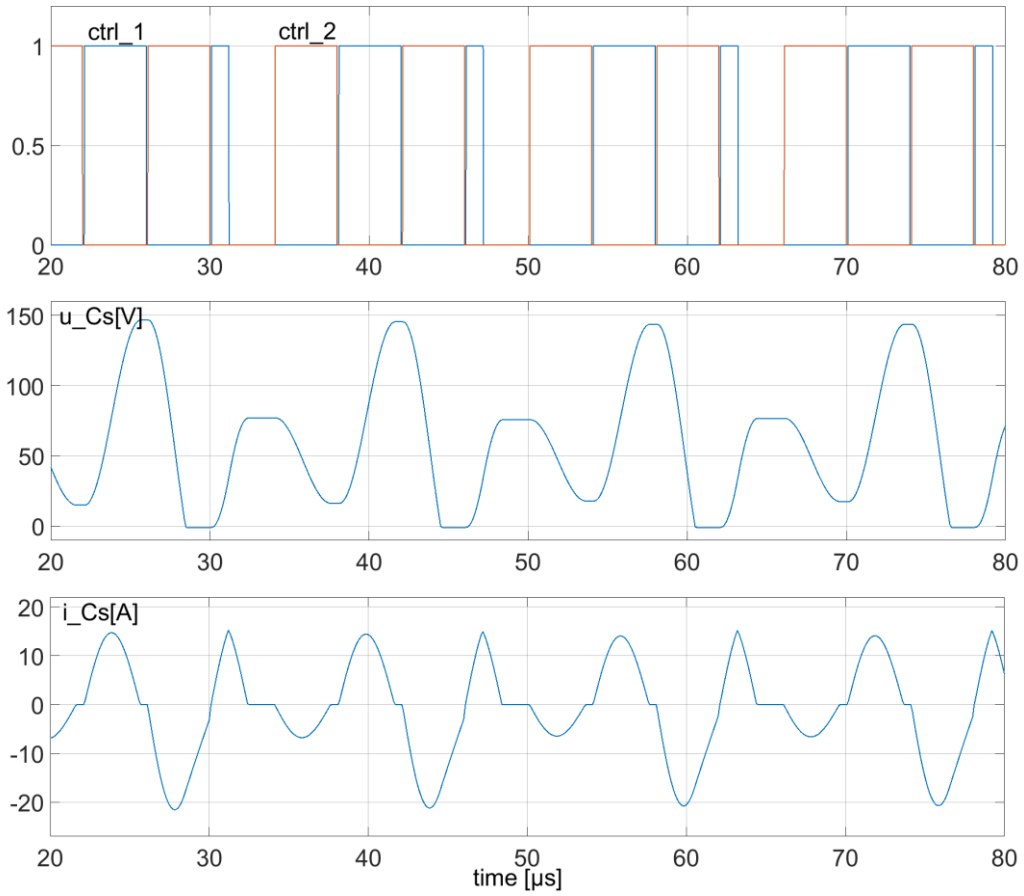


Figure 4.12: The hard switching operation because of the limitation of the switched capacitor charging current I_{CSmax} = 18[A]. Energy transfer between the C_3 - u(0)=80[V] and C_1 - u(0)=40[V] capacitors in a series-connected branch. DC-link supply voltage 200[V]. Duration 20-80[µs].

4.3. Laboratory setup description

The designed printed circuit board (PCB) of the balancer is presented in Figure 4.13, while Figure 4.14 gives the schematic of the experimental setup. Figure 4.15 illustrates the setup during the investigation. The details of the experimental setup parameters are presented in Table 4.3.

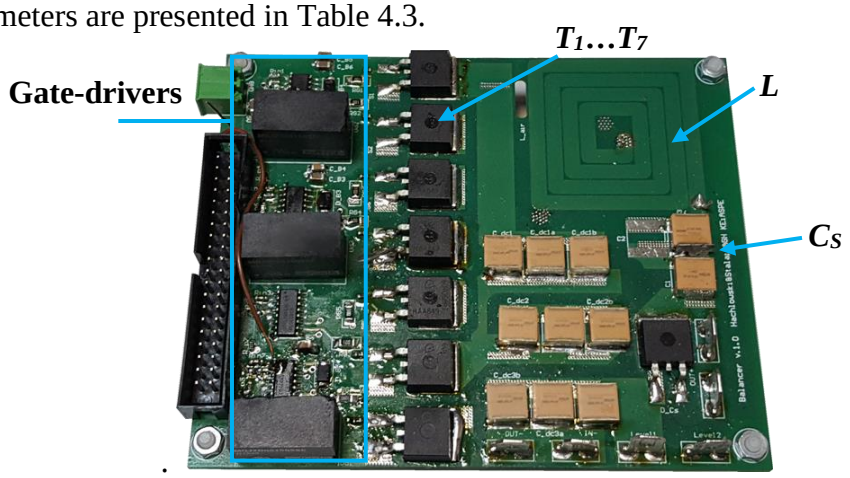


Figure 4.13: The SCABC printed circuit board.

Table 4.3: Parameters of the proposed experimental balancer and test conditions.

Switched capacitor	C_S	250[nF]
Inductance	L	4.9 [µH]
DC-link capacitors	C_1,C_2,C_3	250 [µF]
DC source	U_{in}	200 [V]
Dead-time	t_d	100 [ns]
Resonant frequency	f_{RES}	143 [kHz]
Switching frequency	f_{SW}	125 [kHz]; 60 [kHz]
Transistors	-	IPB60R060P7ATMA1
FPGA controller	-	Cyclone III
PCB size	-	112x93 [mm]

The SCABC that was built was based on a four-layer PCB, which when equipped with TO-263 package semiconductors acts like a heatsink. The design uses a planar, coreless choke. Such an approach ensures a linear, virtually non-saturable inductance, which is advantageous in the initial investigation of a topology. The resonant frequency was assumed to be 150kHz and the switched capacitor was selected to meet the conditions with the achieved air-choke inductance.

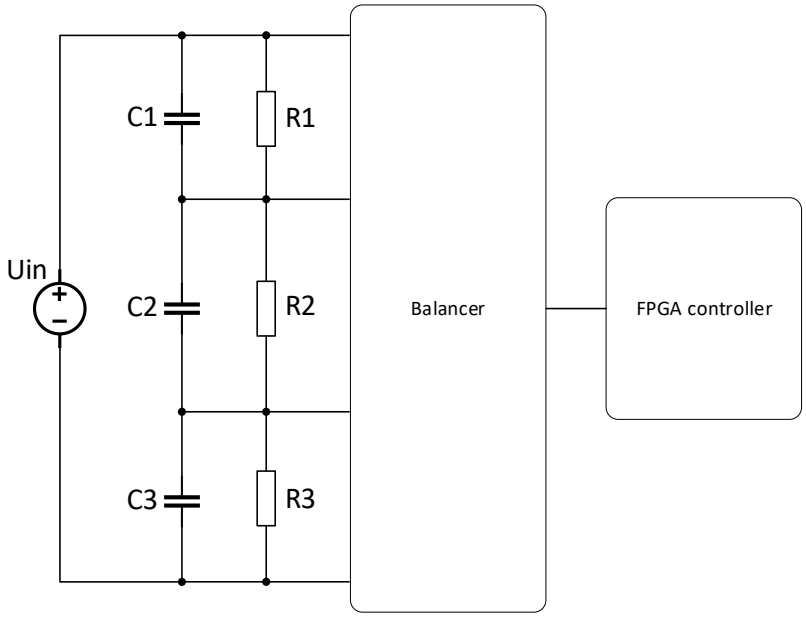


Figure 4.14: The laboratory setup schematic for the SCABC tests.

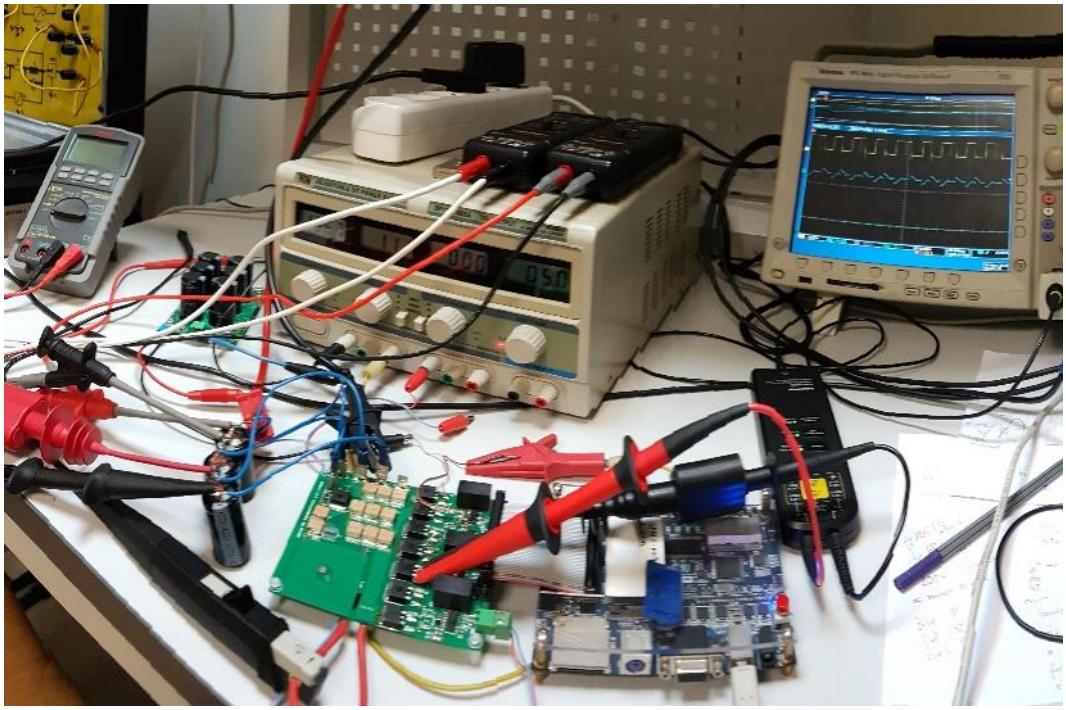


Figure 4.15: The laboratory setup with the SCABC during the investigation.

To drive the transistor gates, the concept of an efficient and low-cost driver system was introduced and is presented in Figure 4.16. It assumed the use of three supply voltage sources. To achieve this, two isolated DC-DC converters were required. The following transistor pairs could be derived, in which the high-side switches could be fed with a bootstrap-type supply: S_2 with S_1, S_6 with S_4', and S_7 with S_5. The switch S_3 was supplied from the same source as S_2 because they have a common source potential. In this way, the gate-driving system for seven transistors could be achieved using two isolated DC-DC power supplies, three dual bootstrap drivers and one single-channel driver. Because switches S_4 and S_6 had to be turned on simultaneously for charging capacitor C_3 – Table 3.1 – the driver chip that is used must allow a simultaneous turn-on state for the low- and high-side switches. To maintain the power supply for driving the high-side switches, additional control pulses had to be introduced for the low-side switches. Such a short turn-on condition would provide the charging of the bootstrap capacitors.

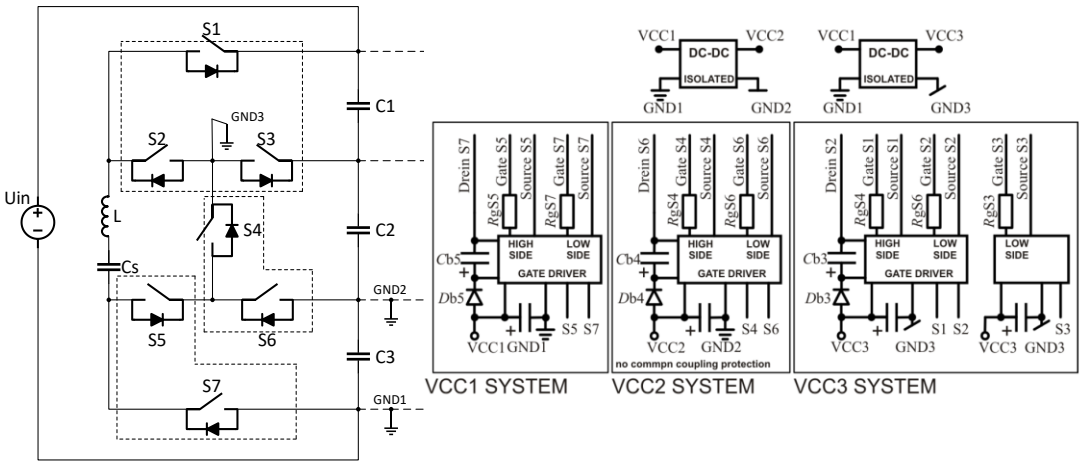


Figure 4.16: The concept of the gate driver system for the SCABC [P.2].

Table 4.4: Active semiconductors for the bootstrap control

-	The charging stage s_I		
Capacitor	C_1	C_2	C_3
Active switch	S_3, S_4, S_5	S_2, S_5	S_2, S_4, S_6
Bootstrap supplied	S_4, S_5	S_5	S_4
Bootstrap activator	S_6, S_7	S_7	S_6
-	The discharging stage s_{II}		
Capacitor	C_1	C_2	C_3
Active switch	S_1	S_3, S_6	S_7
Needs bootstrap	S_1	-	-
Bootstrap activator	S_2	-	-

In order to cause an imbalance in the series-connected capacitors, a resistive voltage divider was connected in parallel. By adjusting the ratio of the resistances, the correct voltage imbalance was set. With the voltage set, the balancer was turned on by activating the gate pulses.

4.4. Experimental results

Three test scenarios were performed and are presented in this section. The first scenario covered the energy exchange between capacitors C_1 and C_2, where the relationship of the voltage across them was $U_{C1}<U_{C2}$. The test was performed for two switching frequencies: 125[kHz] – slightly below the resonant frequency – and 60[kHz]. The current and voltage of the switched capacitor were recorded, as well as the voltages of the balanced capacitors` in a series-connected branch. The results are presented in Figure 4.17 and Figure 4.18. The voltage stresses of the active semiconductors were investigated and are illustrated in Figure 4.19. The second test

scenario revealed a high-rate energy exchange, in which the energy was drained from C_1 and C_2 simultaneously and fed into capacitor C_3. The results were registered and are presented in Figure 4.20: the voltage and current of C_S, and the voltages of the series-connected capacitors. The results presented in Figure 4.21 and Figure 4.22 were recorded for the experiment in which the bootstrap-based supply of the gate drivers was introduced. The first figure – 4.21 – presents the gate signal waveforms, where the supply of the S_5 transistor was achieved in the bootstrap circuit with the S_7 transistor as a low-side device. To enable the S_5 bootstrap capacitor to charge, S_7 was turned-on during the dead-time between switching pulses that were used in the required switching pattern. The second figure – 4.22 – shows the correct operation of the balancer when the bootstrap method for the S_5 gate driver isolated supply was used.

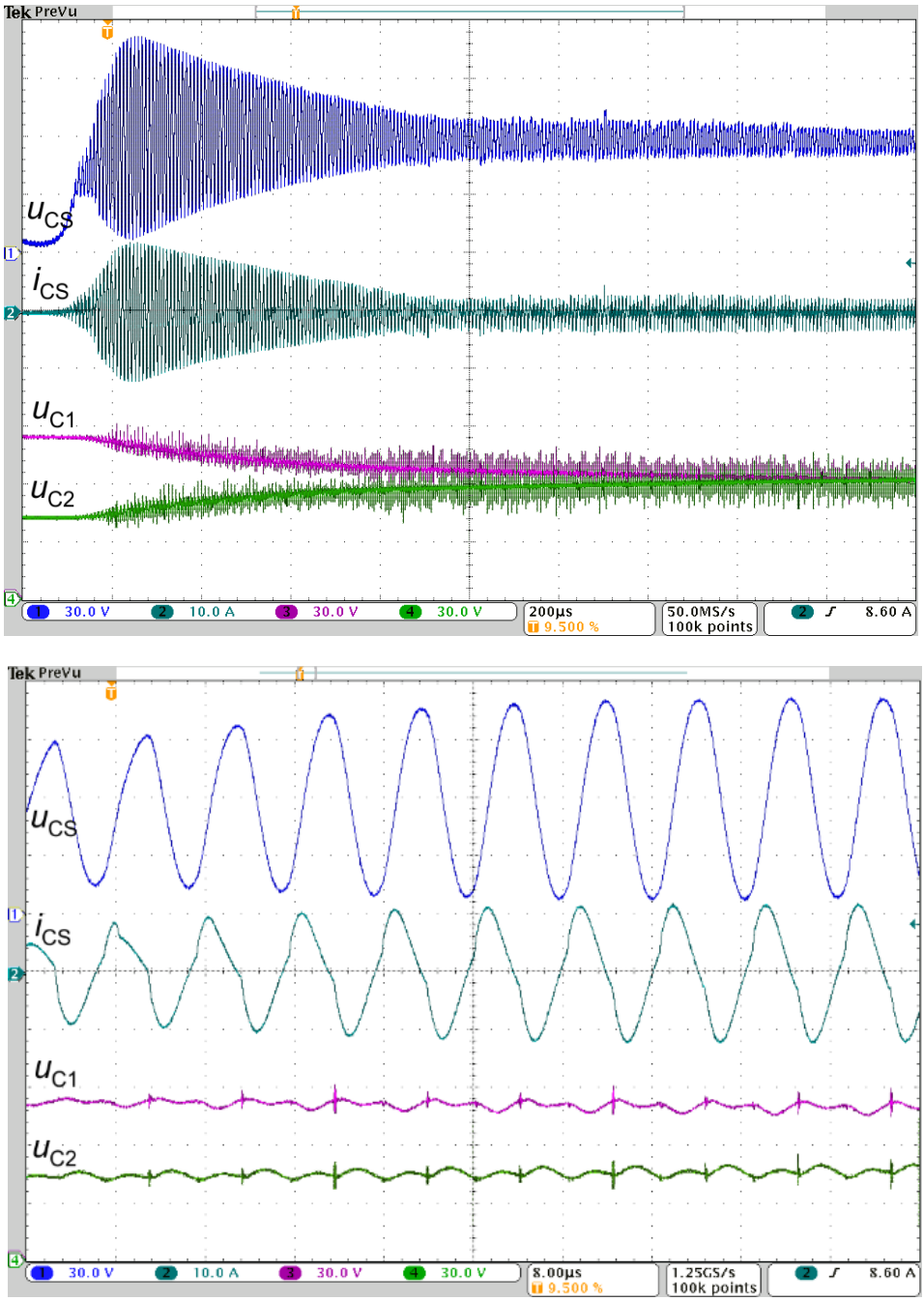


Figure 4.17: Experimental waveforms of the test scenario: $u_{C1}(0)$=40[V], $u_{C2}(0)$=80[V] (50% of the imbalance), switching frequency f_{SW} = 125[kHz]. Energy transfer from C_1 to C_2. Waveforms of the voltage on the C_S, its current and voltages on the series-connected capacitors [P.2].

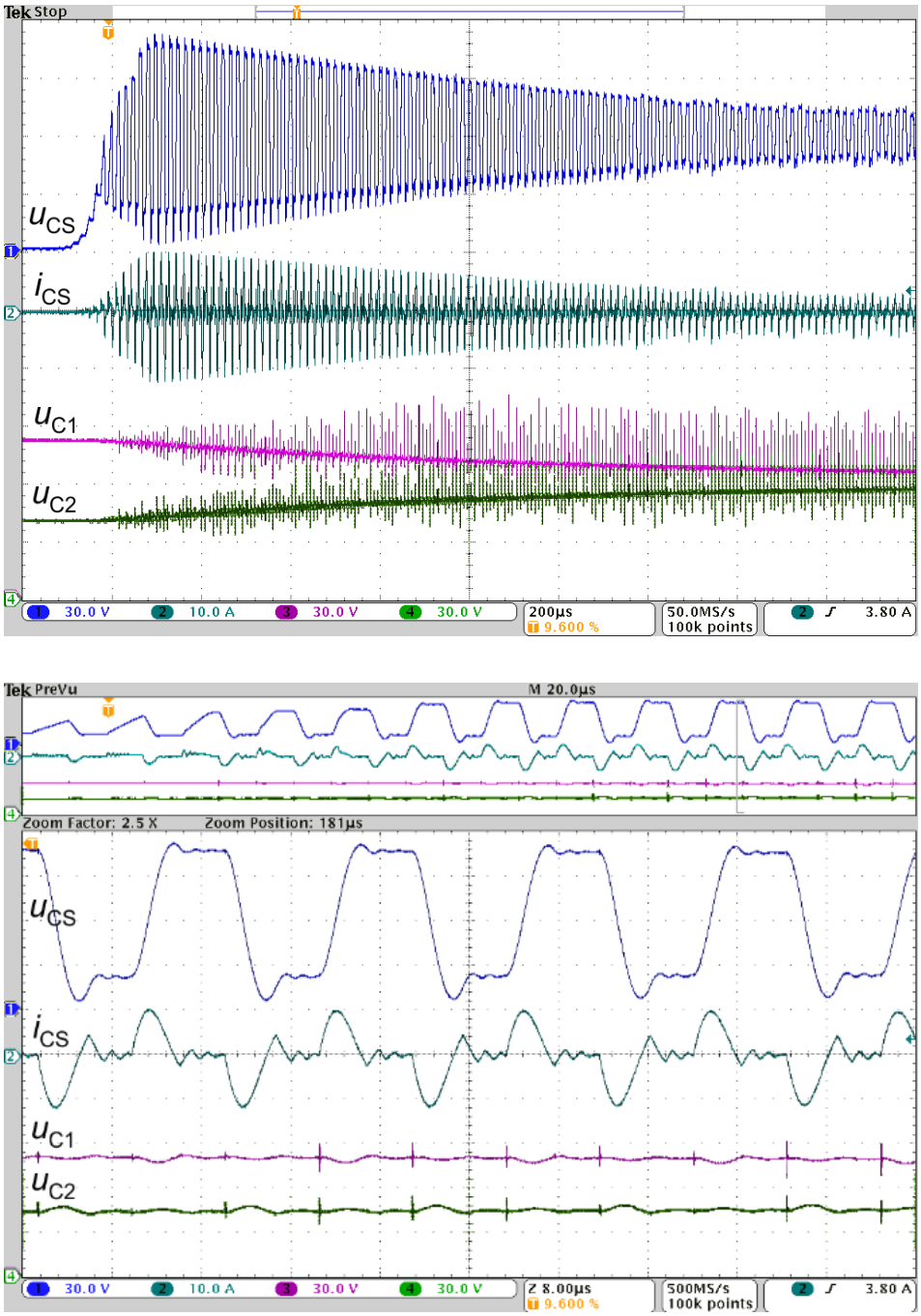


Figure 4.18: Experimental waveforms of the test scenario: $u_{C1}(0)$=40[V], $u_{C2}(0)$=80[V] (50% of the imbalance), switching frequency f_{SW}=60[kHz]. Energy transfer from C_1 to C_2. Waveforms of the voltage on C_S, its current and voltages on the series-connected capacitors [P.2].

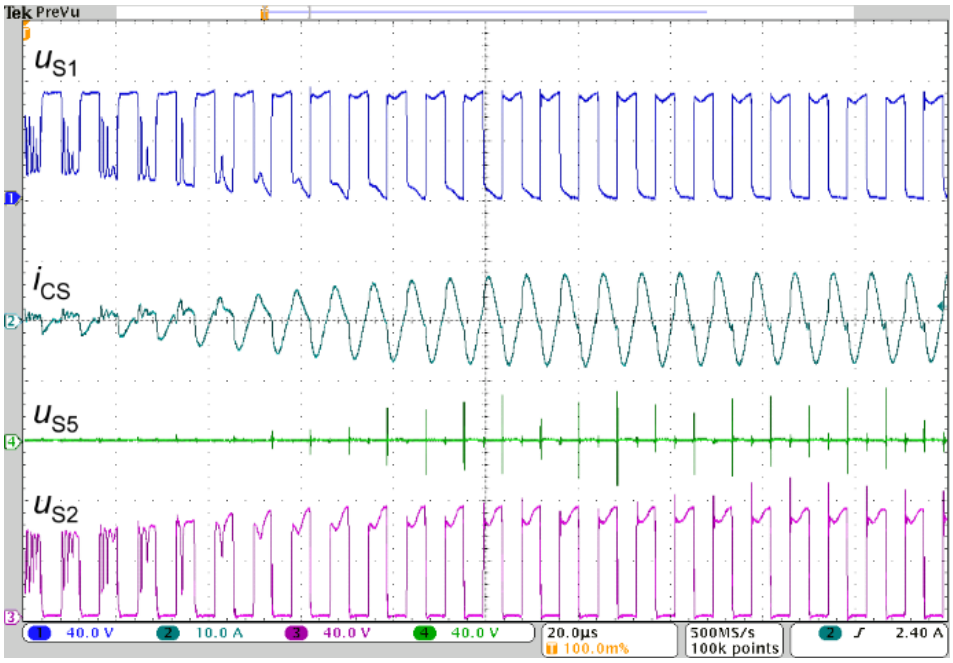


Figure 4.19: Experimental waveforms of the test scenario: $u_{C1}(0)$=40[V], $u_{C2}(0)$=80[V] (50% of the imbalance), switching frequency f_{SW}=125[kHz]. Energy transfer from C_1 to C_2. Waveforms of transistor switch S_1, C_S current, transistor switch S_2, transistor switch S_5 [P.2].

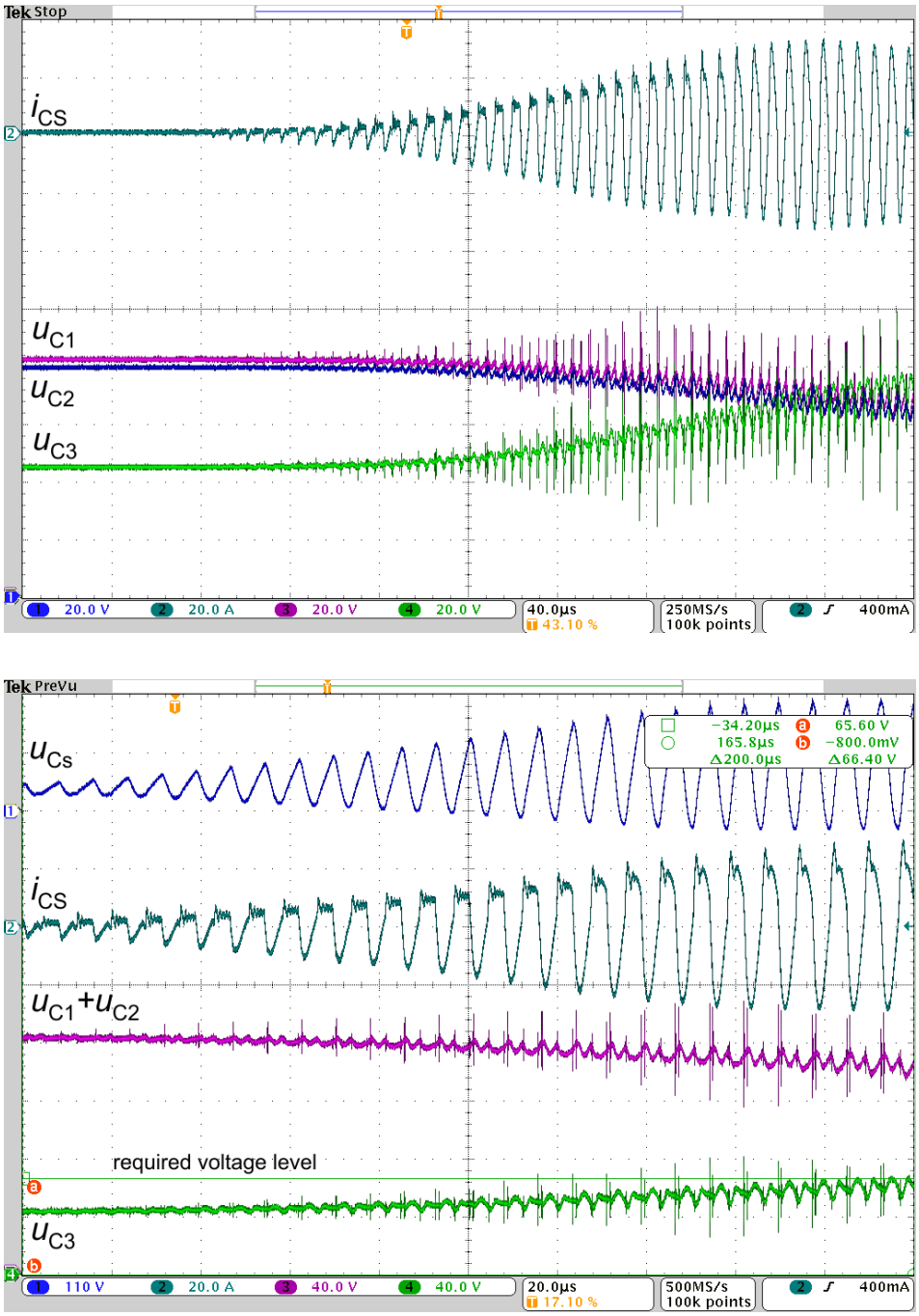


Figure 4.20: Experimental waveforms of the test scenario: $u_{C1}(0)$=80[V], $u_{C2}(0)$=80[V], $u_{C3}(0)$=40[V] (50% of the imbalance), switching frequency f_{SW}=125 [kHz]. High-rate energy transfer from C_1 and C_2 to C_3. Waveforms of the voltage on C_S, C_S current, and voltages on the series-connected capacitors [P.2].

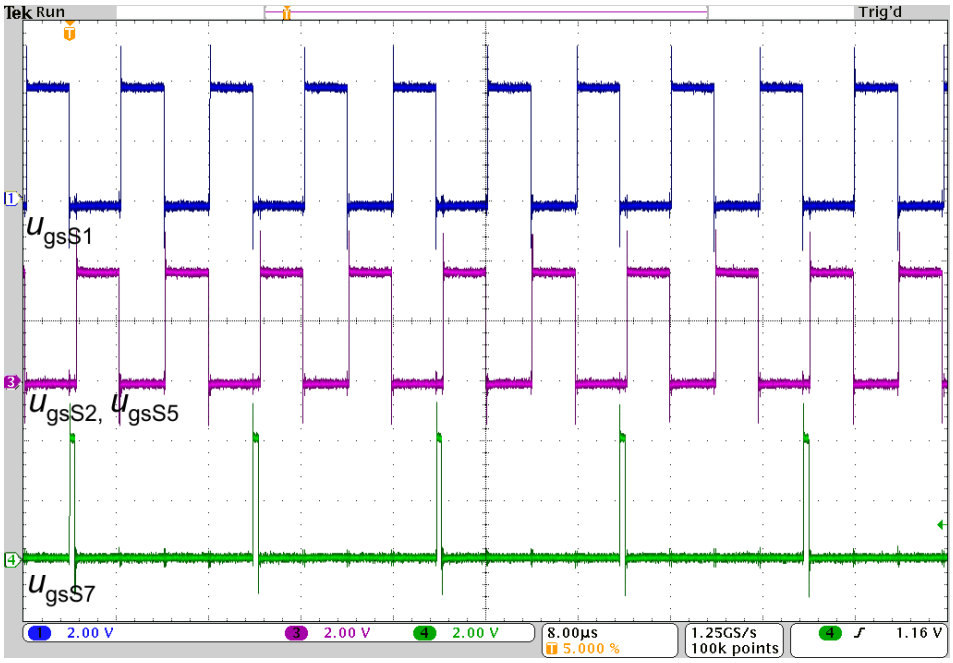


Figure 4.21: Experimental waveforms of the test scenario: $u_{C1}(0)$=40[V], $u_{C2}(0)$=80[V] (50% of the imbalance), switching frequency f_{SW}=125[kHz]. Energy transfer from C_1 to C_2. Control strategy covering the bootstrap supply. Waveforms of the gate signals for transistors S_1, S_2 and S_5, S_7 (charging bootstrap capacitance) [P.2].

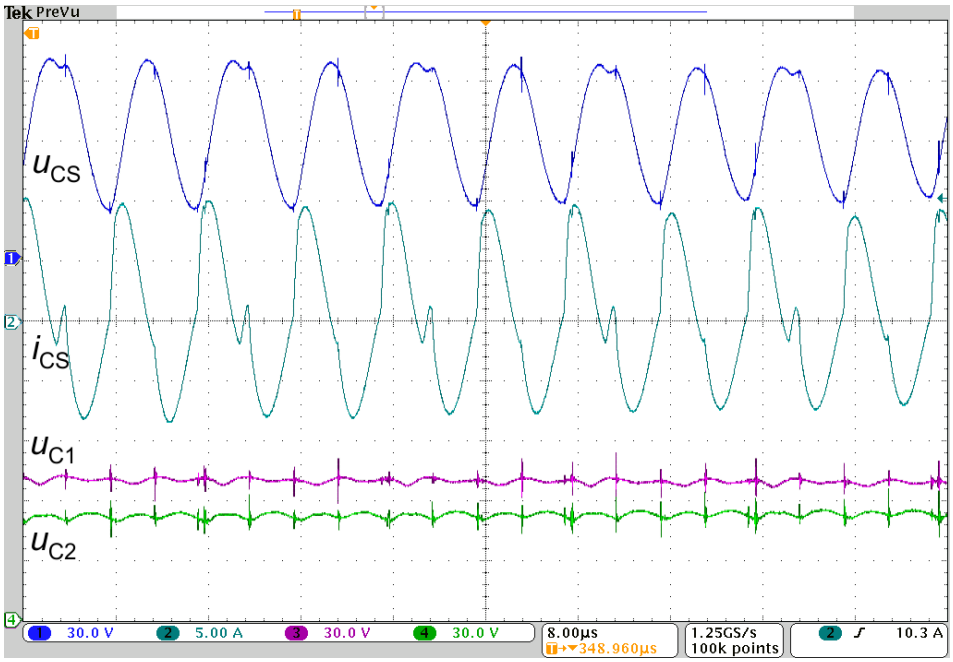


Figure 4.22: Experimental waveforms of the test scenario: $u_{C1}(0)$=40[V], $u_{C2}(0)$=80[V] (50% of the imbalance), switching frequency f_{SW}=125[kHz]. Energy transfer from C_1 to C_2. Control strategy covering the bootstrap supply. Waveforms of the voltage on C_S, C_S current, and voltages on the series-connected capacitors [P.2].

4.5. Conclusions

The proposed balancer topology was proven to operate as was expected. The energy was transferred between the selected capacitors in the balanced series bank through the balancing resonant branch, which equalised their voltages. The portion of energy that was transferred, and thus the process dynamics could be adjusted by design, so by appropriately tuning of the resonant LC_S branch, or by changing the switching frequency of the circuit. Additionally, a high-rate transfer was achieved by discharging the two capacitors of the bank simultaneously. From these results, it can be seen that the dynamics of the voltage change on the capacitors was significantly higher when a single capacitor was charged from the two remaining ones.

The simplification of the balancer`s gate-driver circuitry that was introduced operated correctly. The bootstrapping method helped to reduce the area of the printed circuit board and reduced the complexity of the design and the number of hardware components that were required. However, this was offset by the insignificant complication of the switching pattern and an increased pause between the energy exchange cycles.

The voltage stress on the active switches were maintained at a reasonable level during the operation and reached up to half of the supplied DC voltage at their peaks. This fact can be favourable from a practical application cost point of view as transistors with a lower voltage rating can be used when compared to the operational DC source voltage. The current and voltage magnitudes on C_S were dependent on the resonant branch parameters and for the presented balancer, respectively, reached:

- 12[A] and 110[V] for test scenario: $u_{C1}(0)$=40[V], $u_{C2}(0)$=80[V] (50% of the imbalance), switching frequency f_{SW}=125[kHz]. Energy transfer from C_1 to C_2
- 30[A] and 220[V] for test scenario: $u_{C1}(0)$=80[V], $u_{C2}(0)$=80[V], $u_{C3}(0)$=40[V] (50% of the imbalance), switching frequency f_{SW}=125[kHz]. High-rate energy transfer from C_1 and C_2 to C_3

The experimental test scenario with a low operating frequency (Figure 4.18) revealed a disadvantage of the proposed balancer topology. Once the voltage of the switched capacitor was set, during both the charging and discharging stages,

the oscillatory high frequency current continued to flow. These oscillations are marked in Figure 4.23

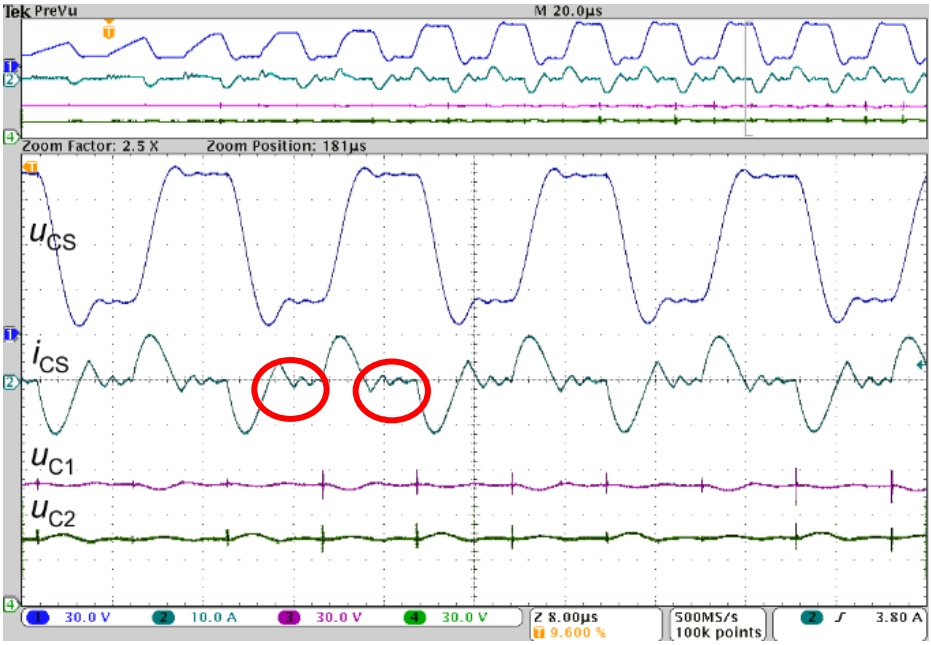


Figure 4.23: Parasitic oscillations in the resonant branch.

The closed path for this current is presented in Figure 4.24. This current is assumed to recharge the junction capacitances of the transistors in the loop and was damped by the parasitic resistances and therefore affected the efficiency of the balancing process negatively.

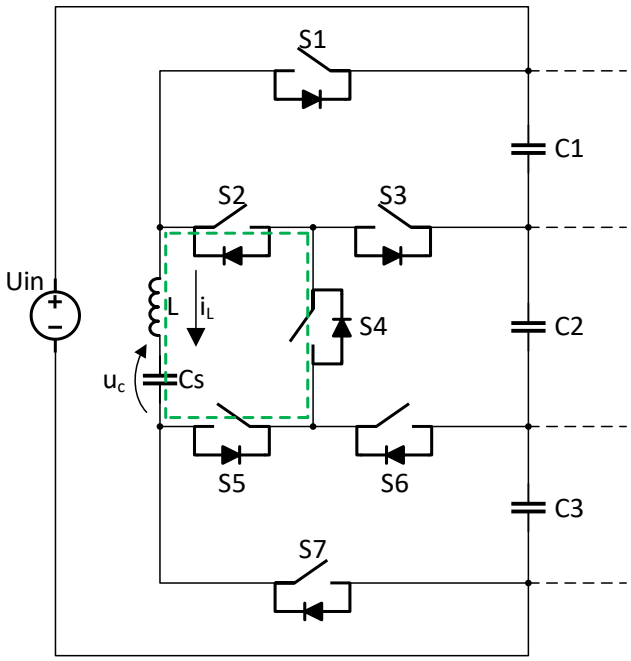


Figure 4.24: Closed path for the high-frequency oscillatory current in negative direction.

The problem could be eliminated by a precisely matching the switching frequency to the oscillation of the current in the circuit. However, because the parameters of the components can drift due to multiple reasons, such a solution would not be adequate. What is more, it would also make it impossible to operate the balancer with low frequency to equalize the voltage with a low dynamics. To resolve this issue, an updated topology is proposed in Figure 4.25. The resonant branch that is formed by the switched capacitor and inductance is now split. The inductor was moved outside of the transistor array, and in order to form an oscillatory LC_S branch for every possible operation scenario, two chokes were used. Affected by this will be the operation modes in which the energy is drawn or fed into the C_2 capacitor in the series connected branch as the inductance of the resonant circuit will be double compared to the other modes. This will require adjusting the duty cycle of the two complementary control signals as the two resonant frequencies and thus the duration of the charge and discharge will be unequal. This matter will be discussed in detail in Section 5.3.1.

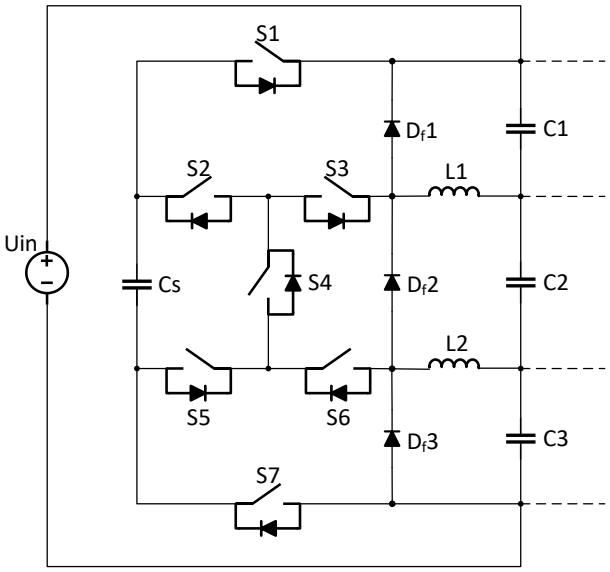


Figure 4.25 Upgraded topology of the Switched Capacitor Active Balancing Converter.

With the three freewheeling diodes ($D_{f1}…D_{f3}$) that were introduced in the updated topology to avoid breaking the inductors' current, an additional current path was provided, so the parasitic oscillatory current was able to flow through the series-connected bank capacitors and charge them. The energy loss was minimised. All further investigations of the SCABC were performed using the updated circuit topology.

5. Switched Capacitor Active Balancing Converter as an input stage of a Multilevel, Neutral-Point-Clamped Inverter

This chapter presents the proposed balancer circuit as a front converter for a two-leg, four-level neutral-point-clamped (NPC), single-phase inverter. A few configurations are possible for this type of tandem. In the first one, a DC-link that is built with three series-connected capacitors is supplied from a DC source, which creates a capacitive voltage divider for the NPC inverter. An SCABC operates as the DC-link`s voltage conditioner and balances the voltages. Although the amount of power that is converted by the balancer is not significant, the control algorithm is complex. Therefore, this study focused on implementing a control logic and simulation of the converter connected to an NPC inverter. The second case, in which the DC source supplies only one middle capacitor in the series-connected branch was also investigated. With this configuration, the SCABC not only provides the DC-link balance, but also boosts the supply voltage to supply the NPC inverter three-fold. The setup was investigated in simulations as well as using the developed experimental setup.

5.1. The problem of a DC-link voltage imbalance in a two-leg, four-level, single-phase NPC inverter with a PD-PWM modulation

As was emphasised in Chapter 1.3, multilevel NPC inverters suffer from a DC-link voltage imbalance, which is an obstacle for the correct operation of the device. To understand the problem in detail for a seven-level NPC inverter that is supplied by the three series-connected capacitors that form the DC-link, a simulation model was developed. This model is presented in Figure 5.1. A simulated configuration of the supplies for the NPC inverter is presented in Figure 5.2 and the principle of its operation is presented *via* waveforms in Figure 5.3. The inverter was supplied with a 400[V] DC source and generated AC power of 1[kW].

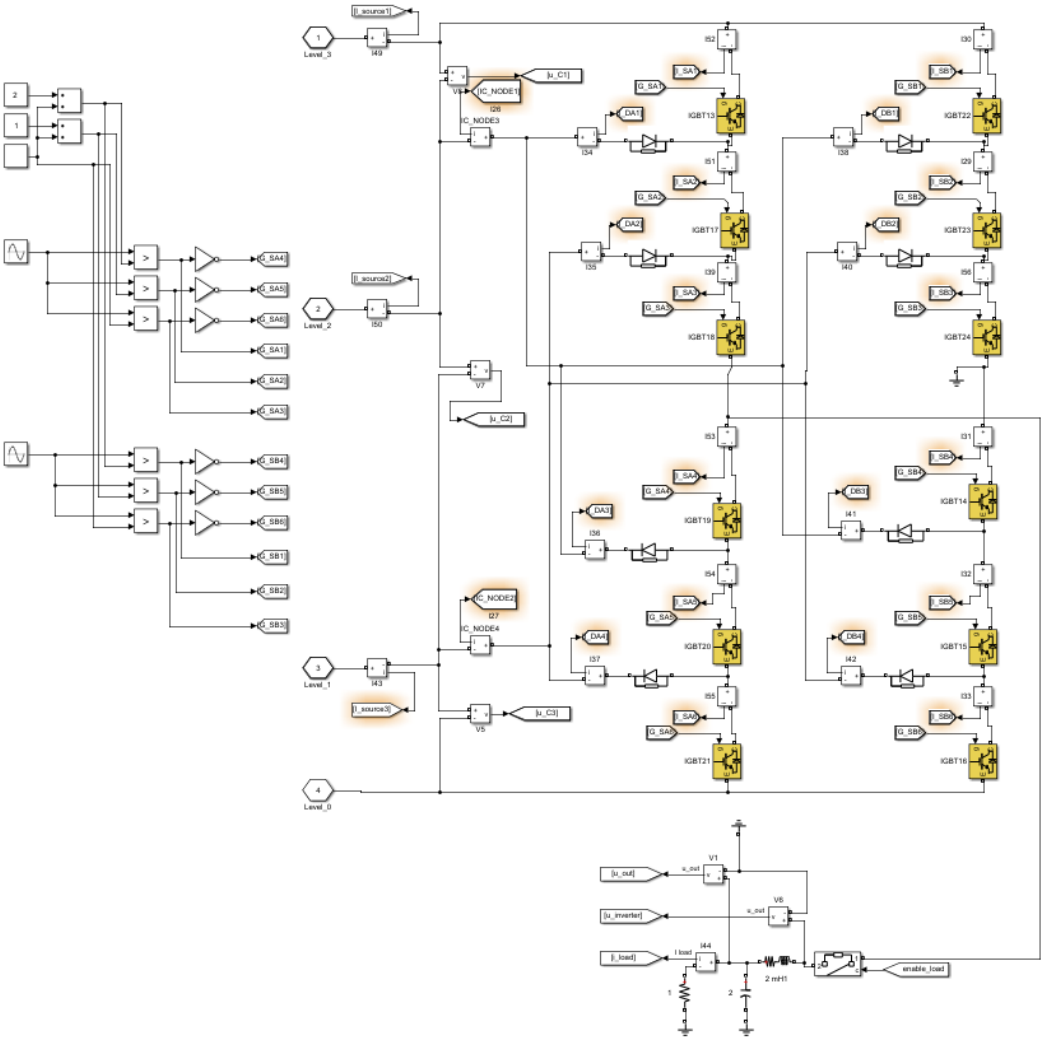


Figure 5.1: Simulink® model of a seven-level NPC inverter with PD-PWM control.

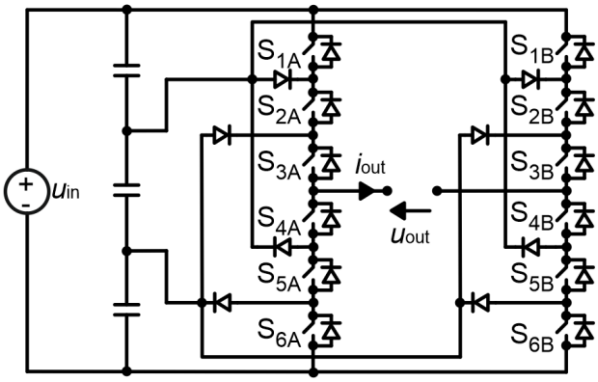


Figure 5.2: The simulation circuit of the inverter with the DC-link fully supplied by the DC source.

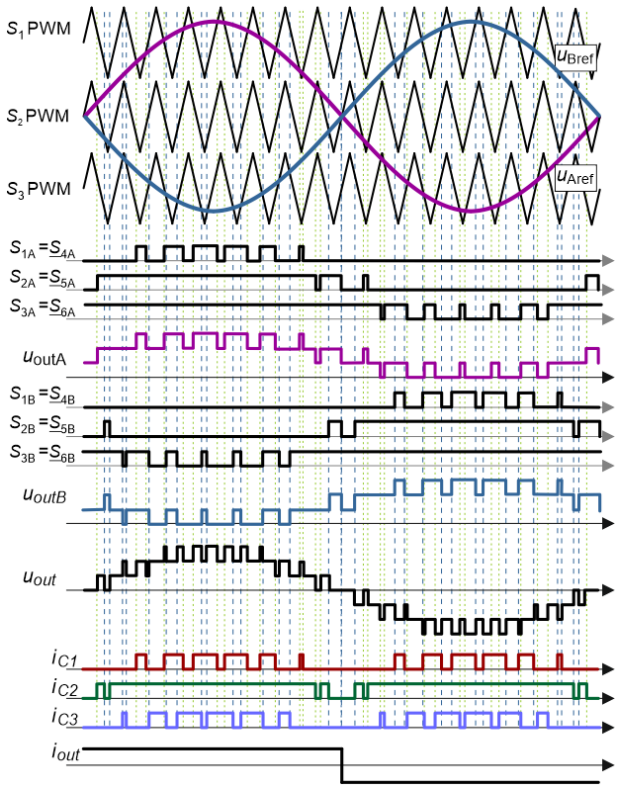


Figure 5.3: The principle of the operation of the seven-level NPC inverter [P.3].

The simulation results showed that the energy that was drained from each of the DC-link capacitors was not equal and caused a voltage imbalance the capacitors. Figure 5.4 presents the NPC`s output current waveforms and the currents that were drained from each of the capacitors. In Figure 5.5, the voltage for each capacitor of the DC-link is presented as well as the output voltage of the NPC inverter.

The study conducted showed that to operate correctly, the NPC seven-level inverter with the PD-PWM modulation required an auxiliary balancing circuit to condition the DC-link voltages. When it operated without them, the output waveforms of the inverter were distorted.

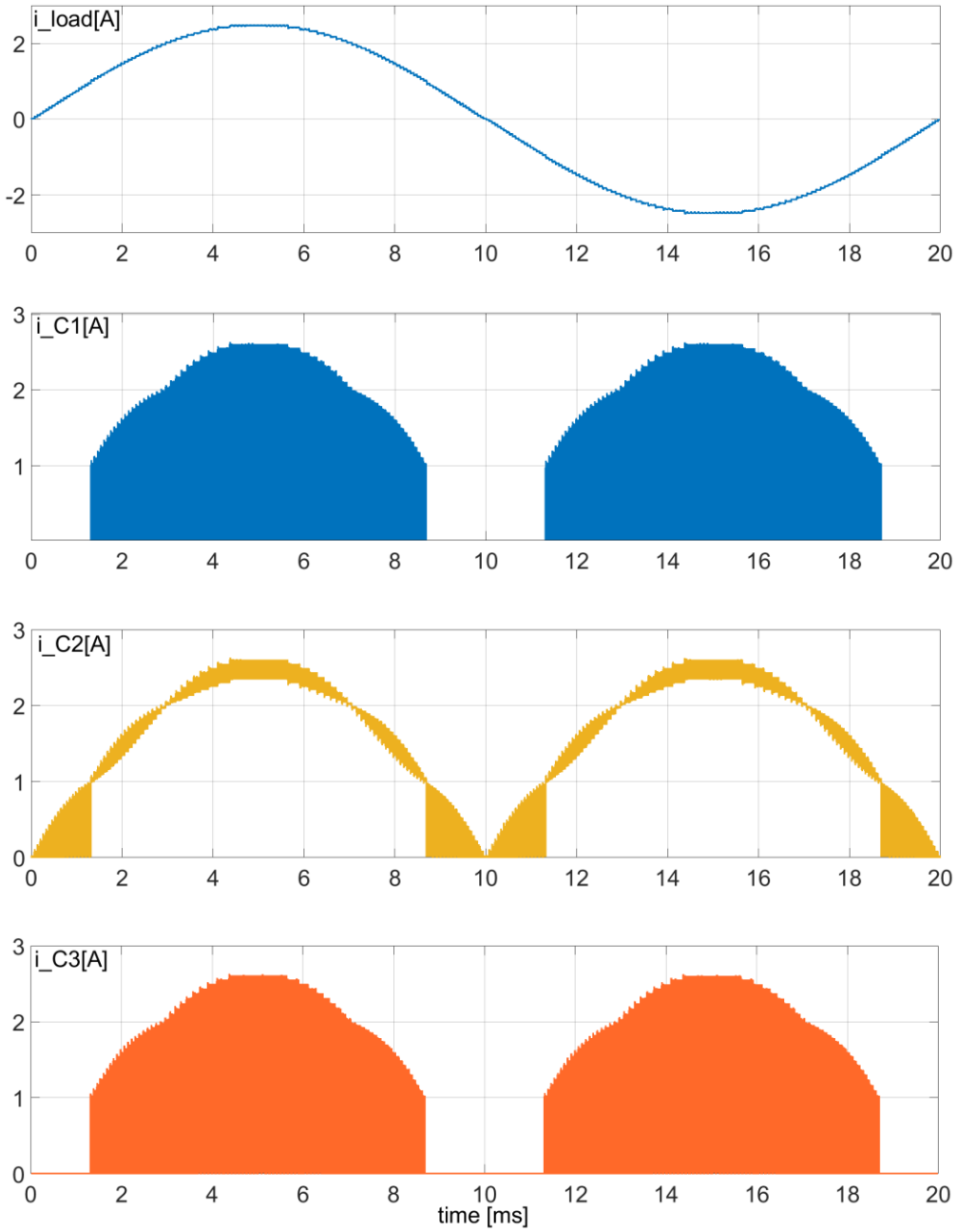


Figure 5.4: Waveforms of the seven-level inverter: current flowing through the load, input DC-link capacitors.

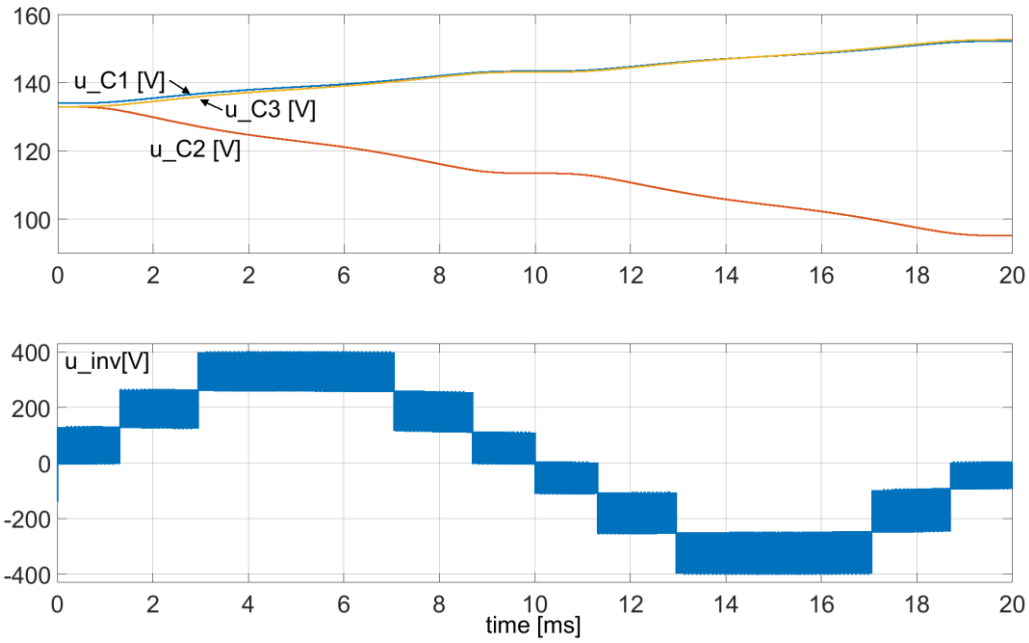


Figure 5.5: Voltages of the DC-link capacitors and inverter output voltage without the DC-link voltage balancing.

5.2. Balancing the voltages of a single-phase, seven-level NPC inverter's DC-link: simulation study

This section presents the results of a MATLAB®/Simulink® simulation of a configuration, where the SCABC is balancing the DC-link build with three series-connected capacitors, which supplies the NPC inverter. A 400 [V] DC voltage source supplies the complete DC link. The main attention was given to the development of control algorithm. The simulation results presented, provide insight into SCABC waveforms, output waveforms of the NPC inverter, and control signals and states.

5.2.1. Implementation of the control algorithm

The control system is composed in MATLAB®/Simulink® environment with the main components presented in Figure 5.6. and contains:

1. The voltage measurement with signal filtering.
2. The state machine logic.
3. The switching signals generator.
4. The switching pulses distribution block.

It is based on the core control system described in detail in sections 3.3 and 4.1 thus the transistors` turn-on signals generation and their distribution are proven as a solid design. In the state machine logic proposed in this section, a decision of proper capacitors selection for balancing process is being made. The State Machine

also decides whether the DC-link balancing is needed and conditions for the NPC inverter are sufficient to deliver power to its load.

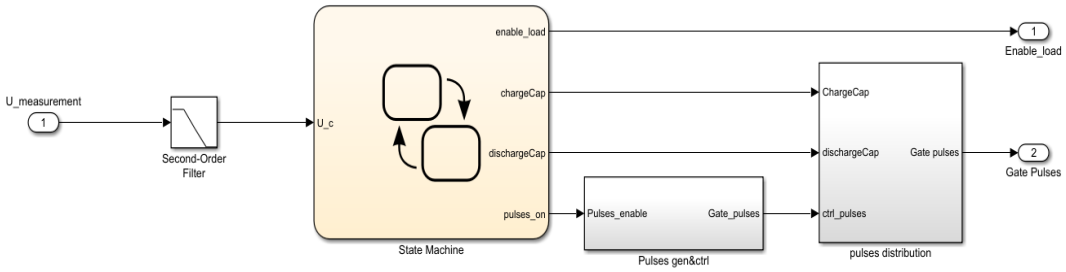


Figure 5.6: The control system of the proposed balancer implementation.

To ensure the correct operation of the control logic of the balancer, a measurement of voltages on the series-connected capacitors is mandatory. The measurement stage is composed of voltage sensors and a low-pass filter block.

The state machine (SM) consists of three main states which form a closed loop:

1. An initialization.
2. An idle mode.
3. A balancing.

The SM contains one input of bus type which is fed with the measurements of the voltages on each of the three series-connected capacitors, which are meant to be balanced. All decisions and state switching are based on those measurements, precisely on the mathematical and logical operations performed on them, which will be discussed further in this section.

The output of the state machine logic consists of four values:

1. two integers (from 1 to 3):
    a. Charged capacitor number.
    b. Discharged capacitor number.
2. two Boolean values:
    a. *pulses_on* which enables passing of control pulses to appropriate semiconductor switches when true (balancing active/not active).
    b. *enable_load* which is meant to be fed into the NPC inverter - for which the series connected capacitors are the input DC stage - and when true, indicates that the capacitors are initially balanced and ready to operate under load (normal operation of the NPC converter).

Three independent functions are implemented and run within the main state machine providing a specific output:

1. The function *delta* – it runs constantly and outputs the parameter *delta_max* which is the maximum voltage difference on series connected capacitors.
2. The function *discharge_cap* – is run asynchronously and outputs the capacitor`s number on which the voltage is the highest and thus this capacitor must be discharged at a given time.
3. The function *charge_cap* – is run asynchronously and outputs the capacitor`s number on which the voltage is the lowest and thus this capacitor must be charged at a given time.

Figure 5.7 presents a SM`s flowchart with transitions between the three main states visible. An internal data flow and decision points for each state are also presented. The diagram demonstrates also the independent functions described above, as well as the measured data distribution.

Figure 5.8 presents the implementation of the *charge_cap* function. This is the If-Else type function applied in the MATLAB®/Simulink® Stateflow [5.1]. It performs a logical operation on the values of the voltages across the capacitors, searching for the lowest one. As an output, it provides capacitor number. Its twin function *discharge_cap* works in a similar way, finding the capacitor with the highest voltage value.

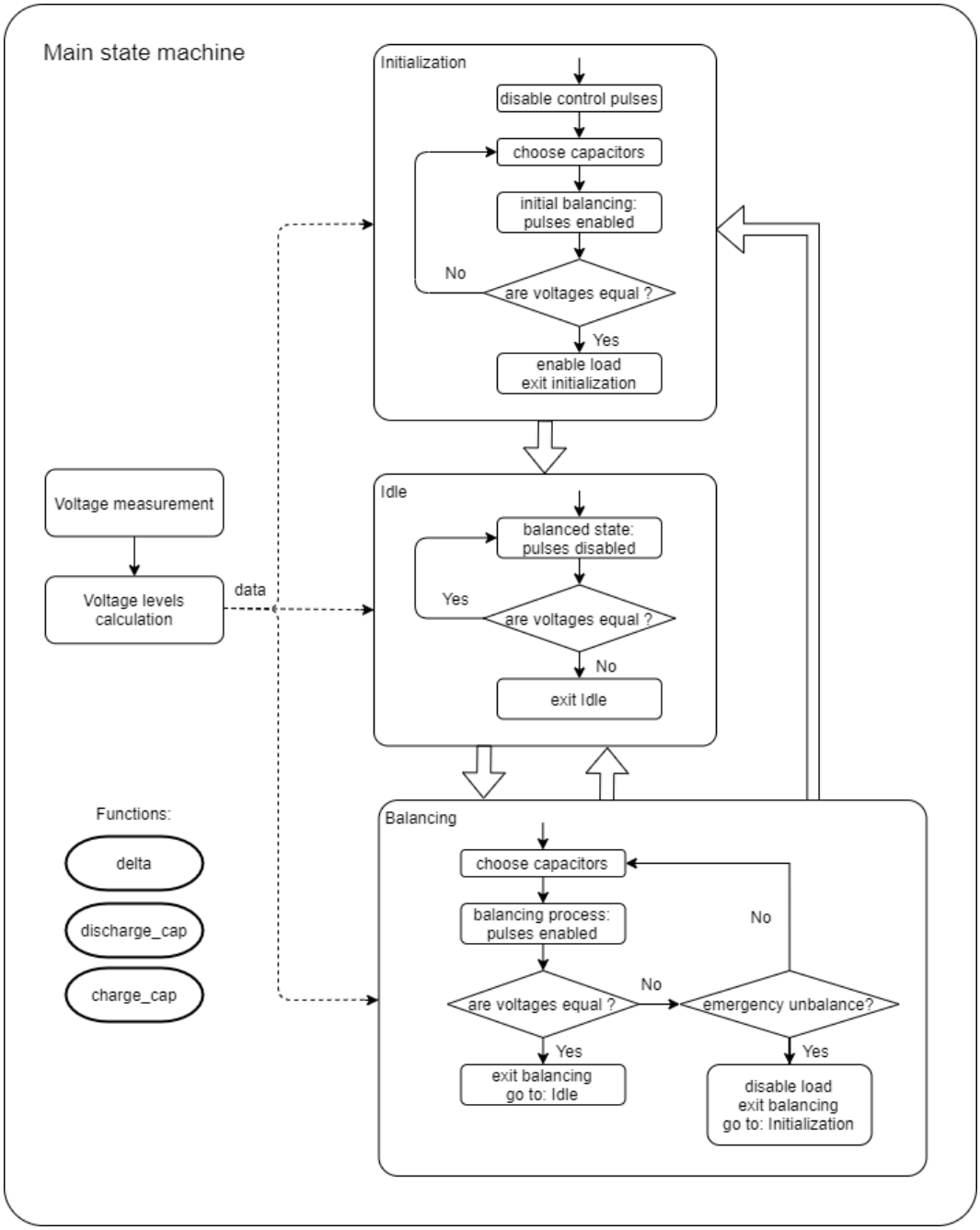


Figure 5.7: Flowchart of the balancer`s State Machine.

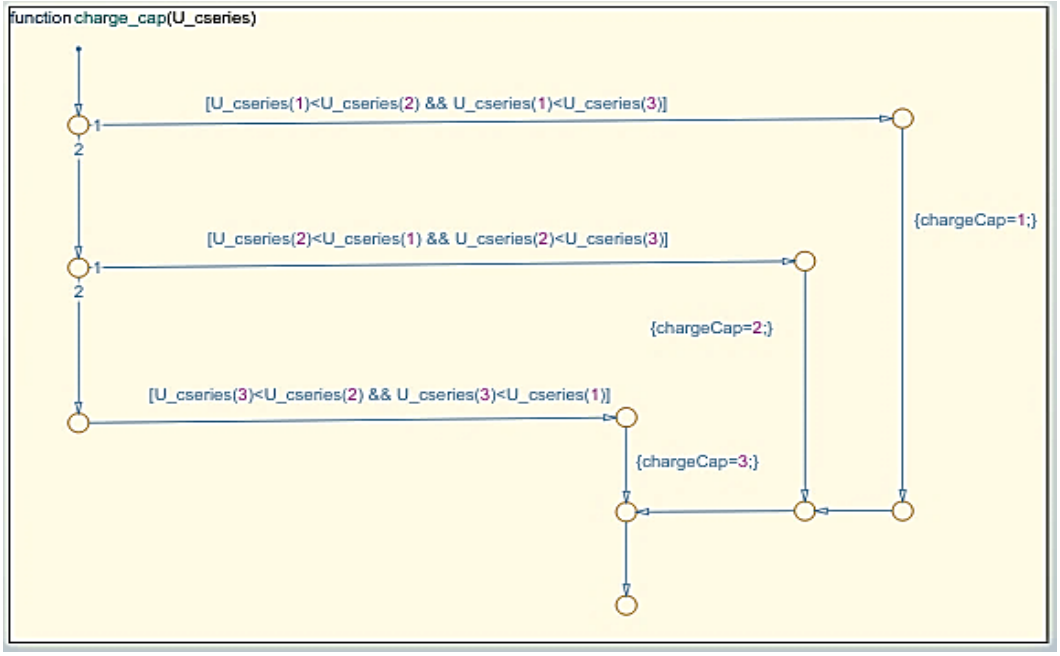


Figure 5.8: Implementation of the Simulink Stateflow function: *charge_cap*.

The State Machine consists of the following main states forming the closed-loop algorithm:

The initialization state:

This is an initial state which is entered when the device is booted. The very first operation after the entry is disabling control pulses as well as the load (*pulses_on* == false, *enable_load* == false) as a safety supervision, maintaining the balancer non-active. Then capacitor selecting functions (*charge_cap* and *discharge_cap*) are called providing numbers for the capacitors to be used for energy transfer. Once the numbers are settled, the control pulses are passed to appropriate semiconductor switches, and the balancing process occurs. As the voltage difference between the discharged and charged capacitor is less than parameter *max_cap_diff* (hysteresis) - which indicates the voltages on those have been equalized - the state machine jumps to a decision point in which the voltages on capacitors are compared. If the value of a signal *delta_max* is larger than the *unbalance_max* (hysteresis), it means that the condition of unbalance is still valid and the state machine loops again the initialization state, seeking for capacitors to be discharged and charged to satisfy the balance conditions. If the signal *delta_max* is lower than *unbalance_max* it denotes that the balance on the series connected capacitors has been achieved and the NPC converter can now operate in appropriate conditions (*enable_load* == true). The SM goes into an idle state.

The idle state:

The state is entered once the capacitors are in a balanced state, meaning that the voltages across them are equal to some given accuracy defined by the *unbalance_max* hysteresis. As no balancing is required, *pulses_on* is now false and no semiconductor switches are active. The function *delta* is constantly running in background supervising voltage difference given as *delta_max*.

The balancing state:

The state is entered from the idle state when *delta_max* exceeds *unbalance_max*, meaning the voltages across the capacitors are not equal and in the unbalance. When entering the state, the functions *charge_cap* and *discharge_cap* are called, providing capacitors which will take part in the balancing process. The appropriate semiconductors are activated by enabling *pulses_on*. During the balancing process, the voltage difference between the discharged and charged capacitors is probed, and when under *max_cap_diff*, it is assumed that voltages balance is reinstated and the state machine jumps back into the idle state.

However, if mentioned voltage difference is under *max_cap_diff* but *delta_max* is larger than *unbalance_max*, meaning that during active balancing process, a third capacitor which has not been taking part had been discharged and thus, an even deeper unbalance circumstance is present. In such a case, the balance state loops again. The new capacitors numbers are provided and the balancing process starts again in the appropriate configuration.

When within the balancing state, *delta_max* exceeds *the unbalance_limit* that indicates that the balancing process does not provide sufficient energy to keep up with power drainage from the capacitors and thus load (the NPC converter in this case) must be deactivated/derated – the *enable_load* goes to a false state and the state machine jumps to the initialization state to recover from a deep unbalance.

5.2.2. Simulation model and study

A schematic of the investigated configuration is presented in Figure 5.9. The model is composed with ones previously developed: the SCABC with core control system, the seven-level NPC inverter, and the control block described in the previous section. Parameters of the model are presented in Table 5.1

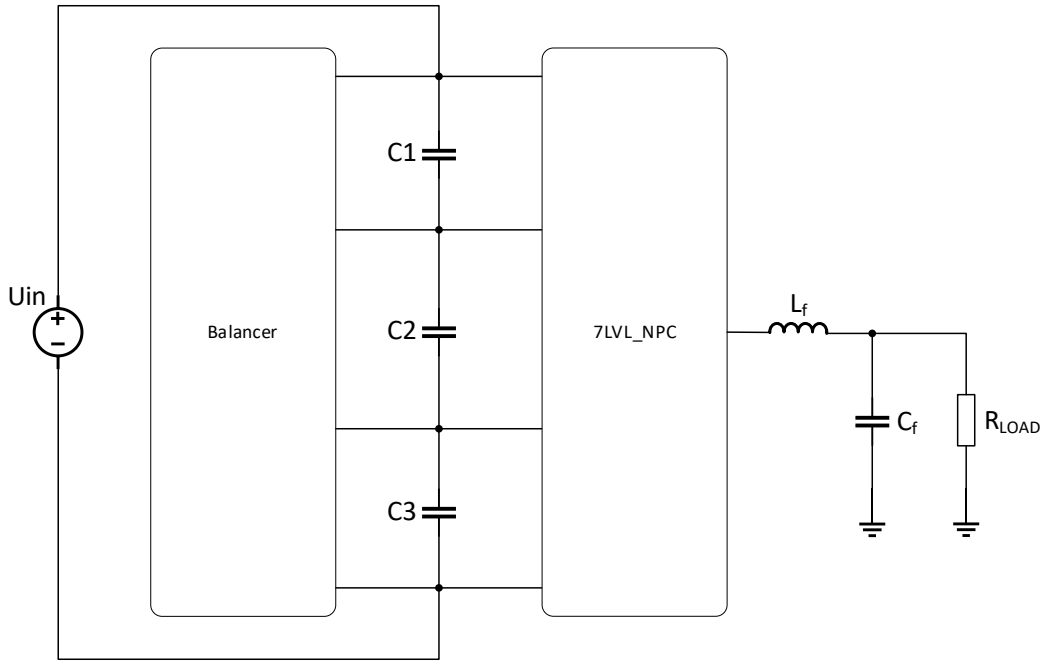
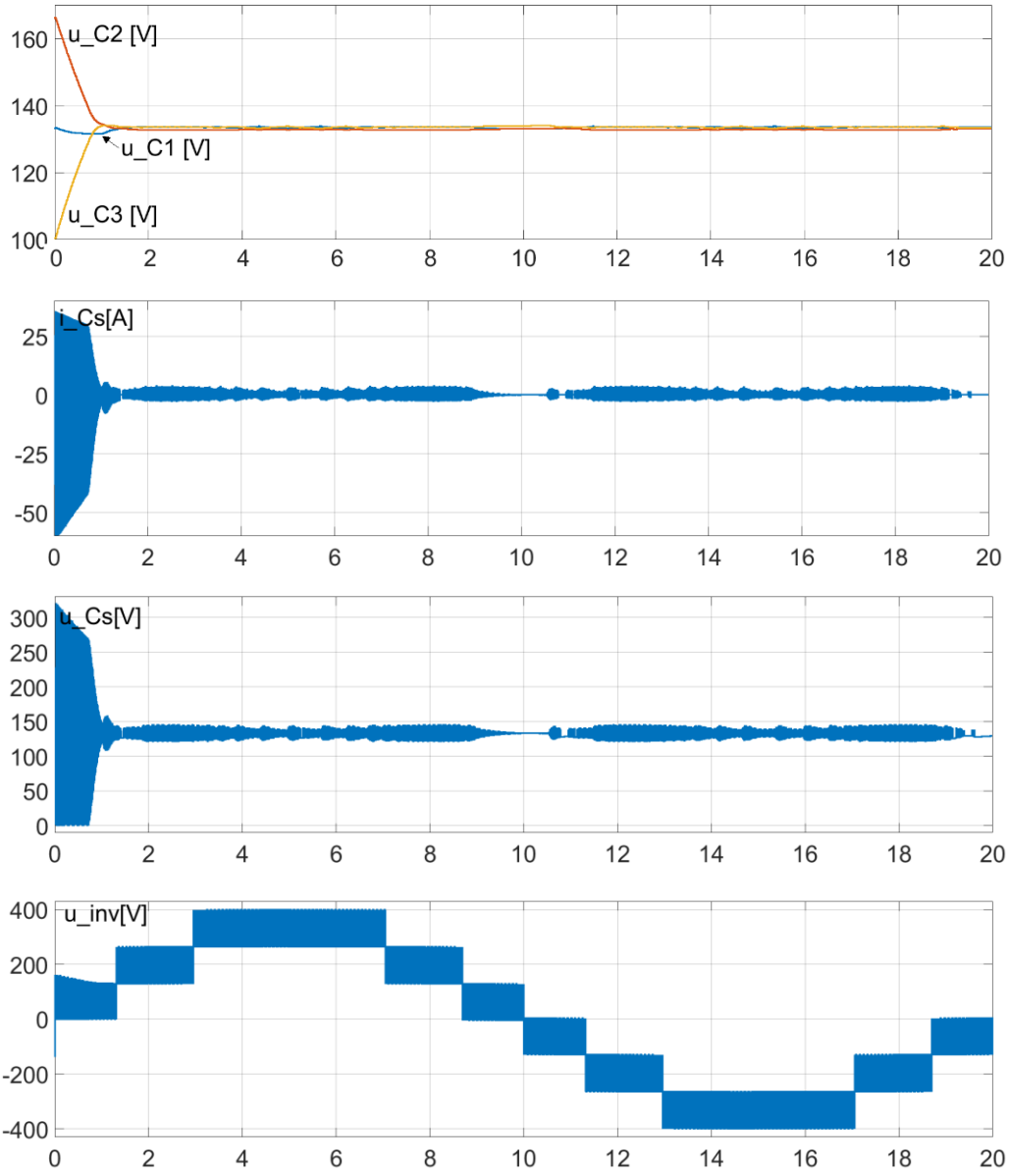


Figure 5.9: Schematic of the investigated setup in which the SCABC balances the DC-link voltages of the NPC inverter.

Table 5.1 Parameters of the simulation model: SCABC and seven-level NPC tandem.

Switched capacitor	C_S	250[nF]
Inductance	L_1, L_2	2x3[µH]
DC-link capacitors	C_1,C_2,C_3	250[µF]
DC source	U_{in}	200[V]
Parasitic resistance of SCABC circuit	R_{PR}	80[mΩ]
Switching frequency	f_{SW}	125[kHz]
Balancer`s dead-time	t_d	100[ns]
Transistors on-state resistance	R_{DS_on}	20[mΩ]
Inverter output power	P_{out}	0,4; 1; 2[kW]
Output filter parameters	L_f, C_f	500[µH]; 47[nF]
Control parameter	*unbalance_max*	3[V]
Control parameter	*max_cap_diff*	1[V]
Control parameter	*unbalance_limit*	20[V]

Two operation cases have been simulated. In the first one, the initial voltages of the DC-link are out-of-balance and the balancer must equalize them during the initialization stage. With a balance condition, the load is connected to the output of the NPC inverter. The load resistance ensures an output power of 0.4[kW]. The second case covers a situation in which the circuit operates in steady state and NPC inverter generates 1[kW] of output power. A rapid increase of load occurs – output power of 2[kW] - so that the balancer cannot keep up and deliver enough power to balance the DC-link within the given boundaries. The load is being disconnected and the balancer`s state machine jumps into the initialization mode to recover the DC-link voltages. Results are presented in Figure 5.10 and Figure 5.11 for both cases respectively.



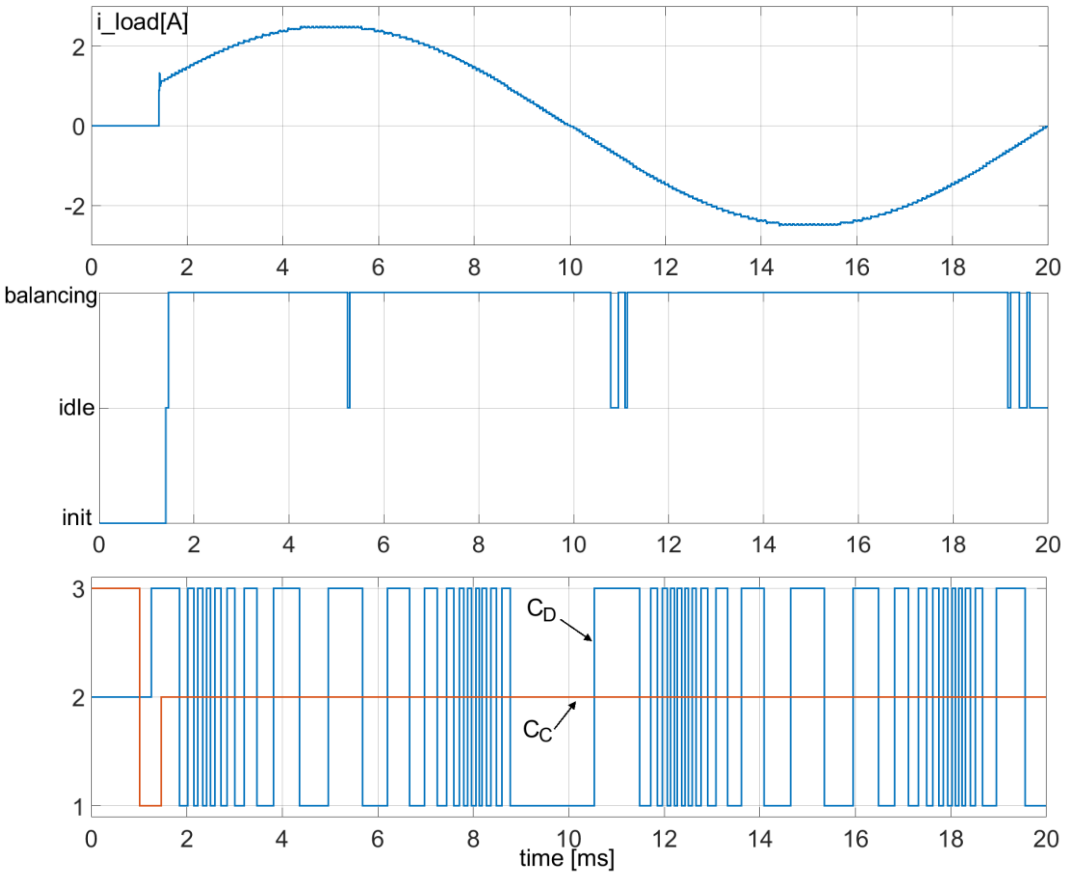
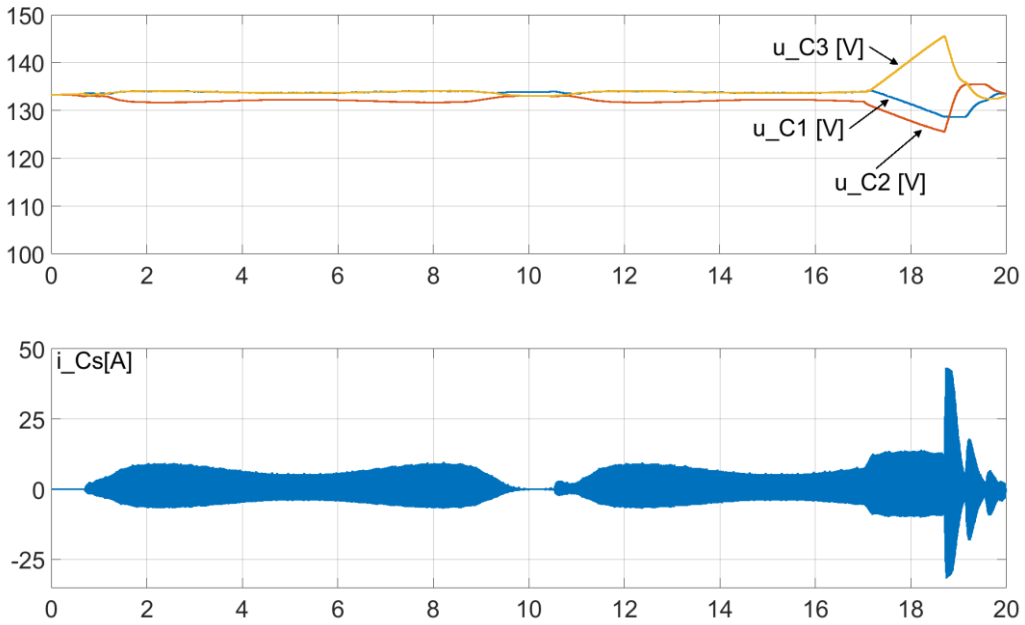


Figure 5.10: SCABC and NPC system start-up with the DC-link voltages imbalanced. Waveforms of the voltage on series-connected capacitors, C_S current and voltage, NPC inverter output voltage, NPC load current, the State Machine states, charged and discharged capacitor C_C and C_D.



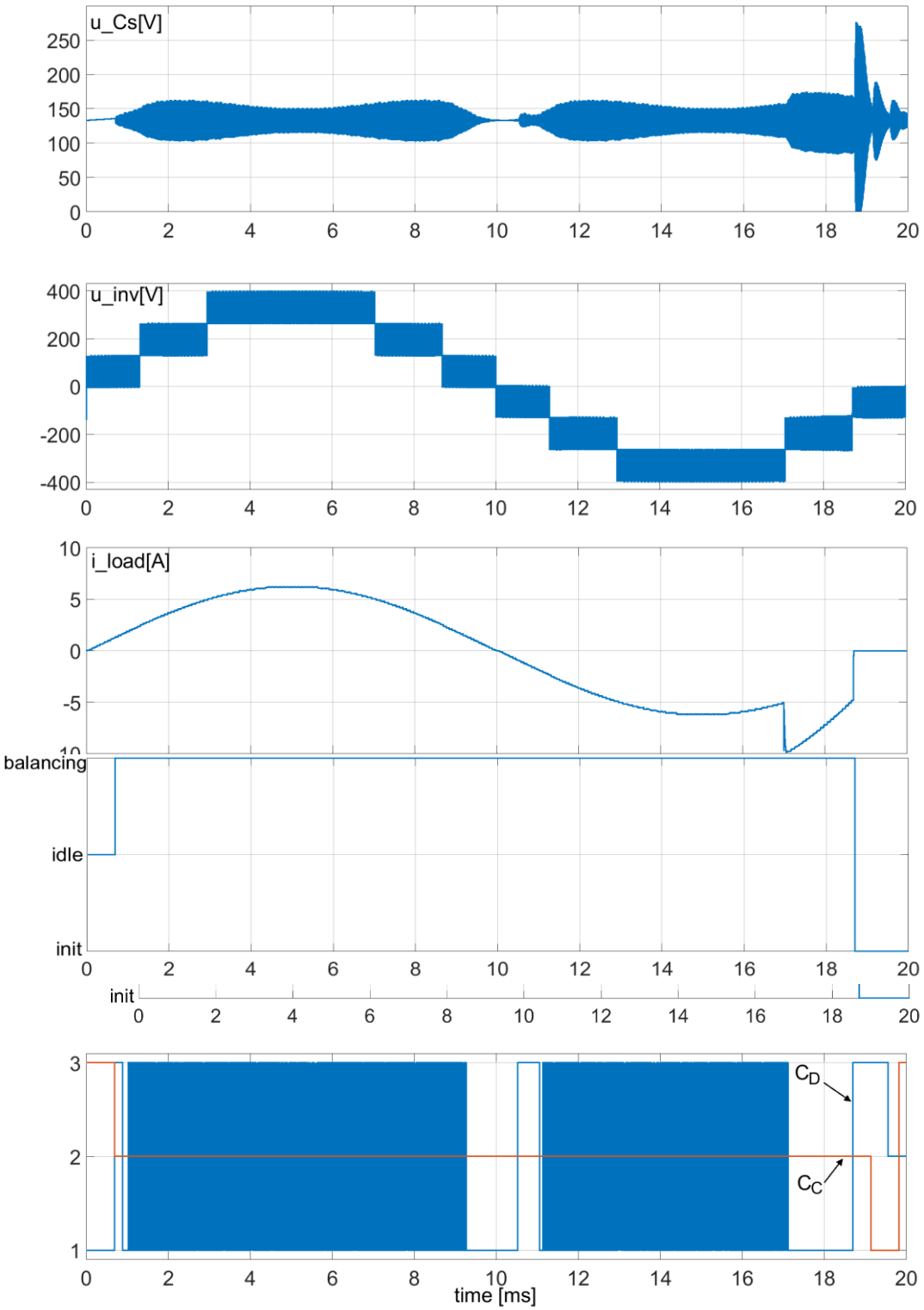


Figure 5.11: SCABC and NPC system during operation with rapid load increase (at 17[ms]). Waveforms of the voltage on series-connected capacitors, C_S current and voltage, NPC inverter output voltage, NPC load current, the State Machine states, charged and discharged capacitor C_C and C_D.

5.2.3. Results discussion and conclusions

The Switched Capacitor Active Balancing Converter controlled with the proposed algorithm successfully operated as a front converter, supplying seven-level NPC inverter with PD-PWM modulation. In the simulation case where the initial voltages of the DC-link are not balanced, the balancer restored equilibrium. Further maintenance of the capacitors` voltages was provided so that the NPC inverter operated undisturbed. In the second simulation scenario, after the output power step occurred, the balancer could not withstand the conditions and provide equal DC-link voltages. With the voltage difference above 20[V], a command is sent to disconnect the load from the NPC`s output. The SCABC jumps into the initialization state to recover the DC-link balance.

5.3. The SCABC as a DC voltage booster, supplying a seven-level NPC inverter

This section provides insight into the research in which the SCABC not only balanced the DC-link voltages for the seven-level NPC inverter, but also boosted the DC voltage that was supplied. Compared to the setup that is described in Section 5.2, only the middle capacitor C_2 of the DC-link is fed from the power supply. This type of configuration was investigated in a simulation study and in an experimental setup that was composed of the newly developed balancer circuit with the improved topology as well an NPC inverter.

5.3.1. Configuration of the SCABC as a DC voltage booster

When transferring energy from one capacitor of the series-connected branch to the other, the balancer actually doubles the voltage of the discharged capacitor. This boosting ability is limited to a unity gain when there is no hard switching. Because the circuit is meant to operate with three series-connected capacitors, it can operate as a voltage tripler. For such an operation scenario, only one of the capacitors is supplied from the DC source.

The brief study of the seven-level NPC inverter described in Section 5.1 revealed that a significant part of the energy was drained from the middle capacitor of the DC-link and the amount was dependent on the modulation index m_a of the inverter. The percentage of total energy that was fed into the NPC inverter by the

C_2 capacitor is presented in Figure 5.12. As the figure shows, the middle capacitor was the one that is most loaded, and provided over half of the energy for $m_a < 0.8$.

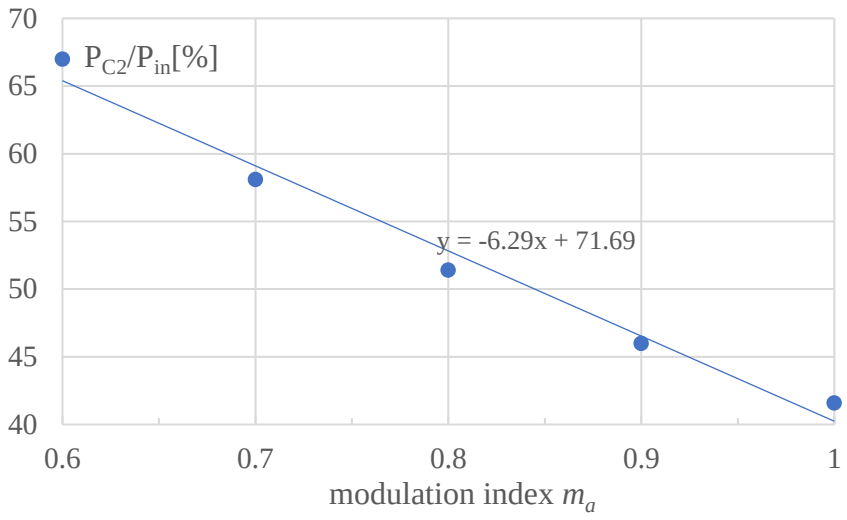


Figure 5.12: Power drainage from the middle capacitor of the DC link of the seven-level NPC. A linear approximation with the equation provided.

Connecting the DC source in parallel to one of the DC-link capacitors enabled the system to achieve a partial power conversion. The energy from the source flowed straight to the NPC`s input (one level) and some of it was not processed by the balancer. The partial power concept has been described in the literature in many topologies [5.2]-[5.4]. The solution improved the efficiency of the conversion process.

The information presented in Figure 5.12 shows that the most beneficial solution was to select capacitor C_2 to be supplied by the DC source. Capacitors C_1 and C_3 are then charged by the balancer. The configuration is shown in Figure 5.13.

With the C_2 capacitor connected to the DC source, only this capacitor was discharged and C_1 and C_3 were charged by turns. This scenario limited the number of operation modes that are presented in Table 3.1 to only three. The following switching order can be used in this type of balancer operation:

$$SwitchingOrder = \{St1, St2, St1, St3, St1 \ldots\} \tag{5.1}$$

where

$St1$: discharging C_2. Active switches: S_3, S_6.

$St2$: charging C_1. Active switches: S_3, S_4, S_5.

$St3$: charging C_3. Active switches: S_2, S_4, S_6.

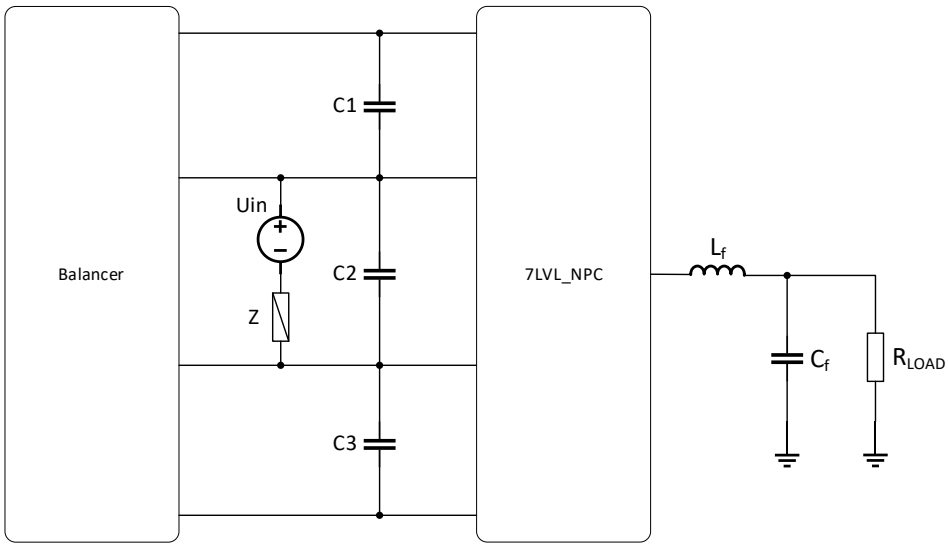


Figure 5.13: Setup of the SCABC as a front, boosting converter for the seven-level NPC inverter. The DC source was connected to the C_2 capacitor.

When the possible operation modes were limited to only those listed above, it was found that the semiconductor switches S_1 and S_7 never participated in the energy exchange process. Therefore, the circuit`s topology could be simplified, and those transistors could be replaced by diodes.

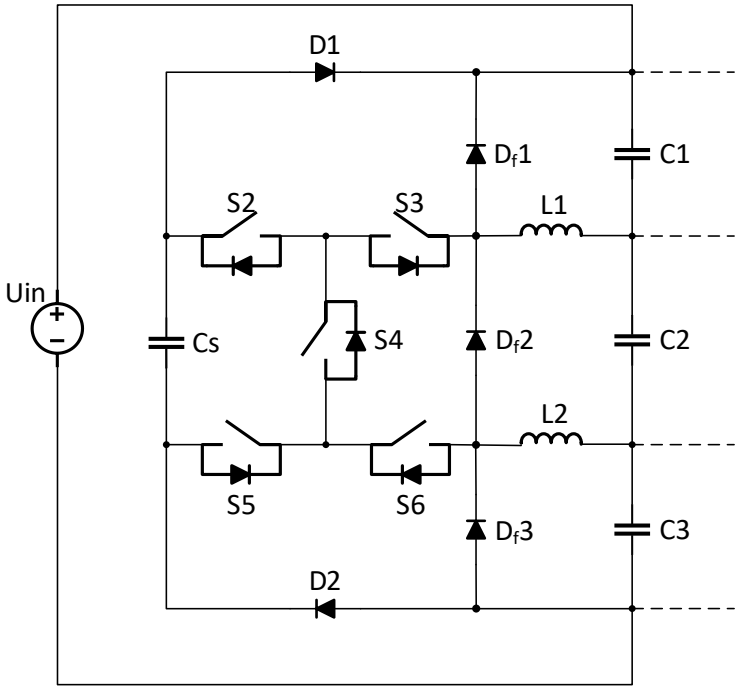


Figure 5.14: Topology of the SCABC reduced of the S1 and S7 transistors.

In the SCABC with the updated topology (Section 4.5), which now contained two inductors, the switching frequency f_{SW} was aligned with the two resonant

frequencies of the circuit. For the operation scenario in which C_2 was discharged, the resonant frequency was expressed as follows:

$$f_{RES\_1} = \frac{1}{2\pi\sqrt{(L_1 + L_2)C_s}} \tag{5.2}$$

For the modes for which C_2 or C_3 were of interest:

$$f_{RES\_2} = \frac{1}{2\pi\sqrt{L_n C_s}} \tag{5.3}$$

To match the switching frequency f_{SW} to the resonant frequencies, an adaptation was designed in the square wave generator of the control. The length of the pulse that activated the transistors in the *St1* state had to correspond to the frequency f_{RES_1} and complementary pulses for *St2* and *St3* had to correspond to the f_{RES_2}. Still, the condition that $f_{SW} \leq f_{RES}$ had to be fulfilled. In the scenario in which the inductances L_1 and L_2 were equal, the following relationship occurred:

$$f_{RES\_1} \approx 0.7 f_{RES\_2} \tag{5.4}$$

$$t_{St1} = 0.5 f_{RES_1}; \quad t_{St2} = 0.5 f_{RES_2};$$
$$T_0 = t_{St1} + t_{St2} + 2t_d; \; f_{SW} = \frac{1}{T_0} \tag{5.5}$$

Figure 5.15 shows the control pulses on the time scale with the dependencies that were determined by equation (5.5)

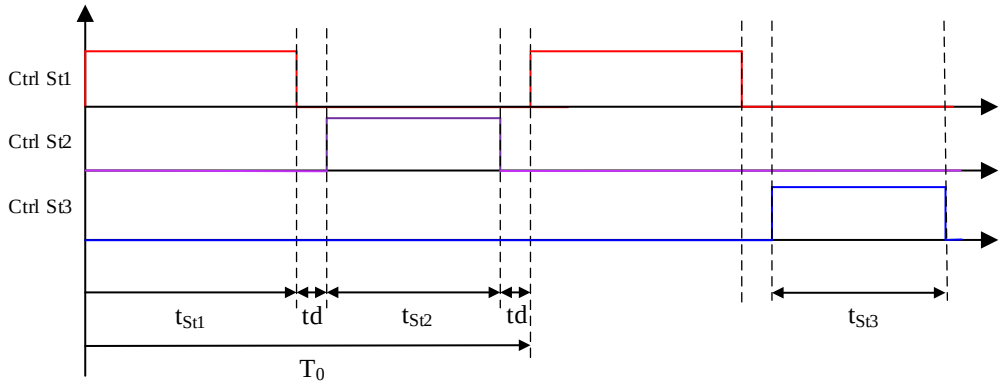


Figure 5.15: The control signals for the updated SCABC topology with two resonant frequencies

The control principle of the balancer in such a configuration is meant to be as simple as possible and therefore an open control loop that was based on the core control system (Section 3.3) was used. The *Turn-on pulses distribution* block was constantly fed with integer 2 as the discharged capacitor number, whereas the charged capacitor number was switched between 1 and 3 at each falling edge of the *Ctrl St1* signal. In this way, the switching order (5.1) was fulfilled.

For the consideration of the power that was to be converted by the balancer, the following assumptions were made: U_{in}=133[V] $\Rightarrow U_{DC\text{-}link}$=400[V]; P_{ACmax}=1[kW], U_{ACrms}=230[V] $\Rightarrow m_a$=0.8. For the given modulation index $m_{a,}$, the power that was consumed by the NPC inverter straight from the DC source was slightly above 50% and the rest – 0.5[kW] – were converted by the balancer. Using equation (3.10), the minimum capacitance of the switched capacitor *Cs* was determined [P.3]:

$$C_S \geq \frac{2P}{u_{\mathrm{Cmax}}{}^2 f_{SW}} = 256[nF] \tag{5.6}$$

5.3.2. Simulation setup and results

The configuration presented in Figure 5.13 was composed as a MATLAB®/Simulink® model and simulations were performed. The parameters applied in the model are presented in Table 5.2.

Table 5.2: The simulation parameters of the SCABC in the voltage-boosting configuration.

Switched capacitor	C_S	320[nF]
Inductance	L_1, L_2	2x3[µH]
Resonant frequency	f_{RES_1}; f_{RES_2}	115;142[kHz]
DC-link capacitors	C_1,C_2,C_3	500[µF]
DC source	U_{in}	133[V]
Parasitic resistance of the SCABC circuit	R_{PR}	80[mΩ]
Switching frequency	f_{SW}	110[kHz]
Balancer`s switching dead-time	t_d	100[ns]
On-state resistance of transistors	R_{DS_on}	20[mΩ]
Diode forward voltage	V_f	1.5[V]
Inverter output power	P_{out}	1[kW]
Output filter parameters	L_f, C_f	500[µH]; 47[nF]

The simulation results presented in Figures 5.16 to 5.20 offer insight into the voltages and currents of the series-connected capacitors, current and voltage of the

switched capacitor C_S, the current of the inductors L_1 and L_2 and the output waveforms of the NPC inverter: voltage and current as well as the current that was drawn from the DC power supply.

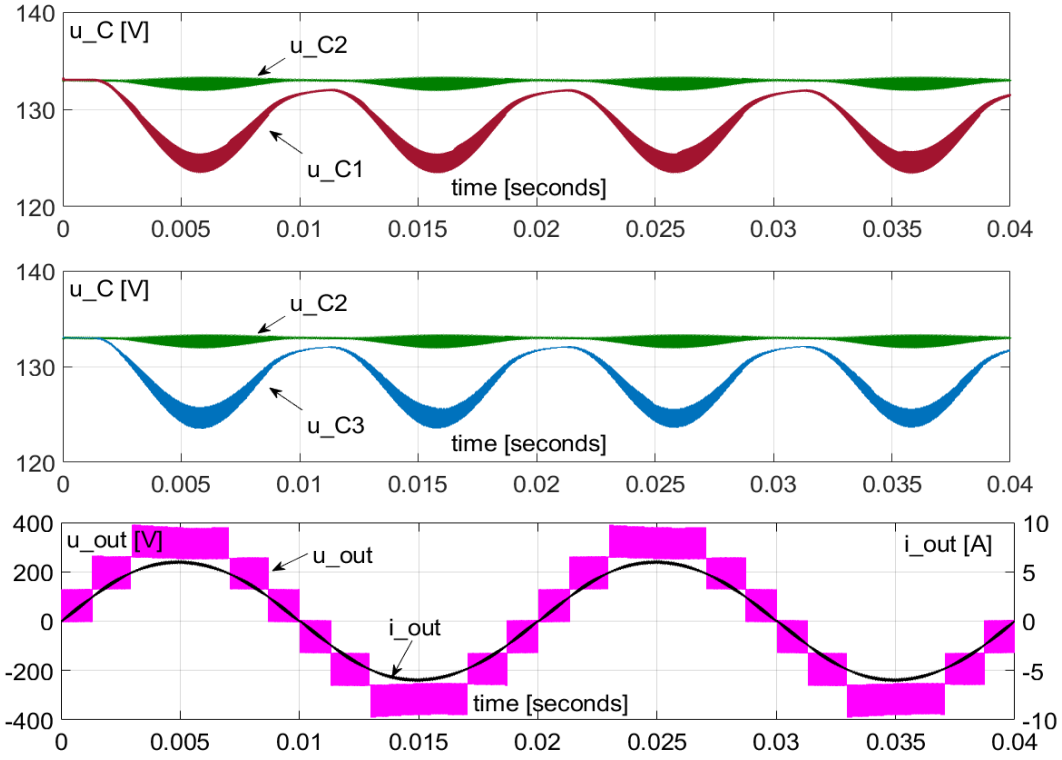


Figure 5.16: Waveforms of the voltages of the DC-link capacitors C_1, C_2, C_3 as well as the output voltage and current of the NPC inverter. A time frame of two periods of the inverter`s output, 50Hz signal [P.3].

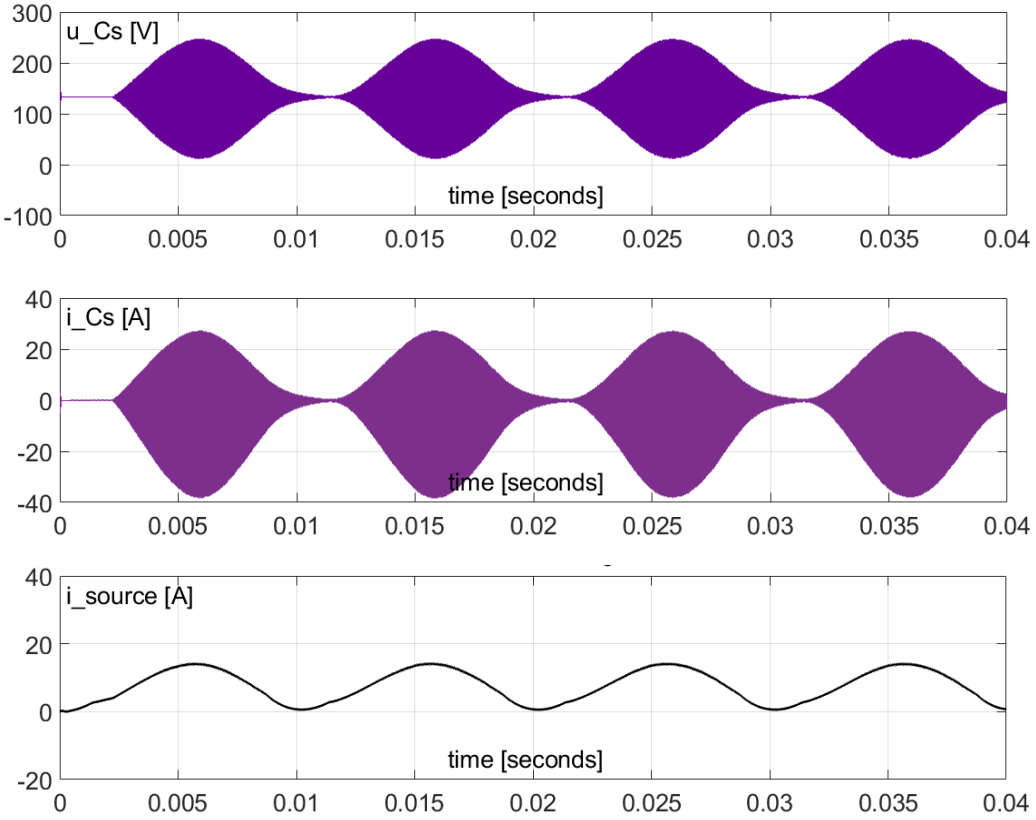


Figure 5.17: The voltage and current of the switched capacitor C_S. A time frame of two periods of the inverter`s output, 50Hz signal [P.3].

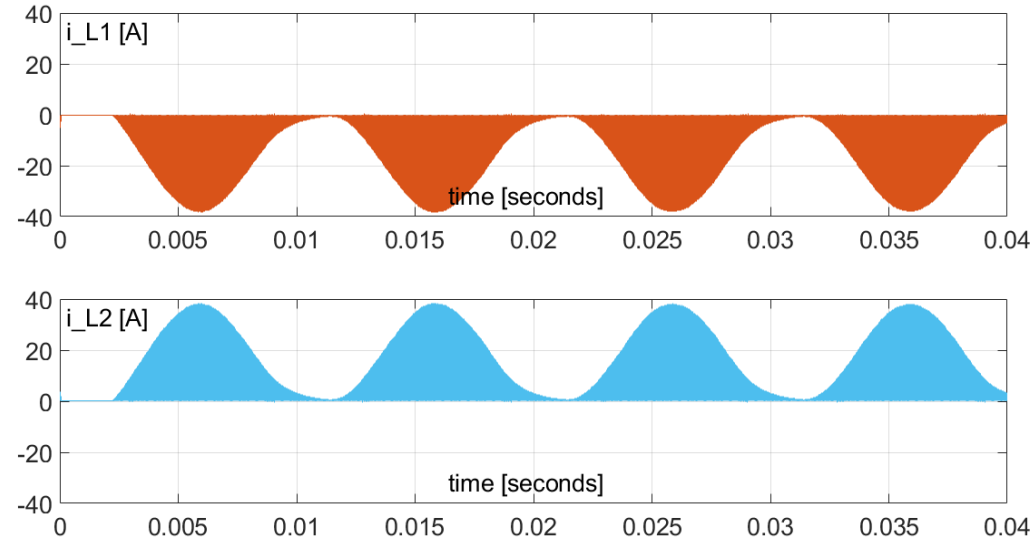


Figure 5.18: The inductor L_1 and L_2 current. A time frame of two periods of the inverter`s output, 50Hz signal [P.3].

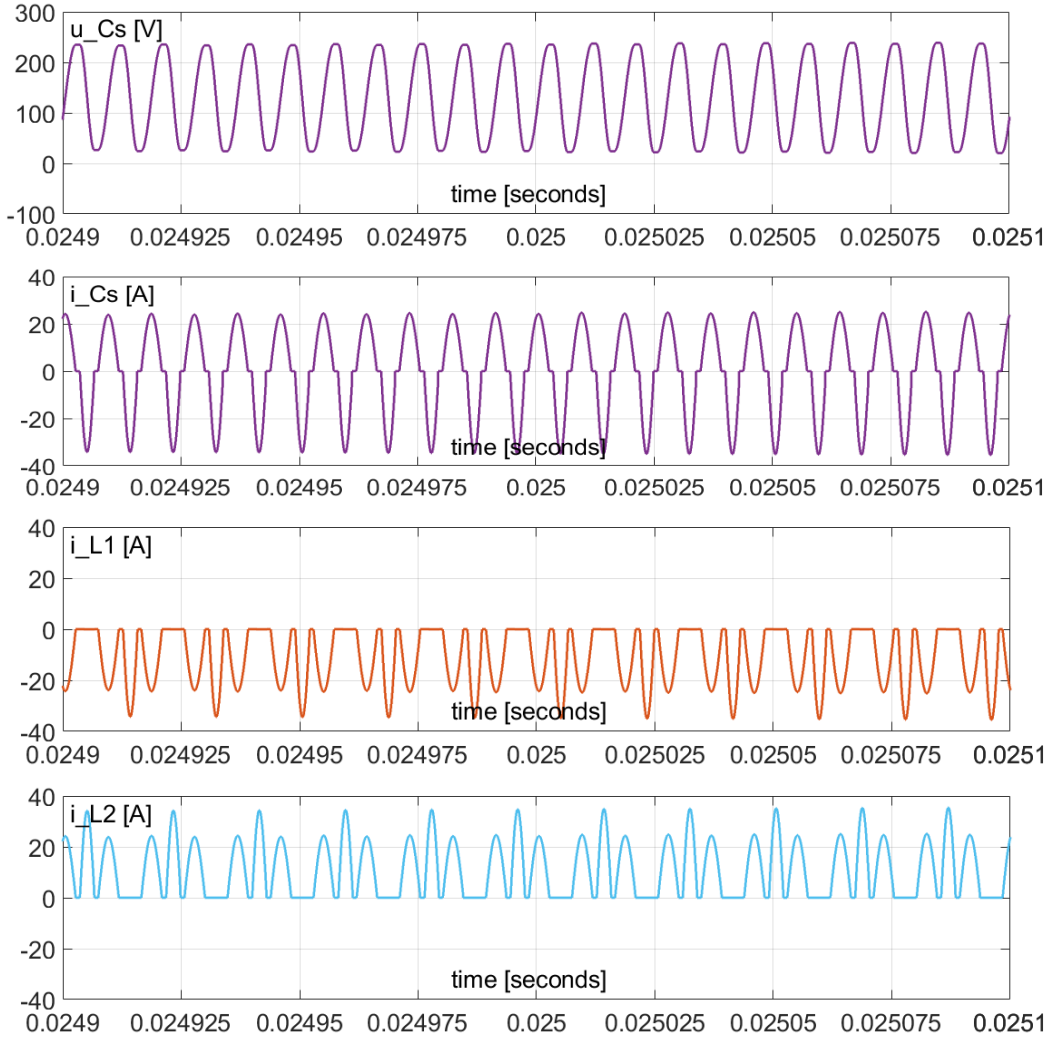


Figure 5.19: Steady state waveforms of the balancer`s resonant branch: C_S and $L_{1,2}$. A time frame of 200[μs] [P.3].

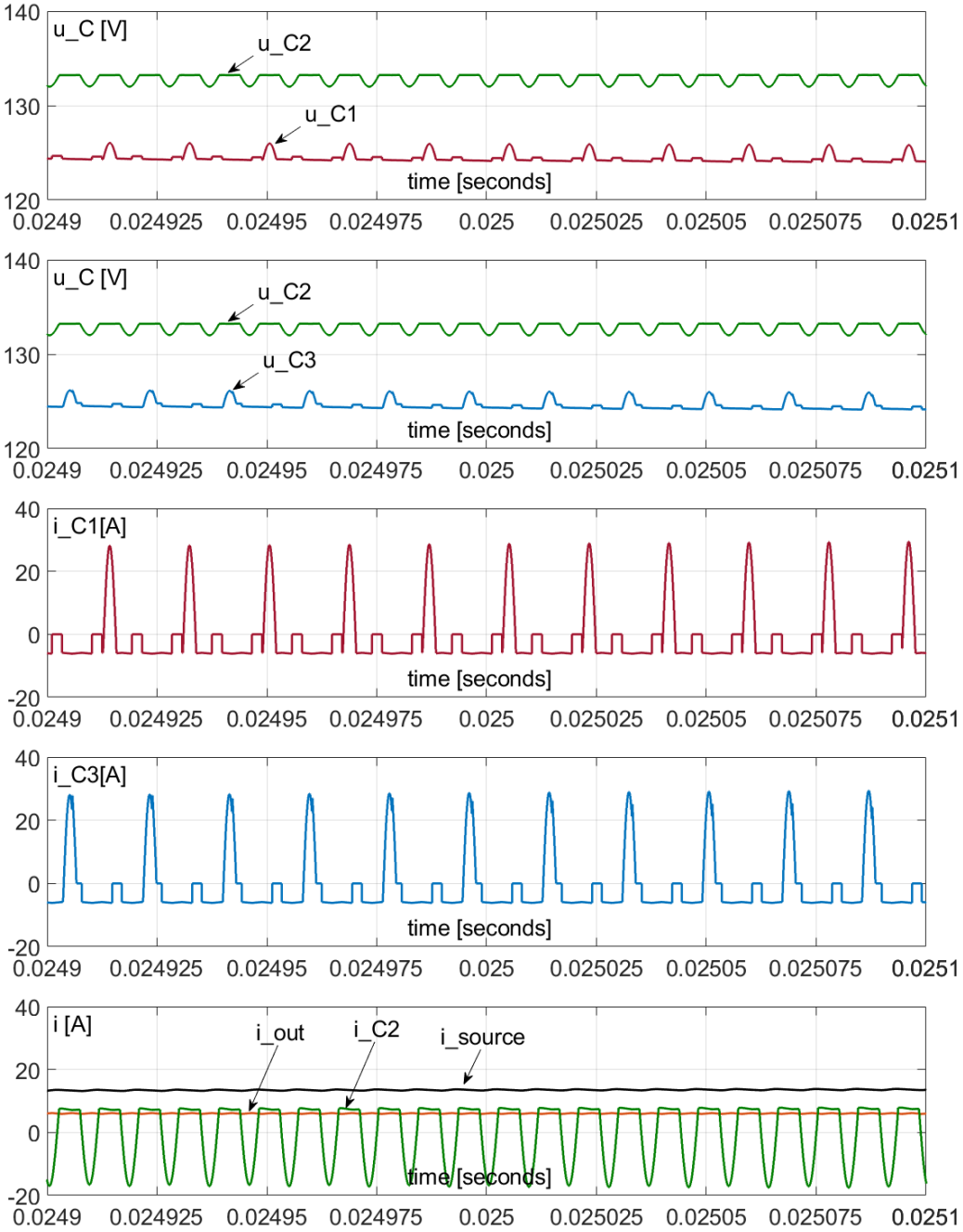


Figure 5.20: Steady-state waveforms of the balancer and the NPC inverter: voltages of the series-connected capacitors, currents of the charged capacitors C_1 and C_3, current of the DC source, discharged capacitor C_2 and the output current of the NPC inverter. A time frame of 200[μs] [P.3].

5.3.3. Experimental setup and presentation of results.

A new device was designed and built using the new and improved topology of the balancer. The PCB that was developed was equipped with GaN HEMT semiconductors from the Transphorm TP65 series [5.5] in the TO-247 package. Two kinds of semiconductors with different R_{DS_on} parameters were tested: 50 and 35 [mΩ]. The schematic of the balancer`s power path is presented in Figure 5.21

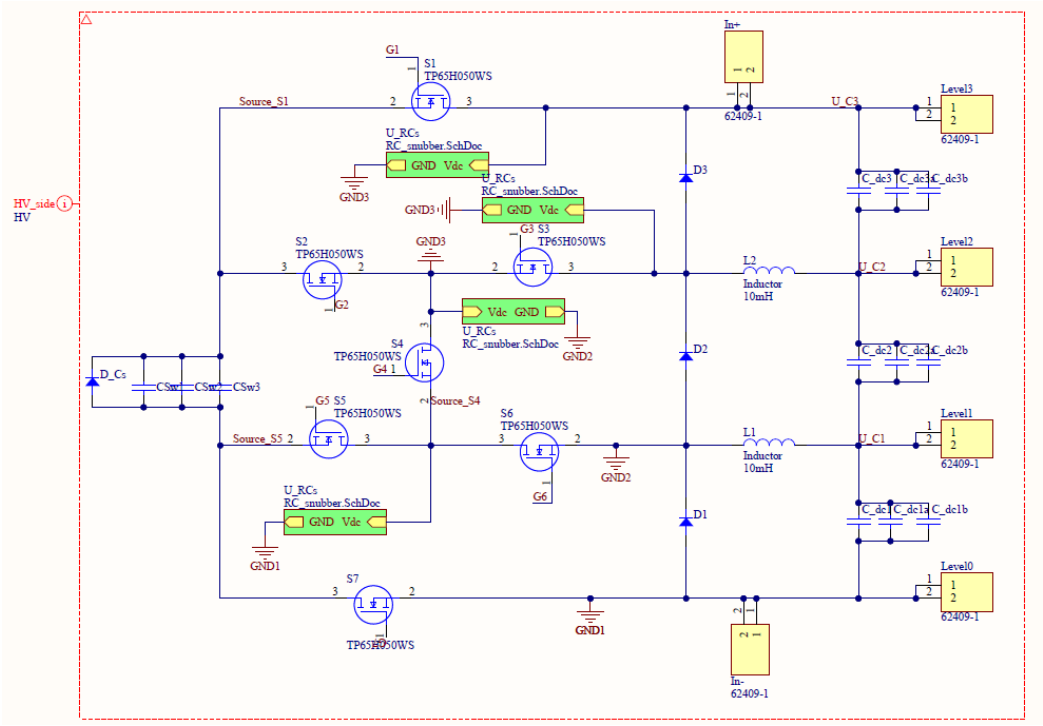


Figure 5.21: Schematic of the new topology for developing the PCB.

In the PCB design, planar inductors with a ferrite E22 [5.6] core were used. Unfortunately, probably due to the manufacturing fault, the winding of one of the indictors had shorted turns. The author decided to use the same cores to build wound inductors using a 100x0.1[mm] litz wire. The cores were gapped using 0.3mm spacers. With four turns, the setup provided an inductance of 3[μH], a saturation knee starting at 43[A] of the DC current and an AC resistance of 10[mΩ] at 100[kHz].

In addition to the power circuit, the design also contained:

1. The gate driver circuit
2. The power supply of the gate drivers and electronic components
3. The voltage measurement circuit that was built with an AMC1211AQDWVRQ1 op-amp to feed the signals into the ADC.

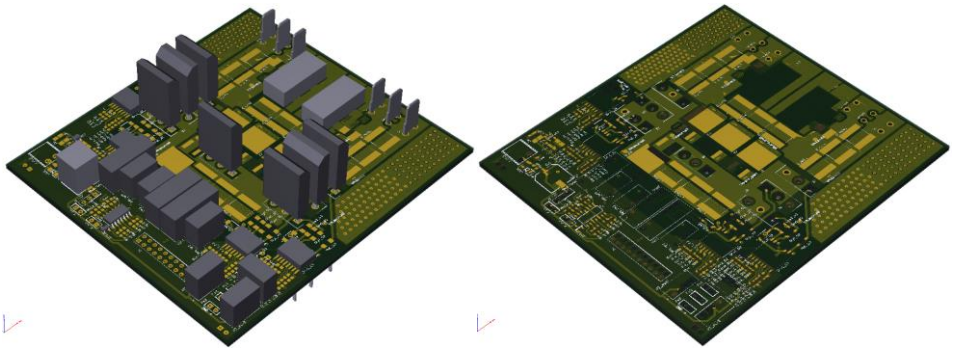


Figure 5.22: The PCB of the updated balancer circuit: a 3D view from Altium designer software.

Tables 5.3 and 5.4 present the details of the investigated system while Figure 5.23 presents the system during the experiment that was conducted. As can be observed, diodes D_1 and D_2 were placed on heatsinks separately from the one for the transistors. The intention was to allow them to operate at the highest possible temperature so that the forward voltage drop V_f was lower and improved the circuit`s efficiency. The investigated balancer was tested in a system with a seven-level NPC inverter in the single-phase bridge topology. The design of the inverter was not part of the research for this dissertation, but it was assembled and commissioned by the author of this dissertation.

Table 5.3: Hardware details of the NPC inverter and the balancer for the experimental setup.

The SCABC

Switching frequency f_{SW}	110[kHz]
Switches in the balancer:	TP65H050WS, TP65H035WS
Diodes in the balancer:	DPG80C300HB

The NPC inverter

Switching frequency f_{SW}	78[kHz]
Switches in the inverter:	IPB107N20N3GATMA1
Diodes in the inverter:	IDB15E60ATMA1

Table 5.4: Detailed information on the experimental setup with the balancer as the voltage booster,

Switched capacitor	C_S	260[nF]
Inductance	L_1, L_2	2x3[µH]
Resonant frequency	f_{RES_1}; f_{RES_2}	127;180[kHz]
DC-link capacitors	C_1,C_2,C_3	470[µF]
DC source	U_{in}	133[V]
Switching frequency	f_{SW}	110[kHz]
Balancer's Dead-time	t_d	100[ns]
Inverter output power	P_{out}	1[kW]
Output filter parameters	L_f, C_f	500[µH]; 47[nF]
FPGA controller	-	Cyclone III

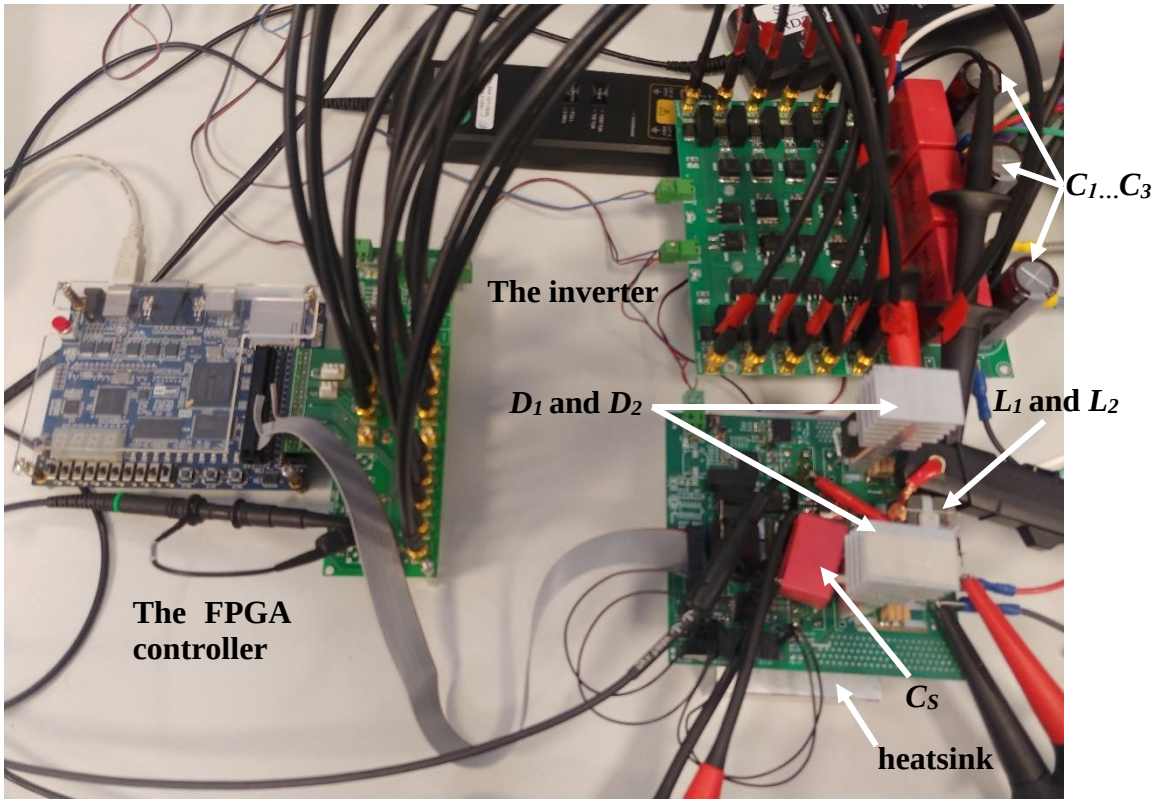


Figure 5.23: The experimental system: Cyclone III FPGA, the NPC inverter, and the SCABC.

The results of the experiments that were performed by the author of the dissertation are presented in Figures 5.26 to 5.28. The waveforms of the voltage and current of the switched capacitor, the currents of the resonant chokes, the output

voltage of the inverter as well as the DC source current are also provided. The performance of the balancer and the NPC tandem was evaluated by measuring their efficiency. The scheme of the setup is presented in Figure 5.24. A Yokogawa WT3000 power analyser [5.7] was used to measure the efficiency. The results are presented in Figure 5.29. In order to obtain only the SCABC efficiency, a setup for measuring the NPC inverter was built. The diagram is presented in Figure 5.25 and the measurement results are presented in Figure 5.30.

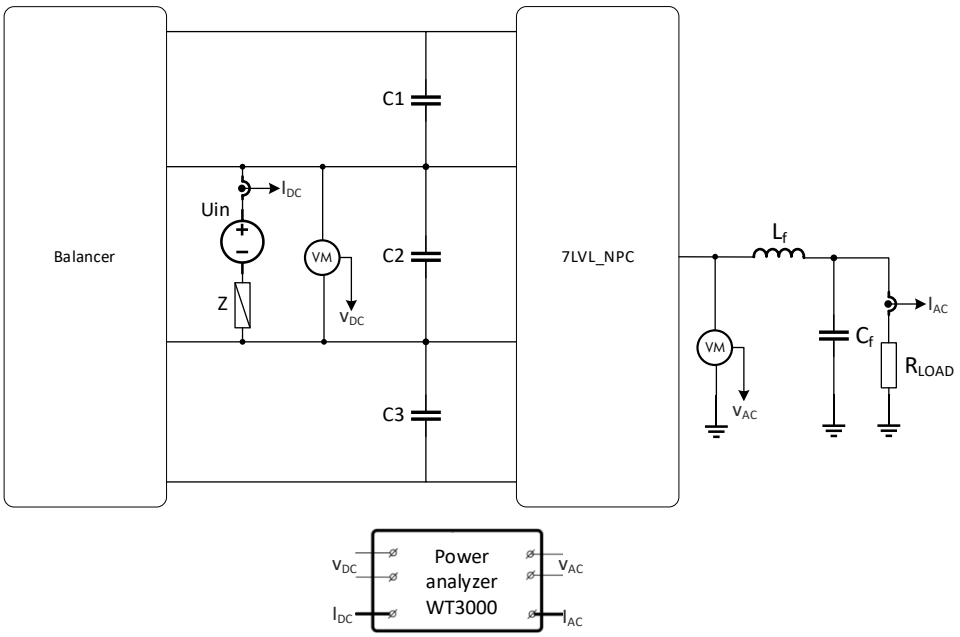


Figure 5.24: Laboratory setup to measure the efficiency of the circuit.

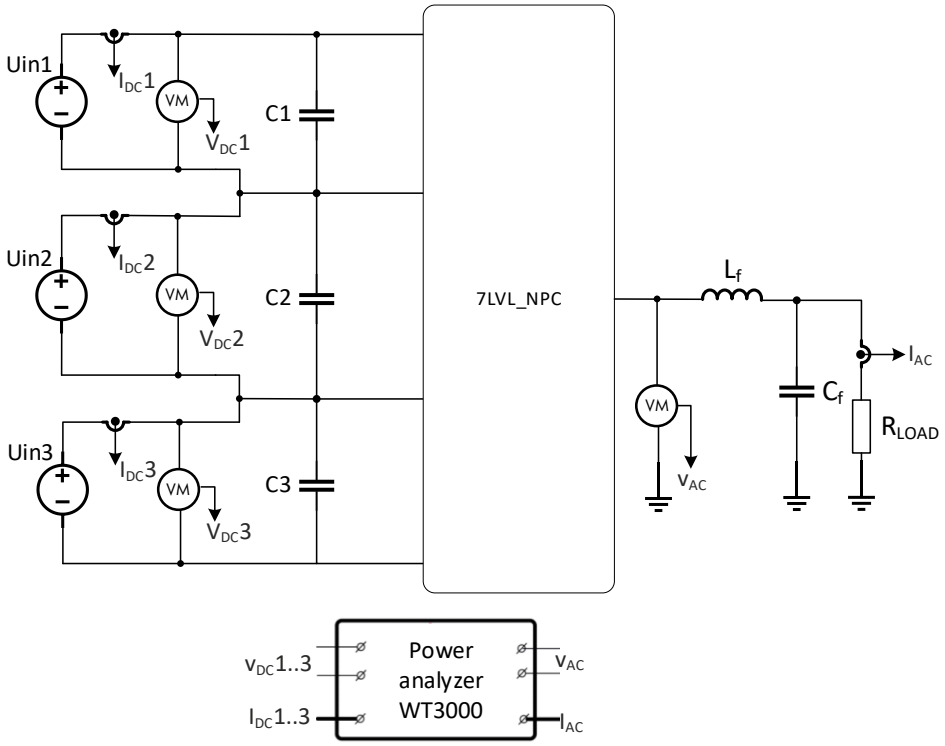


Figure 5.25: Laboratory setup for measuring only the NPC efficiency.

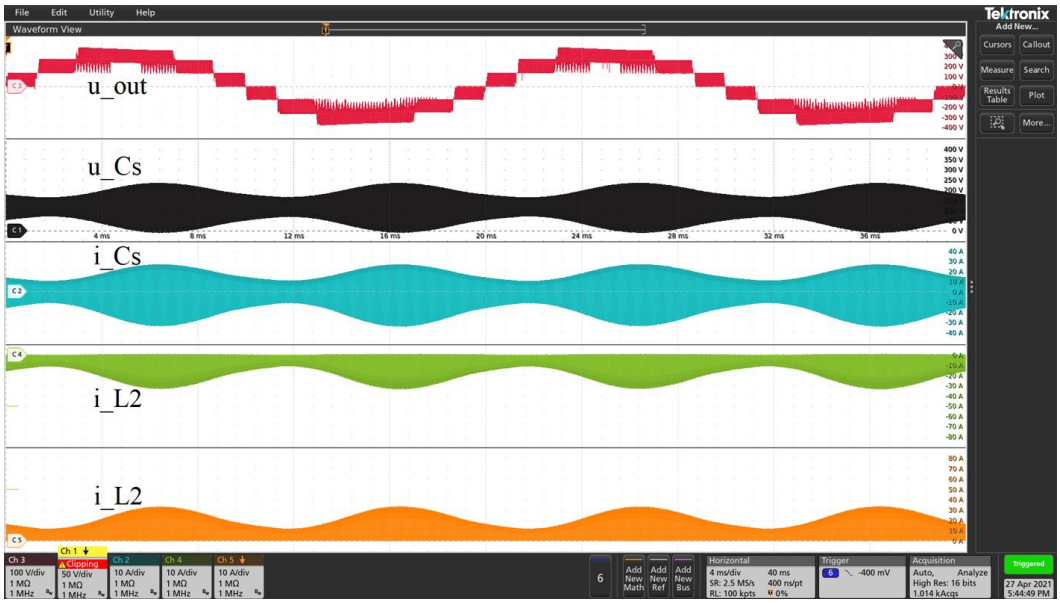


Figure 5.26: Operation of the balancer in the boosting mode for supplying the NPC inverter. The waveforms of the output voltage of the inverter (100[V/div]), the voltage and current of the switched capacitor (50[V/div], 10[A/div]) as well as the currents of resonant chokes (10[A/div) [P.3].

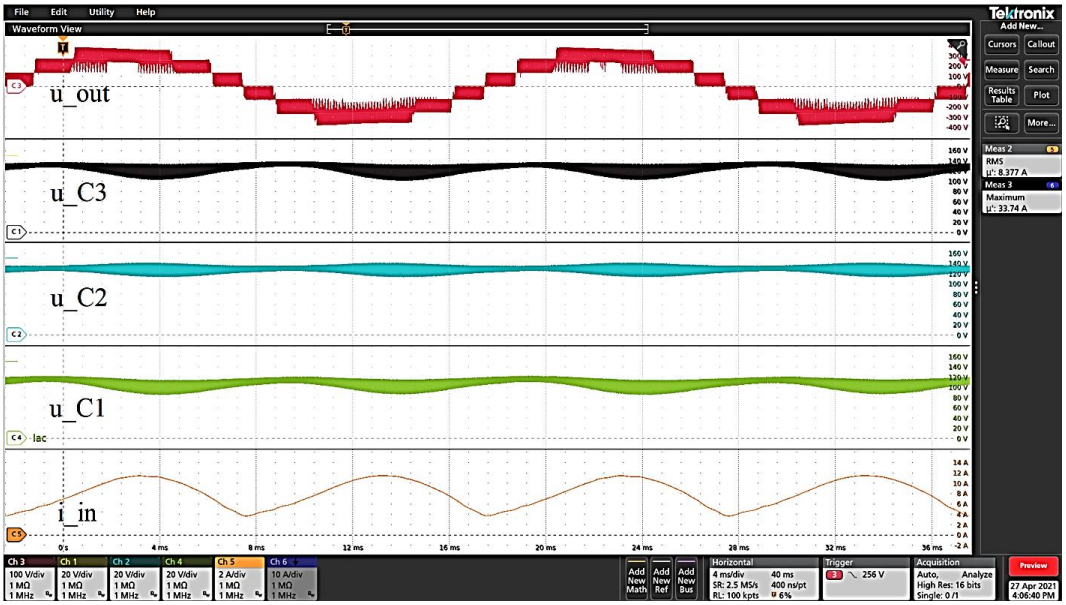


Figure 5.27: Operation of the balancer in the boosting mode for supplying the NPC inverter. The waveforms of the output voltage (100[V/div]), the voltage on the DC-link capacitors (100[V/div]) and the current of the DC power supply that was connected with the C2 capacitor (2[A/div]) [P.3].

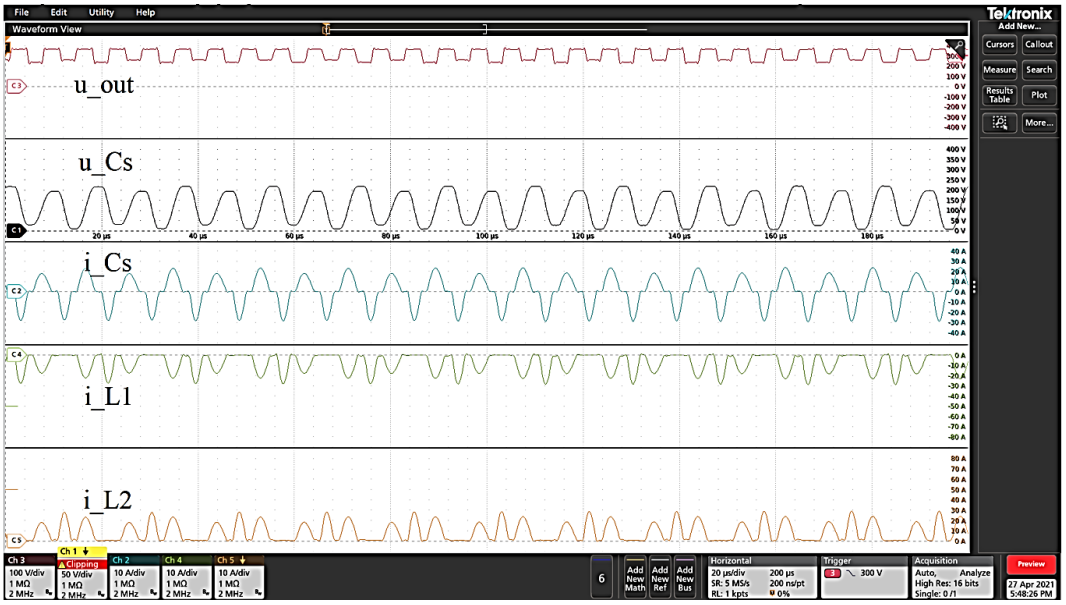


Figure 5.28: Operation of the balancer in the boosting mode for supplying the NPC inverter. The waveforms of the output voltage of the inverter (100[V/div]), the voltage and current of the switched capacitor (50[V/div], 10[A/div]) as well as the currents of the resonant chokes (10[A/div); 20 µs/div [P.3].

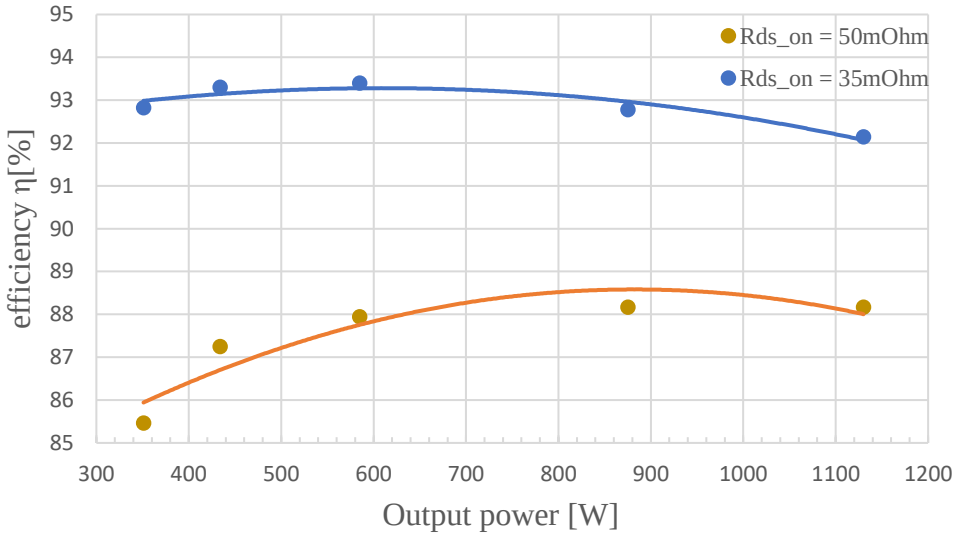


Figure 5.29: Efficiency of the balancer and the NPC tandem for two values of the semiconductors` R_{DS_on}.

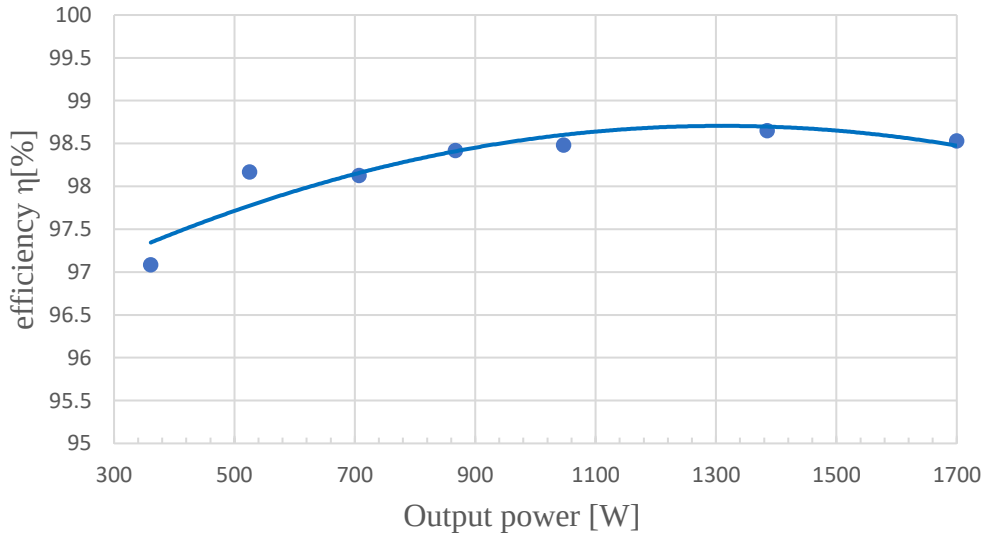


Figure 5.30: Efficiency of the seven-level NPC inverter that was supplied from three DC power sources.

5.3.4. Results summary and conclusions

For the research conducted, the balancer was configured in a way in which the C_2 capacitor was supplied from the DC source, and the capacitors C_1 and C_3 were fed by the SCABC. In this manner, the supply voltage was boosted three-fold and provided the energy source for the seven-level NPC inverter. The voltages of the DC-link capacitors remained balanced. However, a minor voltage drop of an oscillatory nature occurred on capacitors C_1 and C_3. The frequency was a double-grid frequency. This phenomenon was caused by the parasitic resistances and voltage drops in the SCABC circuit. When the circuit was simulated using

idealised components – $R_{DS\_on} = 0$ and $V_f = 0$ – the voltage on the charged capacitors was almost linear. The comparison is presented in Figure 5.31.

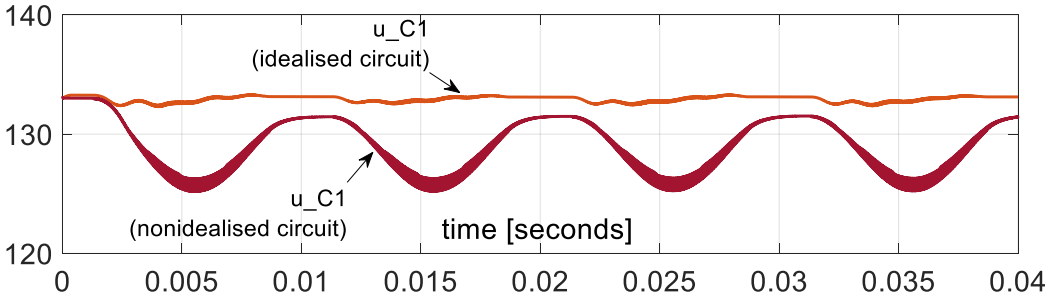


Figure 5.31: The steady state waveforms of voltage on the C_1 DC-link capacitor in the idealised scenario (R_{DS_on}=0 and V_f=0), and in the non-idealised scenario ($\sum R_{DS\_on} \approx 100[m\Omega]$ and $V_f \approx 1.5[V]$ for each diode) [P.3].

The efficiency of the SCABC and the NPC tandem in which the peak performance was reached at approximately 600[W] was also measured. In addition, the impact of the on-state resistance of the transistors was shown because a measurement was recorded for two types of semiconductors. To extract only the SCABC efficiency, the NPC inverter was measured. With the inverter`s efficiency loss of approximately 2% at 600[W], it was assumed that the peak efficiency of the SCABC reached 95.4%.

6. Active power decoupling ability of the SCABC connected to the multilevel NPC inverter.

This chapter presents the research in which the SCABC compensated a ripple at a double frequency of the output fundamental frequency, which propagated to the DC side of the subsystem. Two scenarios were investigated and are presented. In the first, the balancer operated in the same configuration as in Chapter 5 (i.e., discharging the capacitor C_2 and charging C_1 and C_3 by turns). However, the control algorithm was improved. The balancer operated with a variable switching frequency, and therefore, the AC ripple of the DC source current was minimised by correctly storing the energy in capacitors C_1 and C_3 of the DC-link. The simulation and experimental results are presented. The second scenario analysed the balancer that was connected to a five-level NPC inverter. Capacitors C_1 and C_2 were the DC-link of the inverter, while capacitor C_3 was the energy storage for the AC component of power. The simulation results are presented for this scenario.

6.1. Power decoupling in a system with a single-phase inverter

When connected to the utility grid, single-phase AC-DC and DC-AC power converters often face the phenomenon of an instantaneous power imbalance. Without the appropriate compensation, a ripple second harmonic of power can propagate to the DC circuitry of the system. This could result in a number of problems [6.1]-[6.4]: reduced performance and efficiency, shortened battery lifespan, or decreased PV power production by disturbing the MPPT algorithms.

This decoupling can be realized in a passive or active manner. The passive method uses additional capacitive components that have a value that is high enough to filter out the ripple second harmonic power [6.2]-[6.4]. These are often oversized – from the system perspective – electrolytic capacitors, which are known for their unreliability and high failure rate. The active methods constitute a wide area of research [6.1]-[6.12]. They introduce an extra switching circuit that has dedicated control algorithms of different kinds: dependent or independent, closed or open-loop, and energy storage components: inductive or capacitive.

The power decoupling principle is presented in [6.12] in a very convenient way. The research implies that the energy that is required to compensate for the power imbalance in each decoupling cycle (10[ms] for 50[Hz] grid) can be expressed as

the difference between the maximum and minimum energy of the decoupling capacitor:

$$\Delta W = \frac{1}{2} C (U_{Cmax}^2 - U_{Cmin}^2) = \frac{P_{ac}}{\omega} \tag{6.1}$$

6.2. The SCABC with an active decoupling control as the front-end converter of the seven-level NPC inverter

From the results of the research presented in Sections 5.3.2 and 5.3.3, it can be observed that the current of the DC source contains a variable component of double line (output) frequency. Figure 6.1 presents the relevant waveforms in which the DC source current varies from 0 to approximately 13[A]. This fact was also confirmed in the experiments, which are presented Figure 5.27.

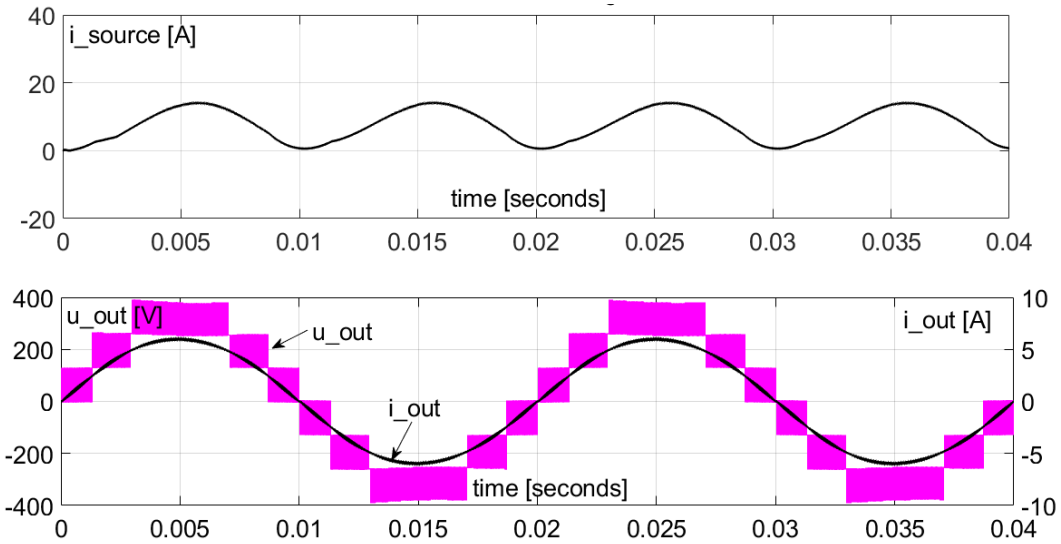


Figure 6.1: The waveforms of the current of the DC source and the voltage and current of the NPC inverter output [P.3].

Because the balancer in the boosting mode that was investigated in Section 5.3 transfers energy to capacitors C_1 and C_3, it was assumed that by controlling the amount of energy that is transferred, the AC component of the supplying current can be compensated. The amount of energy that is transferred can be controlled by the switching frequency as is confirmed by equation (3.10). The function that determines the switching frequency and thus the balancer`s power should have an inverse character compared to the amount of the output power of the NPC inverter. In other words, when the output power reaches its peak value, the charging rate of C_1 and C_3 should be the lowest. When the inverter output power decreases, the current that is drawn from the DC source, C_1 and C_3 are charged with a higher

energy ratio. When such a convention is introduced, capacitors C_1 and C_3 store the instantaneous energy and the double frequency component in the DC source current is reduced.

The control algorithm for the active decoupling must determine the maximum of output power to operate correctly. However, for constant output frequency grid inverters, this can be achieved by the zero-crossing detection of the output voltage. This retains a relatively simple, semi-open control loop. To operate the balancer, the control method presented in Section 5.3.1 was used but was extended with a switching frequency reference block. A diagram of the block is presented in Figure 6.2. As can be seen in Figure 6.1, the maximum value of the DC source current is phase shifted compared to the output current of the NPC by ~2π/3[rad]. This phase-shift is introduced to the reference signal, and therefore, the minimum of the switching frequency aligns with the maximum of the DC current that is being drained from the source.

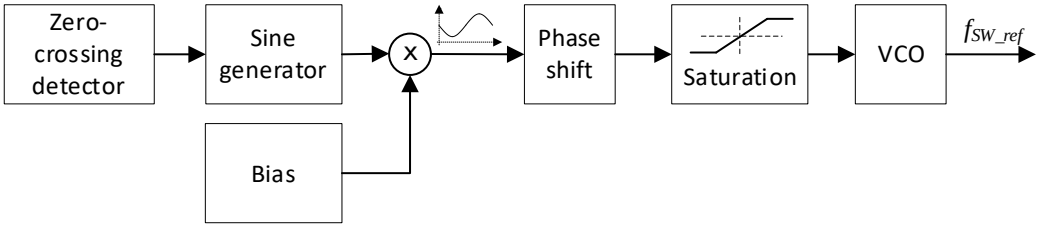


Figure 6.2: Block diagram of the switching frequency reference for the SCABC with power decoupling

The *sine generator* block produces a synchronised sine wave with an amplitude of 0.65 biased by 0.1. This sine signal is then subtracted from *bias* signal with a constant value of 1. The resulting reference signal is limited to 1 by the *saturation* block. The normalised switching frequency reference waveform is presented in Figure 6.3. The values for the reference signal were determined in a simulation study by searching for the smallest AC component in the DC current source.

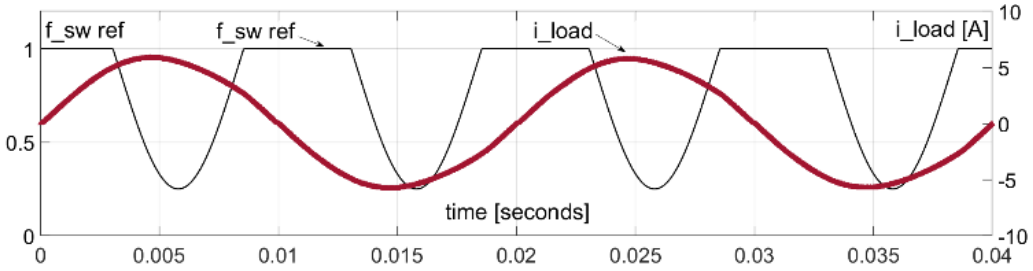


Figure 6.3: Normalised reference switching frequency for the balancer with the output current of the NPC inverter.

For the following study, it was assumed that the voltage across the charged capacitors C_1 and C_3 must not drop below U_{C1min} = 100[V]. The maximum voltage was determined by the DC supply voltage and was equal to U_{C1max} = 133[V]. For the average output power P_{out} = 1000[W], the AC energy in a half period was obtained as an integral of the AC output power:

$$p_{out\_AC} = 1000\sin(618t) \Rightarrow W_{AC} = 1000\left(\frac{1}{618}\right)\cdot 2 = 3.24[\mathrm{J}] \qquad (6.2)$$

The C_1 and C_3 capacitors must have the following capacitance in order to store half (as shown in Figure 5.12) of the total AC energy – using Equation (6.1):

$$C \geq 2\frac{W_{AC}/2}{(U_{Cmax}^2 - U_{Cmin}^2)} \qquad (6.3)$$

The minimum capacitance to meet the voltage ripple requirements was C = 421[μF]. For the research that was conducted, the capacitance of C_1 and C_3 was 500[μF] for the simulations and 470[μF] during the experiment.

6.2.1. Simulation and Experimental Results

The configuration of the device under test is the same as in Section 5.3. The details are presented in Figure 5.13 and Table 5.2.

The simulation results presented in Figures 6.4 to 6.9 offer insight into the voltages and currents of the series-connected capacitors, the current and voltage of the switched capacitor C_S, the current of the inductors L_1 and L_2 and the output waveforms of the NPC inverter: voltage and current as well as the current that was being drawn from the DC power supply.

The results of the experiment are presented in Figures 5.26 to 5.28. The waveforms of the voltage and current of the switched capacitor, the currents of the resonant chokes, the output voltage of the inverter as well as the DC source current are presented.

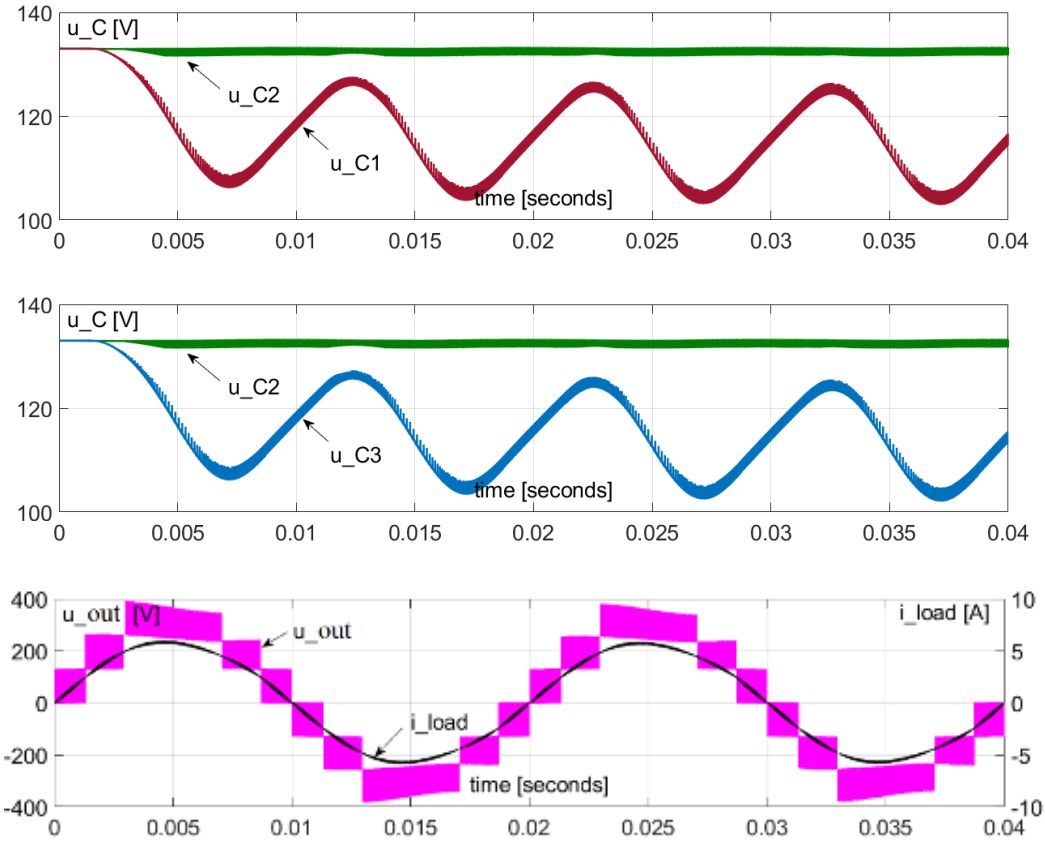


Figure 6.4: The balancer operation with variable frequency. The waveforms of the voltages of the DC-link capacitors C_1, C_2, C_3 as well as the output voltage and current of the NPC inverter. A time frame of two periods of the inverter`s output, 50Hz signal [P.3].

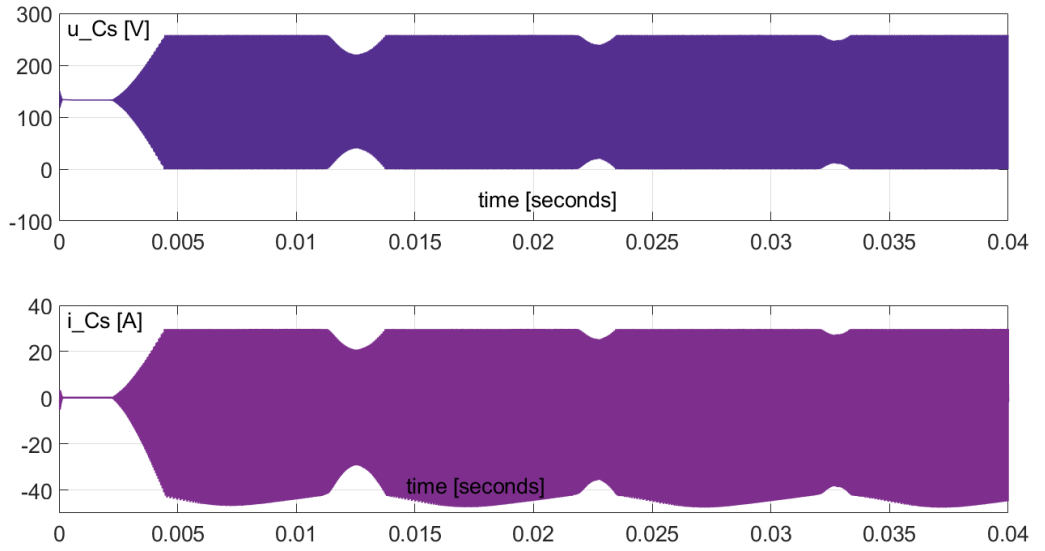


Figure 6.5: The balancer operation with variable frequency. The switched capacitor C_S voltage and current. A time frame of two periods of the inverter`s output, 50Hz signal [P.3].

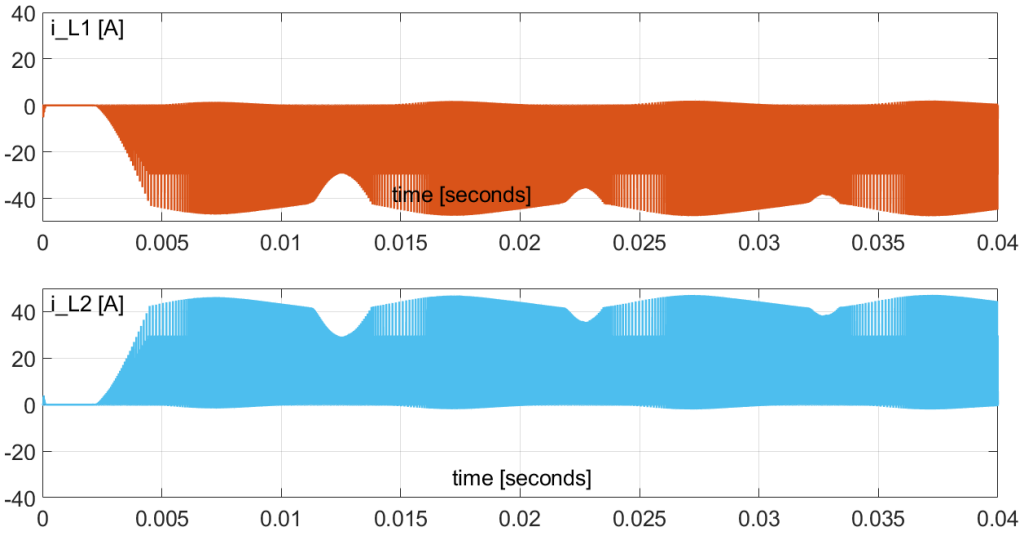


Figure 6.6: The balancer operation with variable frequency. The inductor L1 and L2 current. A time frame of two periods of the inverter's output, 50Hz signal [P.3].

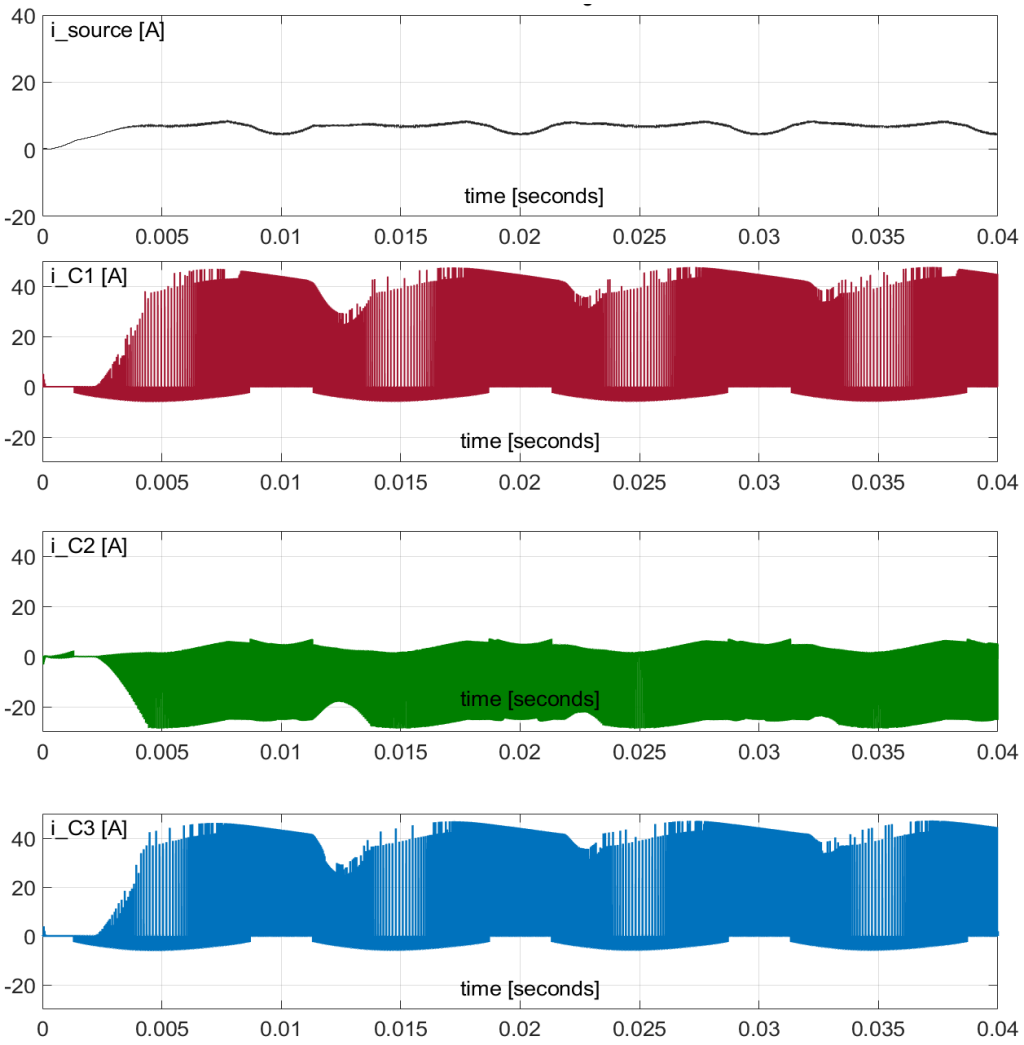


Figure 6.7: The balancer operation with variable frequency. The current of the DC power source and the currents of the series-connected capacitors C_1, C_2, C_3. A time frame of two periods of the inverter`s output, 50Hz signal [P.3].

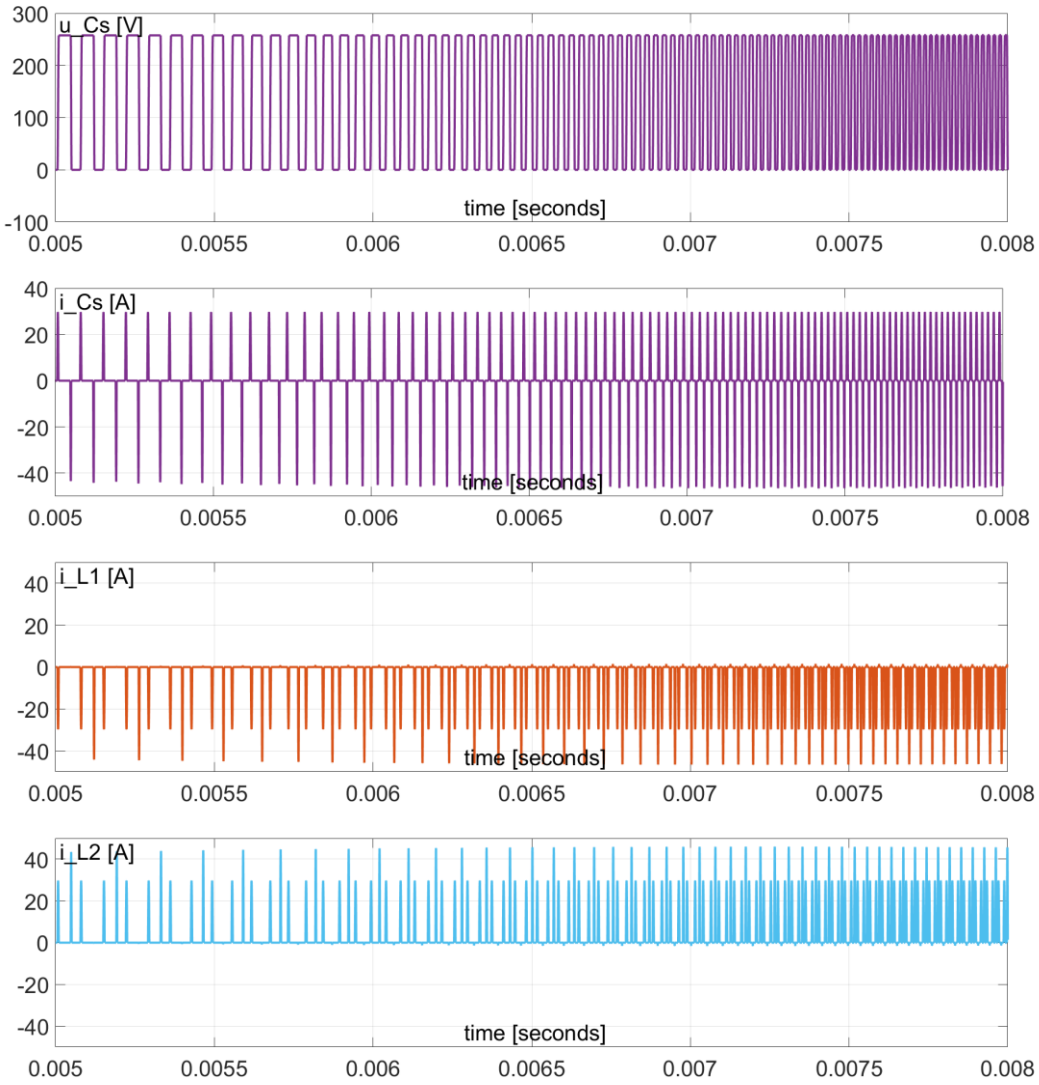


Figure 6.8: The balancer operation with variable frequency. The steady-state waveforms the balancer`s resonant branch: C_S and $L_{1,2}$. A time frame of 3[ms] [P.3].

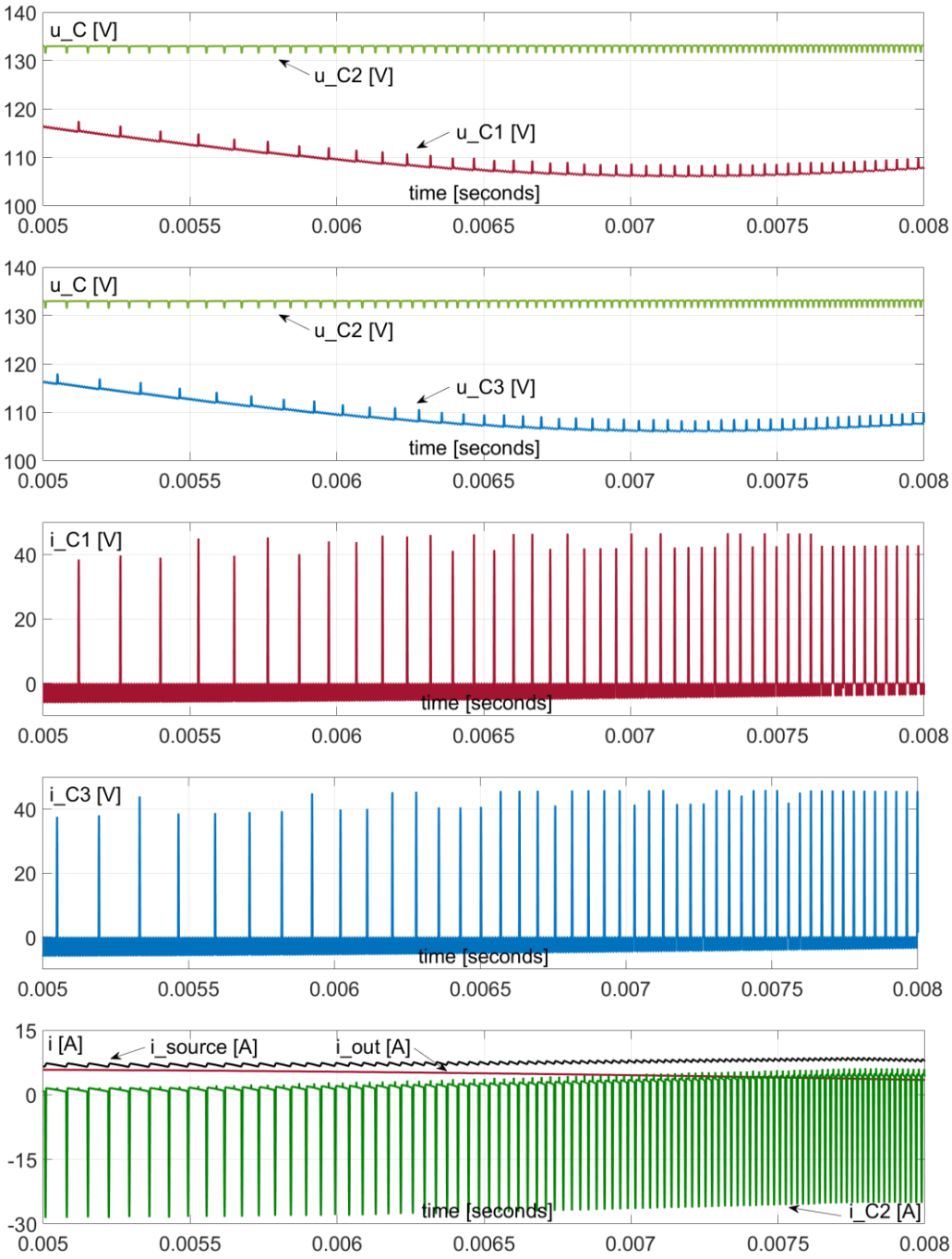
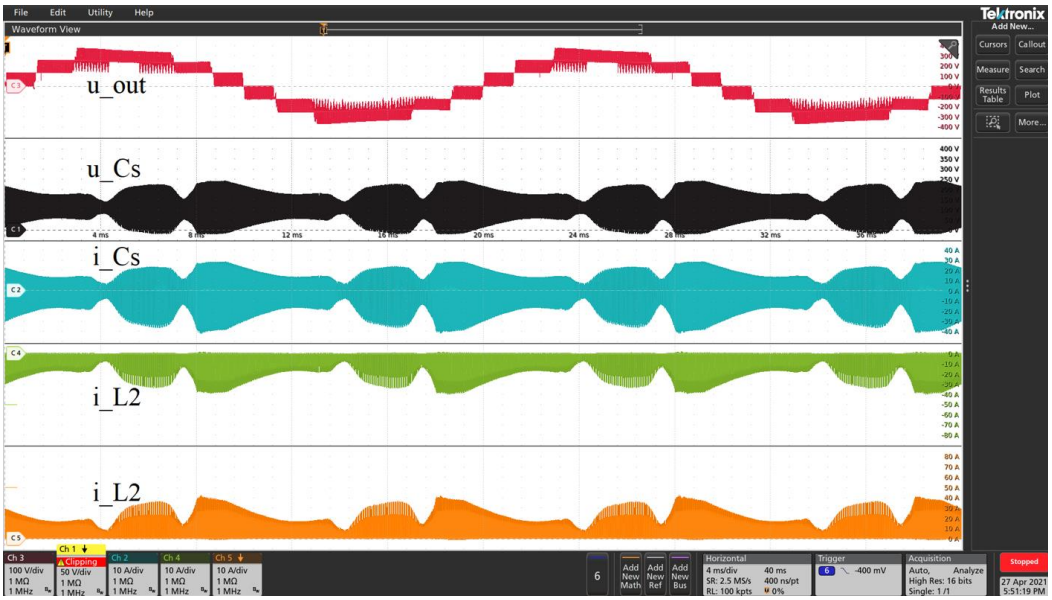


Figure 6.9: The balancer operation with variable frequency. The steady-state waveforms of the balancer and the NPC inverter: voltages of the series-connected capacitors, the currents of charged capacitors C_1 and C_3, the current of the DC source, discharged capacitor C_2 and the output current of the NPC inverter. A time frame of 3[ms] [P.3].

(a)



(b)

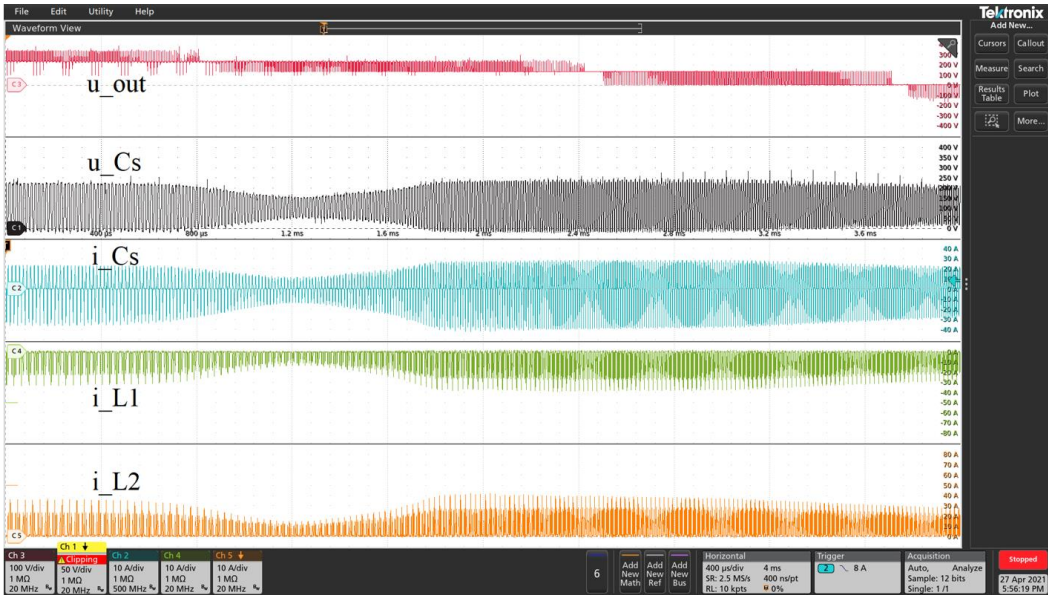


Figure 6.10: Operation of the balancer in the boosting mode and variable frequency for the supply of the NPC inverter. The waveforms of the output voltage of the inverter (100[V/div]), the voltage and current of the switched capacitor (50[V/div], 10[A/div]) as well as the currents of resonant chokes (10[A/div]). (a):4[ms/div], (b):400[µs/div] [P.3].

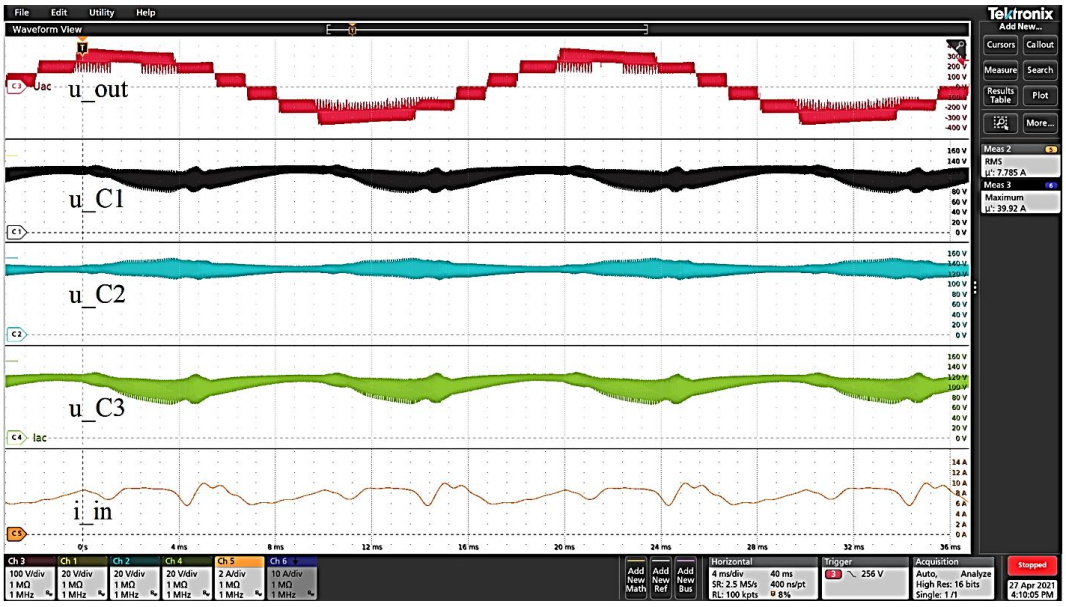


Figure 6.11: Operation of the balancer in the boosting mode and variable frequency for supplying the NPC inverter. The waveforms of the output voltage (100[V/div]), the voltage on the DC-link capacitors (100[V/div]) and the current of the DC power supply that was connected to the C_2 capacitor (2[A/div]) [P.3].

6.2.2. Results summary

Using the proposed control approach, the SCABC successfully boosted the supply voltage three-fold and decoupled the ripple second harmonic of power. The AC component of double grid frequency in supply current was minimised. A comparison of the DC source waveforms is presented in Figure 6.12 for the simulation study. Figure 6.13 presents a comparison of the waveforms that were recorded in the experiment. The double grid frequency component was observed in the voltages of the DC-link capacitors C_1 and C_3 as they provided the storage for the instantaneous energy – Figures 6.4 and 6.11.

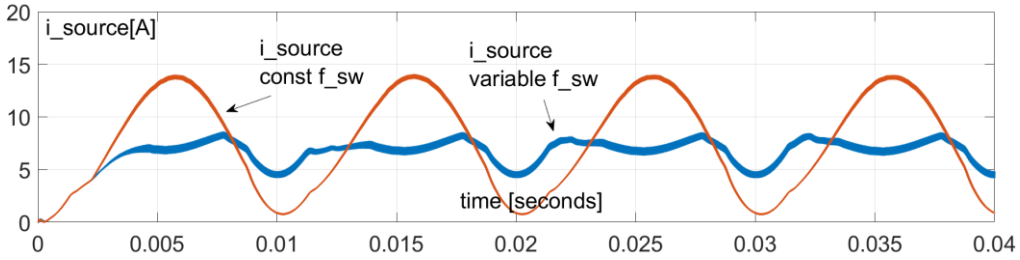
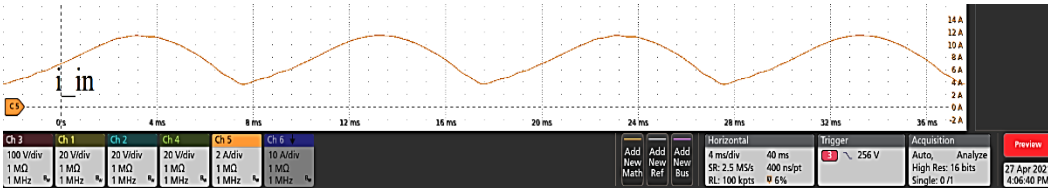


Figure 6.12: The DC source current when the AIVB was operating with a constant switching frequency and variable frequencies according to the reference presented in Figure 6.3. A comparison of the simulation results [P.3].

(a)



(b)

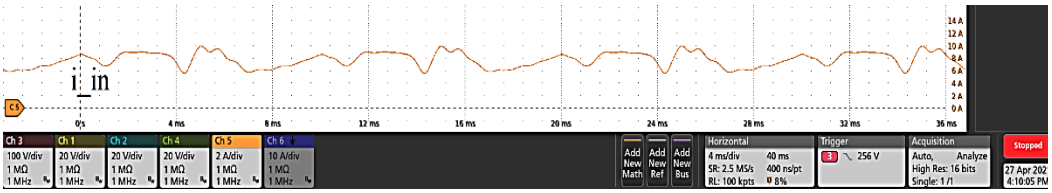


Figure 6.13: Comparison of the experimental results. The DC source current when the AIVB was operating with a constant switching frequency (a) and variable frequency (b) according to the reference presented in Figure 6.3.

6.3. The SCABC with an active power decoupling control as the front-end converter of a five-level NPC inverter composed of three-level legs

This research investigated the possibility of compensating for the variable power component using capacitor C_3 while C_1 and C_2 were supplied from the DC source and formed the DC-link for a five-level NPC inverter (bridge NPC inverter with three-level branches). The diagram of such a configuration is presented in Figure 6.14.

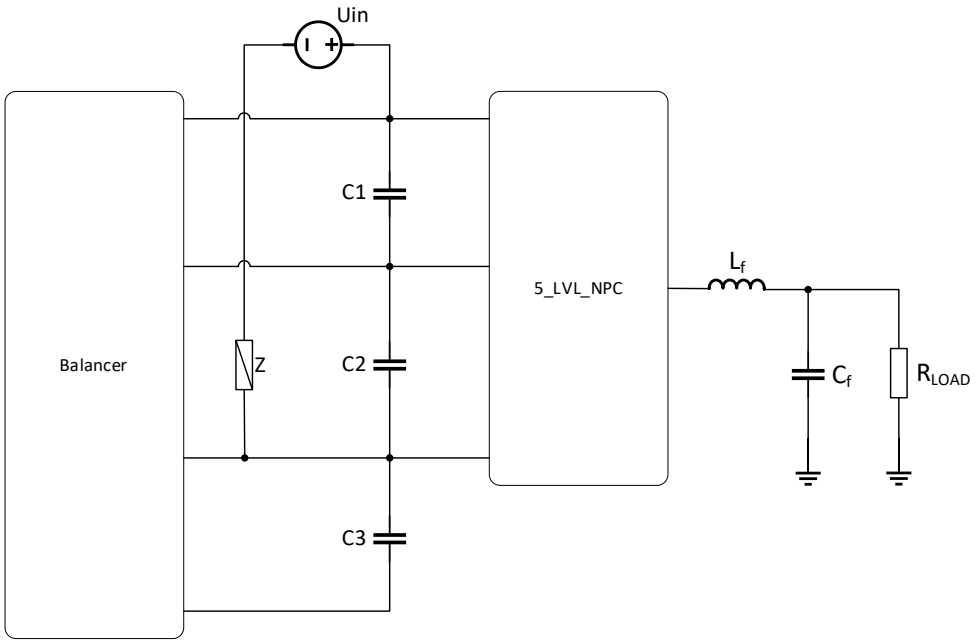


Figure 6.14: The SCABC concept as a front converter with an active decoupling

control for a five-level NPC inverter. The DC source that was connected to the C_1 and C_2 capacitors.

The control of the system presented in Figure 6.15 cause the energy storage (capacitor C_3) to be charged when the energy that is being transferred by the NPC inverter is low. On the other hand, when the energy that is being drained from the DC supply source is high, the control causes the capacitor C_3 to be discharged and the DC-link capacitors to be charged in order to support the power source. In addition, the voltages of the capacitors C_1 and C_2 must be maintained in a balanced state, and therefore, the control logic must determine which of these capacitors must be charged or discharged. The proposed active balancing method is of a closed-loop type. A block diagram of the control loop is presented in Figure 6.15. Measuring of the DC source voltage and current as well as the voltages of the series-connected capacitors $C_{1...}C_3$ is required. The mean value of the source power P_{source} was calculated and provides a reference.

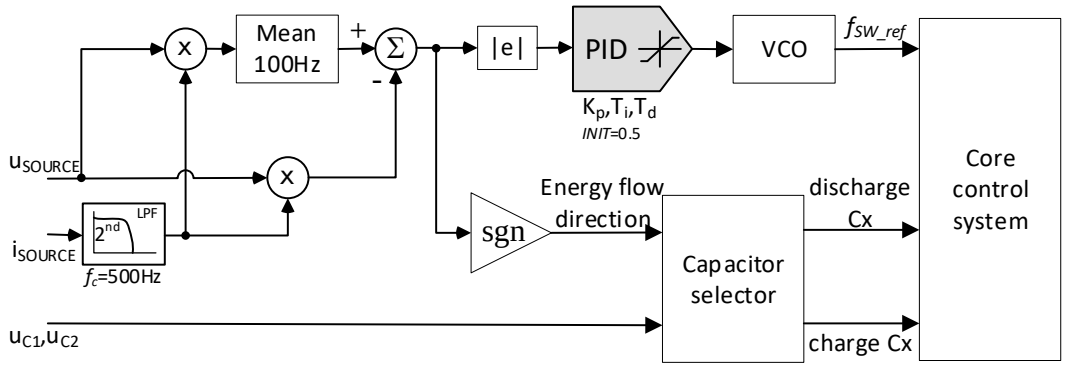


Figure 6.15: The block diagram of the control algorithm for active power decoupling in the system composed of the SCABC and the five-level NPC inverter.

The *capacitor selector* block, presented in the diagram in Figure 6.15 reads the *energy flow direction* signal, and the decision is made to either charge or discharge the capacitor C_3. With the voltages across capacitors C_1 and C_2 is measured, the control algorithm decides which of them participates in the energy exchange process. Thus, the balance of the voltages of C_1 and C_2 is maintained. The SCABC operated at variable switching frequency.

6.3.1. Simulation setup and results

The simulation model for the research of the system presented in Figure 6.14 was developed in the MATLAB®/Simulink® environment. Detailed information on the parameters of the simulation model is provided in Table 6.1. The control part

of the model is presented in Figure 6.16. The *PID* controller was tuned using the built-in Simulink tool: Frequency Response Based PID Tuner. The simulation results presented in Figures 6.17 to 6.20 offer insight into the voltages of the series-connected capacitors, the current and voltage of the switched capacitor C_S, the current of the inductors L_1 and L_2 and the output waveforms of the NPC inverter: voltage and current. Moreover, the current that is being drawn from the DC power supply and the output of the *PID* controller are also presented.

Table 6.1: The simulation parameters of the SCABC with active power decoupling and a five-level NPC inverter.

Switched capacitor	C_S	250[nF]
Inductance	L_1, L_2	2x3[μH]
DC-link capacitors	C_1 , C_2	500[μF]
	C_3	100[μF]
DC source	U_{in}	375[V]
Parasitic resistance	R_{PR}	80[mΩ]
Maximum switching frequency	f_{SW}	110[kHz]
Dead-time	t_d	100[ns]
On-state resistance of transistors	R_{DS_on}	20[mΩ]
Inverter output power	P_{out}	1 [kW]; 1[kVA], $cos\varphi$ = 29.2[deg]
Output filter parameters	L_f , C_f	500[μH]; 47[nF]
PID controller	K_P , T_i , T_d	0.38732; 0.524; 0.00106

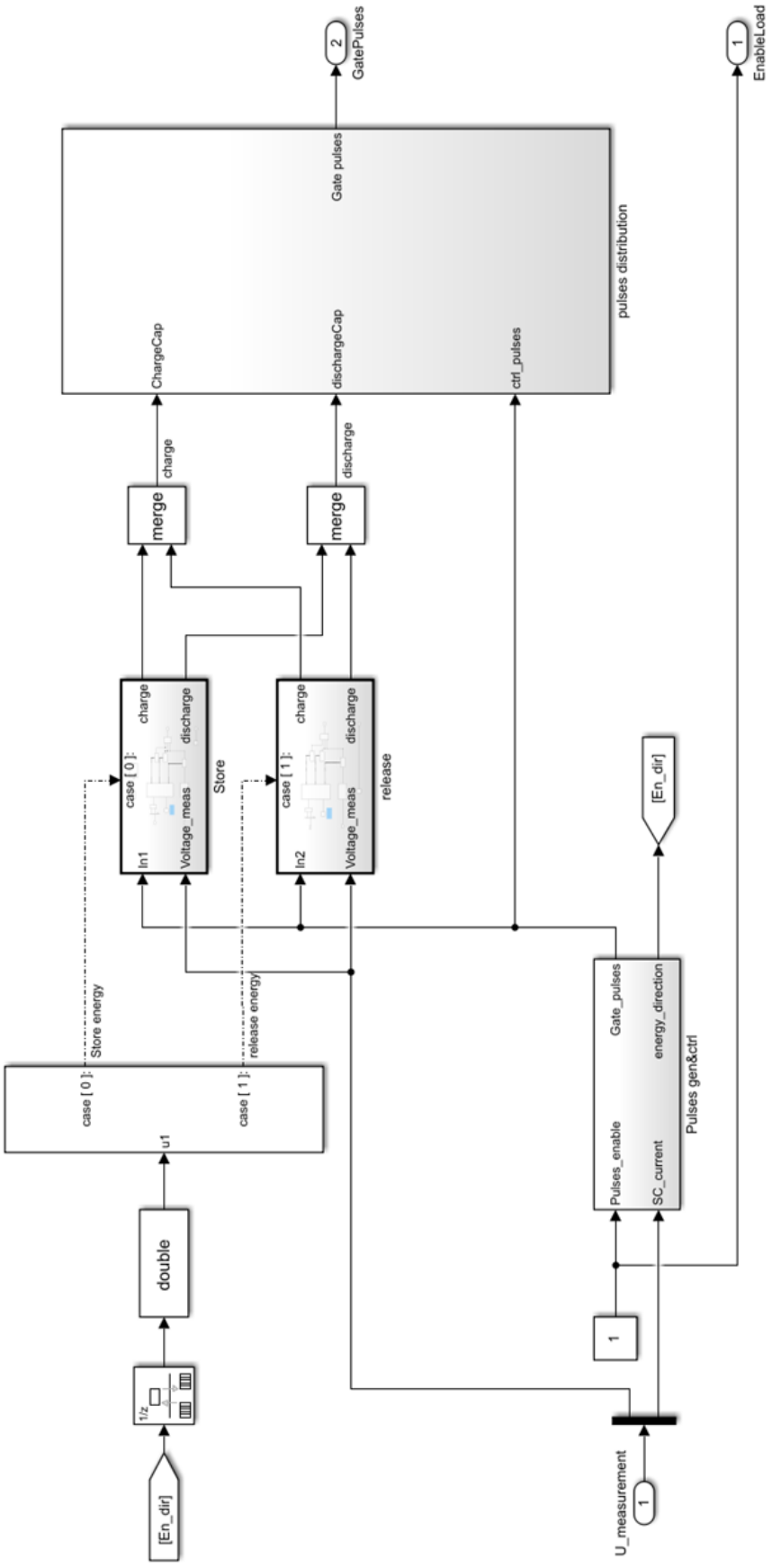


Figure 6.16: The control system implementation in MATLAB®/Simulink® for an SCABC with active power decoupling for a five-level NPC inverter

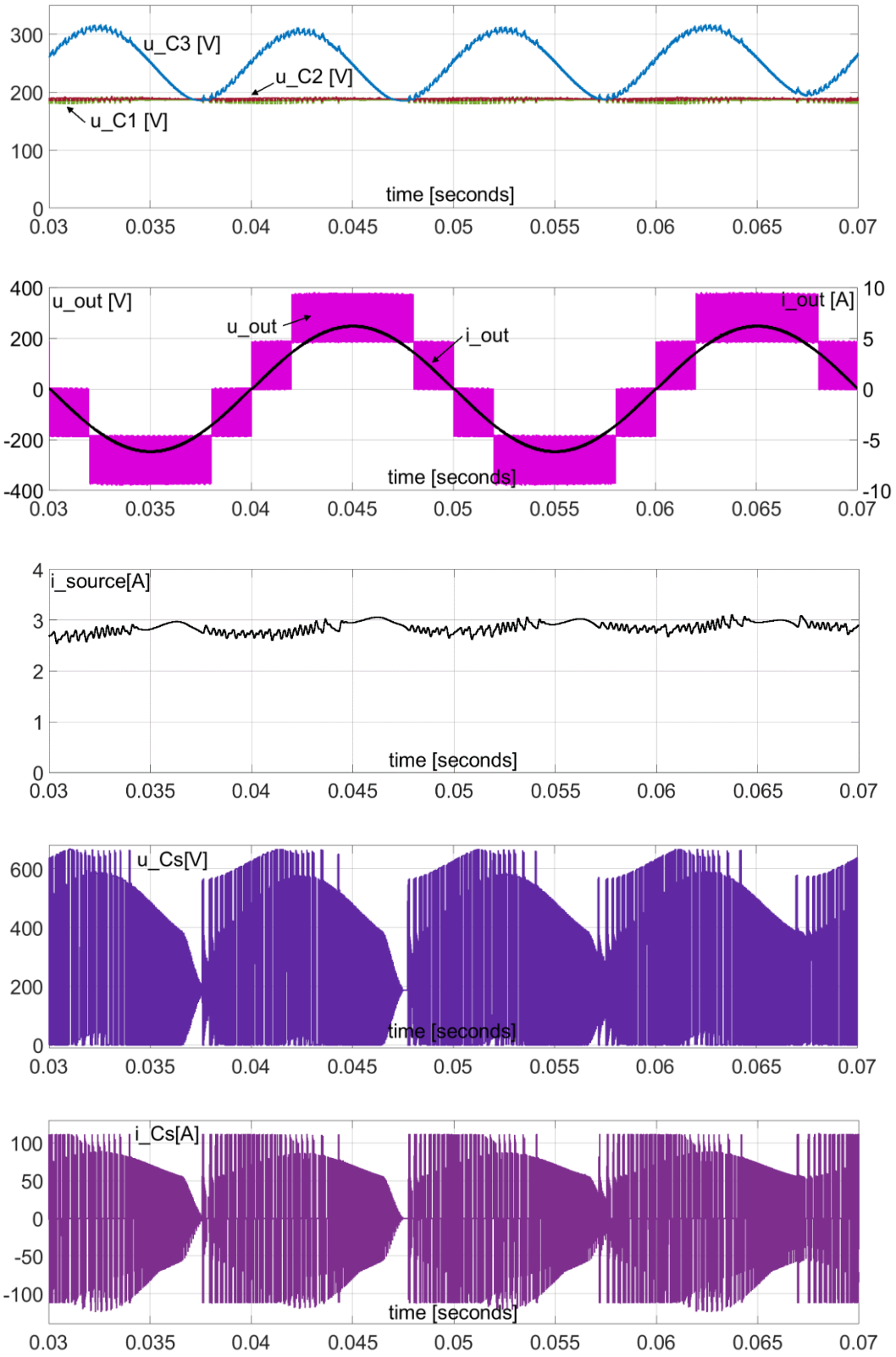


Figure 6.17: The balancer steady-state operation with active power decoupling. The waveforms of the voltages of the DC-link capacitors C_1, C_2, storage capacitor C_3, output voltage and current of the NPC inverter, the current of the DC source, the voltage and current of the switched capacitor C_S. A time frame of two periods of the inverter`s output, 50[Hz] signal.

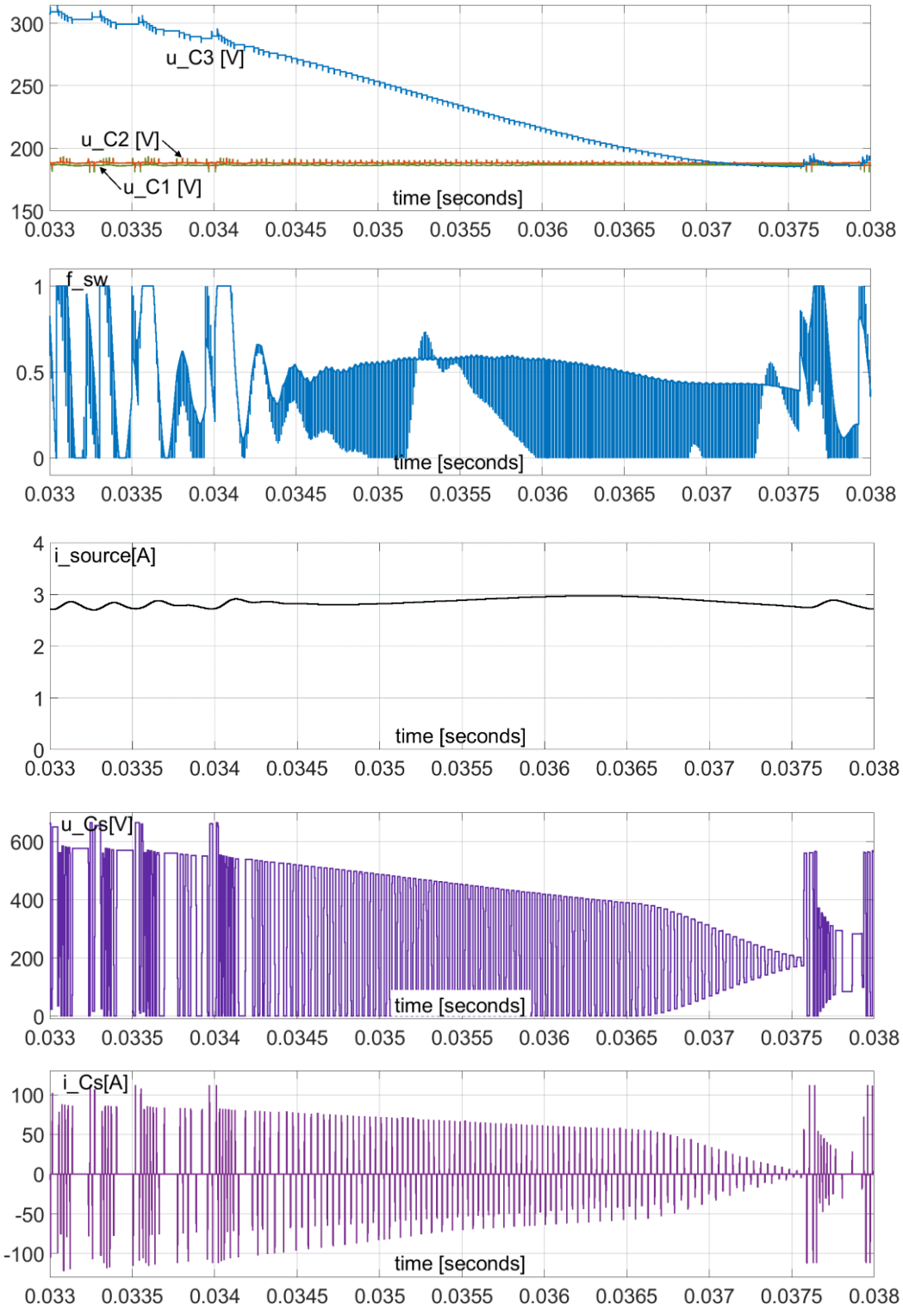


Figure 6.18: The balancer steady-state operation with active power decoupling. The waveforms of the voltages of the DC-link capacitors C_1, C_2, storage capacitor C_3, the normalised switching frequency, the current of the DC source, the voltage and current of the switched capacitor C_S. A time interval of 5[ms].

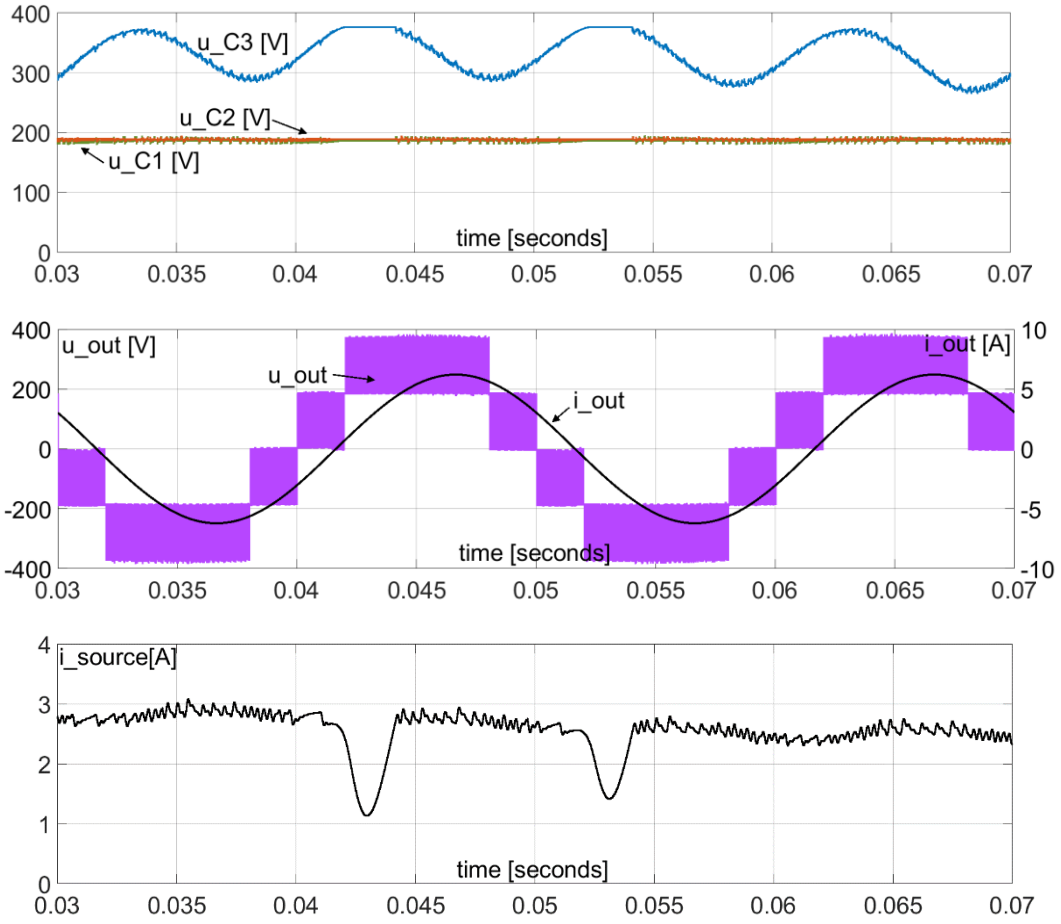


Figure 6.19: The balancer steady-state operation with active power decoupling. The waveforms of the voltages of the DC-link capacitors C_1, C_2, storage capacitor C_3, the output voltage and current of the NPC inverter, the current of the DC source. A time frame of two periods of the inverter`s output, 50[Hz] signal. Output power 1[kVA], $cos\varphi$ = 29.2[deg].

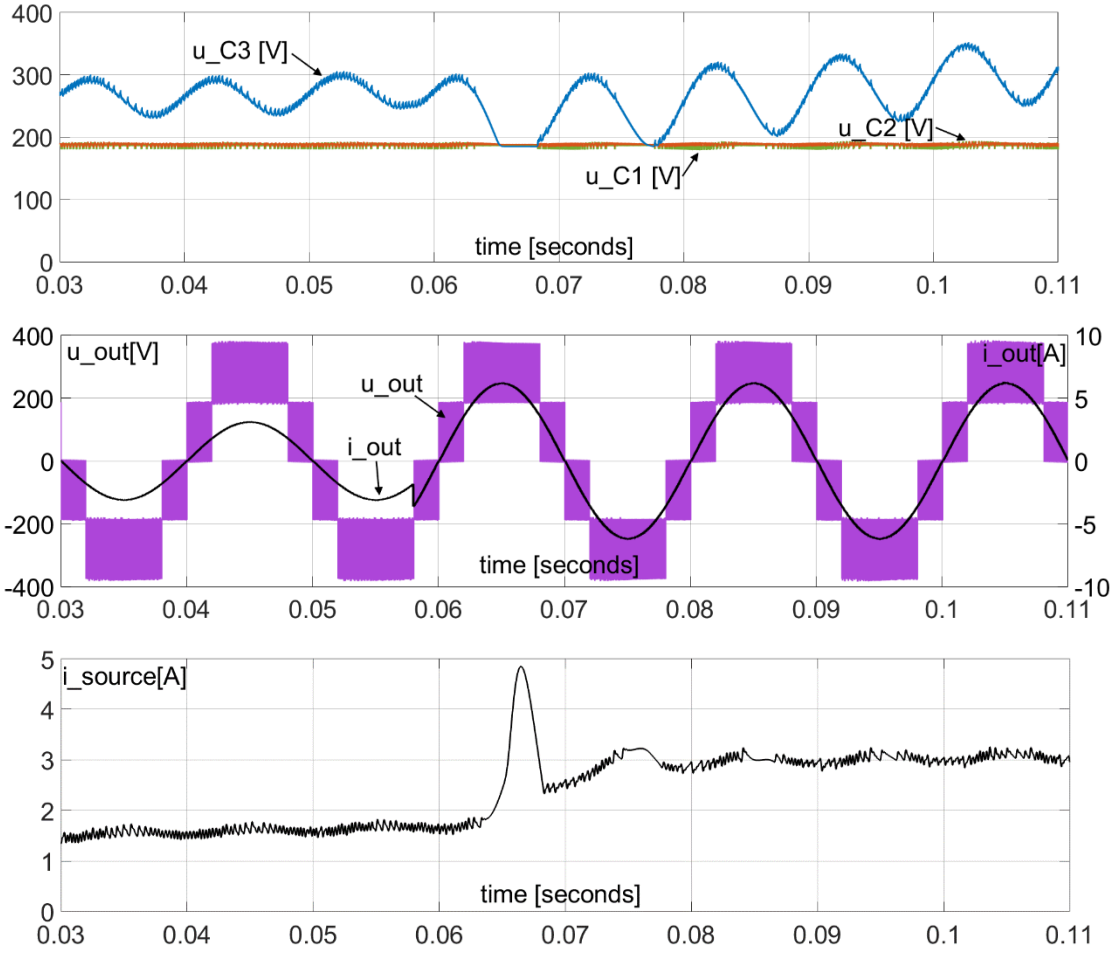


Figure 6.20: The balancer dynamic-state operation with active power decoupling. The waveforms of the voltages of the DC-link capacitors C_1, C_2, storage capacitor C_3, the output voltage and current of the NPC inverter, the current of the DC source. A time span of four periods of the inverter`s output, 50[Hz] signal. Output power step from 0,5[kW] to 1[kW] at 58[ms].

6.3.2. Research Summary

In the investigated configuration, the SCABC was operated as a DC-link balancer with power decoupling ability for a five-level NPC inverter. The capacitors C_1 and C_2 were the voltage divider for the inverter, whereas capacitor C_3 provided the energy storage for the AC component of the current. The presented figures prove that the circuit operated correctly. The near to DC character of the power source current confirms the effectiveness of the control algorithm that was used. Figure 6.21 presents the supply current with the algorithm active compared to the waveform with the decoupling inactive. The waveforms of the voltages of the series-connected capacitors – u_{C1}, u_{C3}, u_{C3} – show that the energy of the ripple second harmonic power was stored in capacitor C_3.

The capacitance of storage capacitor C_3 was five times smaller compared to the other DC-link capacitors, which was advantageous. For the scenario with a reactive component in output power, the capacitance could be considered to be too large for the circuit needs. The reason are the dips in the source`s current, which are visible in Figure 6.19, where the decoupling capacitor C_3 was already charged to its maximum voltage and the power demand of the NPC inverter was not significant. The setup was also able to handle the step change of the load. The results presented in Figure 6.20 show that the current of the DC source settled in approximately 10[ms], which is half of the period of the output current.

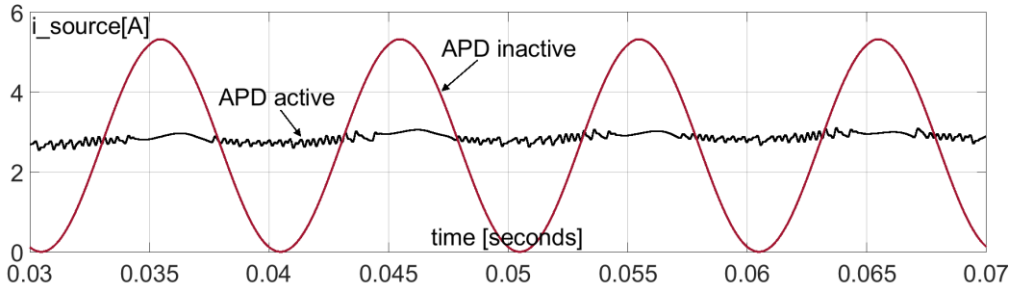


Figure 6.21: Comparison of the DC source current with operative vs nonoperative active power decoupling (APD).

7. Summary and final conclusions

7.1. Dissertation summary

This dissertation presents the analysis, simulation, and experimental investigations of a Switched Capacitor Active Balancing Converter for controlling the voltage sharing on series-connected capacitors. The main body of the dissertation is followed by an analysis of the research that has been published on the subject matter. Moreover, an introduction to the topic of switched capacitor converters is also given.

The preceding chapters present the operation principle and mathematical expressions that describe the proposed circuit. The possible operation modes and basics of converter control are presented as well as the equations for sizing the circuit components. The sources of power losses are elaborated and their effect on the efficiency of the converter is presented. The simulation model as well as the project of the experimental converter are presented. The results of the research are provided and discussed – the concept of the converter was also proven. When the imperfections of the SCABC were revealed, an updated topology was proposed.

The further research undertaken focused on a balancer operating as the front converter of multilevel NPC inverters. Various configurations of the system were investigated in both simulation and experimental models. The research for the dissertation was directed toward developing the control algorithms that are critical for the correct operation of complex systems that are composed of a multilevel inverter and a balancer. Moreover, the research was enhanced by the ability of the SCABC to manage instantaneous power in the power conversion system. Compensation of the ripple of second harmonic power was achieved in the DC-AC system with seven- and five-level NPC inverters.

With the research that was conducted and the results that are presented, it is believed that all of the objectives of this dissertation have been met. Moreover, the theses that were propounded have been confirmed: the proposed switched capacitor converter is able to successfully equalise voltages on three series-connected capacitors. Furthermore, it can operate as the front converter of the multilevel NPC inverter, thereby providing balanced DC-link voltages and a reduced AC component of the supply current.

7.2. Final conclusions

A theoretical analysis of the proposed converter led to the following conclusions:

1. The output power of the balancer was dependent on the capacitance of the C_S capacitor and the value of the input voltage.
2. The power of the balancer was dependent on the switching frequency.
3. The majority of the losses were conduction losses that were associated with the resistances of the circuit`s components: R_{DS_on}, R_{ESR}, R_W and to a forward voltage drop of diodes V_f.
4. The control signals affected the efficiency by matching the switching frequency f_{SW} to the resonant frequency f_{RES} and by the deadtime t_d that was introduced.
5. The hard switching operation was possible and provided limitation of the current of the resonant branch.
6. A high-rate energy exchange operation was also possible: discharge of two capacitors simultaneously.

Proof of concept stage:

1. The results acquired in the simulation and experimental tests are adequately correlated.
2. It was possible to implement all of the proposed operation modes in a real application of the converter.
3. It was possible to introduce a compact and efficient gate driver circuitry using the bootstrap technique.
4. The voltage stresses of the transistors did not exceed half of the supply voltage.
5. With the circuit`s flaws revealed in the experimental tests, an updated and improved topology was developed and presented. Behaviour of the circuit was improved.

The operation of the balancer as a front-converter for a seven-level NPC inverter:

1. The SCABC successfully maintained the equilibrium state of the DC-link voltages.
2. The developed control algorithm was proven in various operation scenarios such as the initialisation with deep DC-link imbalance and a step change of the load.

3. The balancer could operate when only one of the three series-connected capacitors of the DC-link was used. Together with its DC voltage boosting ability, the balancing functionality was maintained.
4. The peak efficiency of the converter that was built using GaN semiconductors was estimated to be 95,4%.

Active power decoupling:

1. When the correct, variable switching frequency control was used, the balancer successfully decoupled the AC component of the power that was being propagated to the DC side of the converter system.
2. In the configuration with a seven-level inverter, the double grid frequency ripple energy was stored in the C_1 and C_3 capacitors. In the operation scenario with the five-level NPC, the storage was accomplished by capacitor C_3.
3. The decoupling was also successful with a reactive component that was present in the output power of the NPC.

7.3. Author`s Achievements and Possible Future Work

The author's major achievements that are included in the dissertation are:

1. Analysis of the newly introduced topology, investigating quality of its waveforms and possible applications as a standalone converter or as a subpart of a complex power conversion system.
2. Analysis of a load of the proposed circuit components and deriving the formulas for sizing those as a function of assumed operation quantities: output power, input voltage, and switching frequency.
3. Analysis and mathematical description of power losses and efficiency for the proposed switched capacitor converter topology.
4. Designing and developing the control algorithms presented in the dissertation, which cover multiple operation modes of an SCABC and include:
    a. solving the problem of decision making on ongoing switching strategy
    b. adjusting to the conditions of variable power in the systems with DC-AC converters

c. synchronization with AC output and elimination of the double frequency ripple
d. Switching strategy for the bootstrap type gate supply

5. Hardware implementation of the control algorithms
6. Designing, assembling, and commissioning the experimental setups that were investigated during the research conducted.

Possible future work:

1. Deriving time-dependent formulas for the topology presented as well as a small-signal model and incorporating it into development process would be beneficial in terms of applications in industry and control design. Much more work needs to be done to fully use the proposed topology for power converters. For example, the efficiency of each operation mode should be calculated and verified by experimental results. The efficiencies of each mode should also be compared.
2. Conducting experimental investigations of an SCABC equipped with other type of semiconductors, such as superjunction (SJ) MOSFETs, thereby providing great $Q_G \cdot R_{DS\_on}$ and $R_{DS\_on} \cdot A$ figures of merit.
3. Conducting experimental investigations for the operation case where closed-loop control with series-connected capacitors voltage measurement is required.
4. Conducting experimental investigations for the operating scenario in which the middle capacitor of the DC-link is supplied directly from a PV array.
5. Developing a compact SCABC converter using planar inductors and SMD semiconductors that can operate in the range of hundreds of kilohertz.

Appendix

Appendix A: List of the equipment that was used during the research:

1. Tektronix THDP0200 Differential voltage probes
2. CWTMini Hf1B Rogowski current waveform transducer
3. Tektronix TCP0030A Current probes
4. Tektronix MSO58 Oscilloscope
5. Tektronix MSO5204 Oscilloscope
6. Motech LPS-305 Power supply
7. Delta SM300-10D Power supplies
8. Yokogawa WT3000 Power analyser
9. WayneKerr 3260B LCR meter
10. Ed-k DPG-10 Power choke tester
11. Altera DE0 FPGA Development kit

Appendix B: Electronic diagrams and printed circuit board project of the improved SCABC.

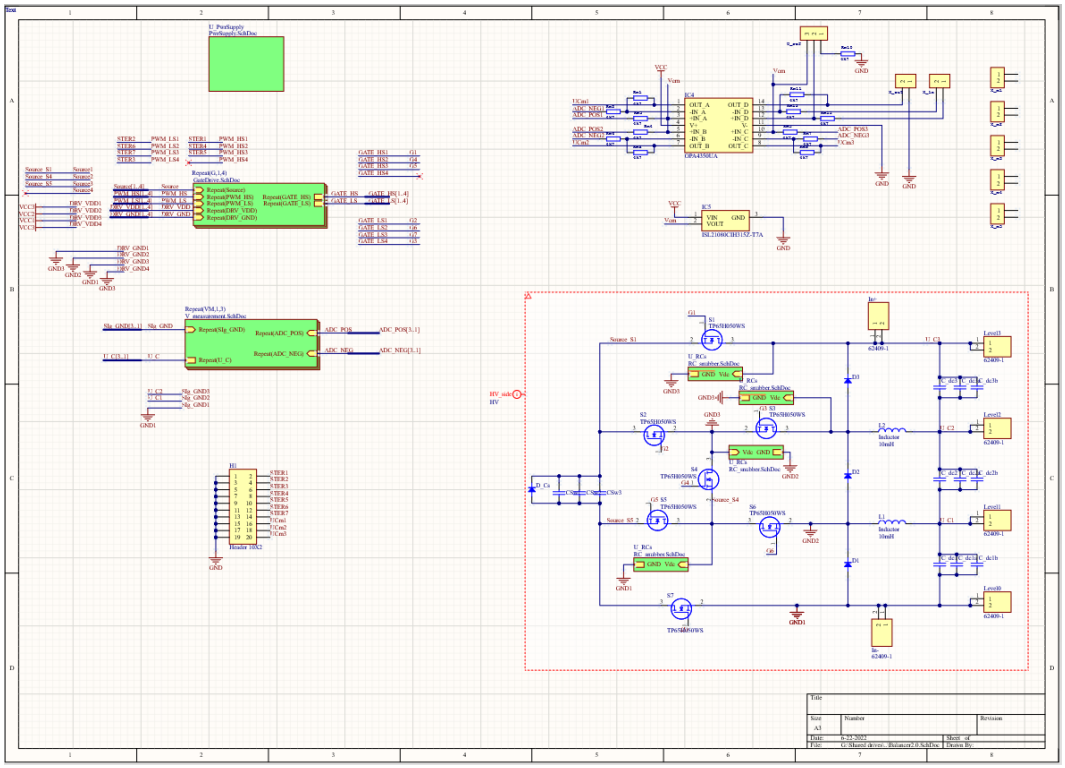


Figure B.1 The master electronic diagram of the improved SCABC circuit.

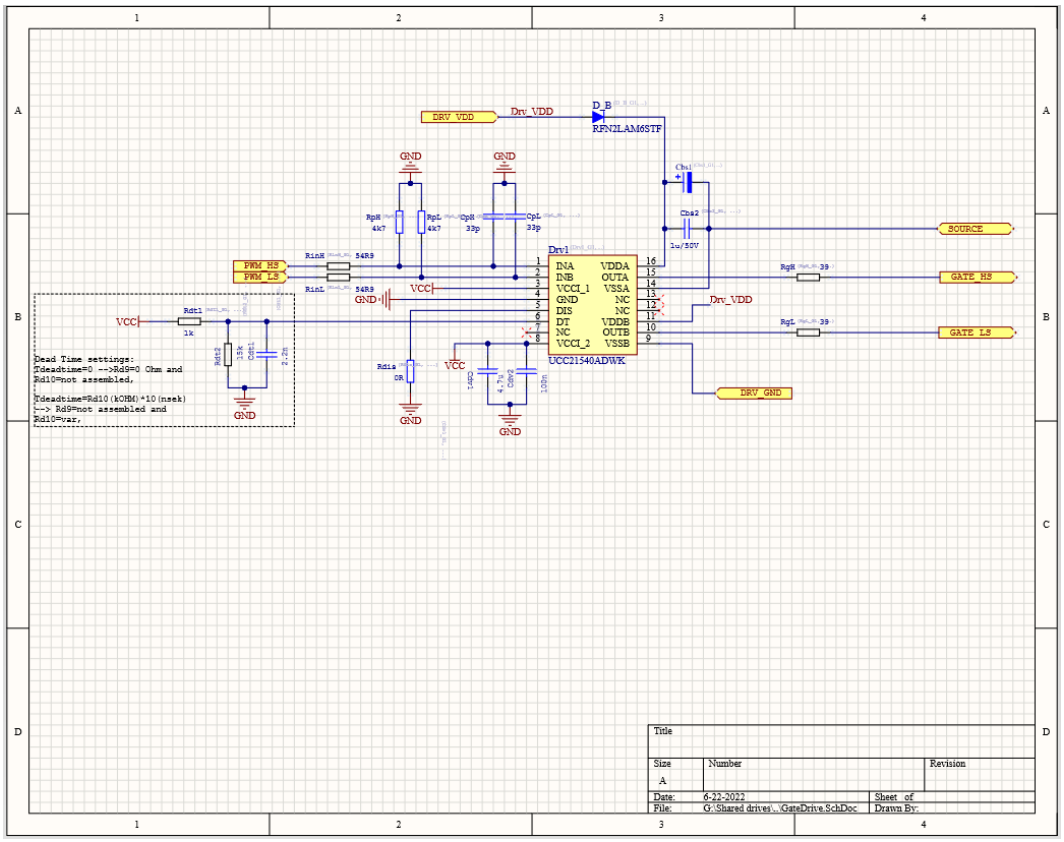


Figure B.2 Electronic diagram of the gate-driver circuit.

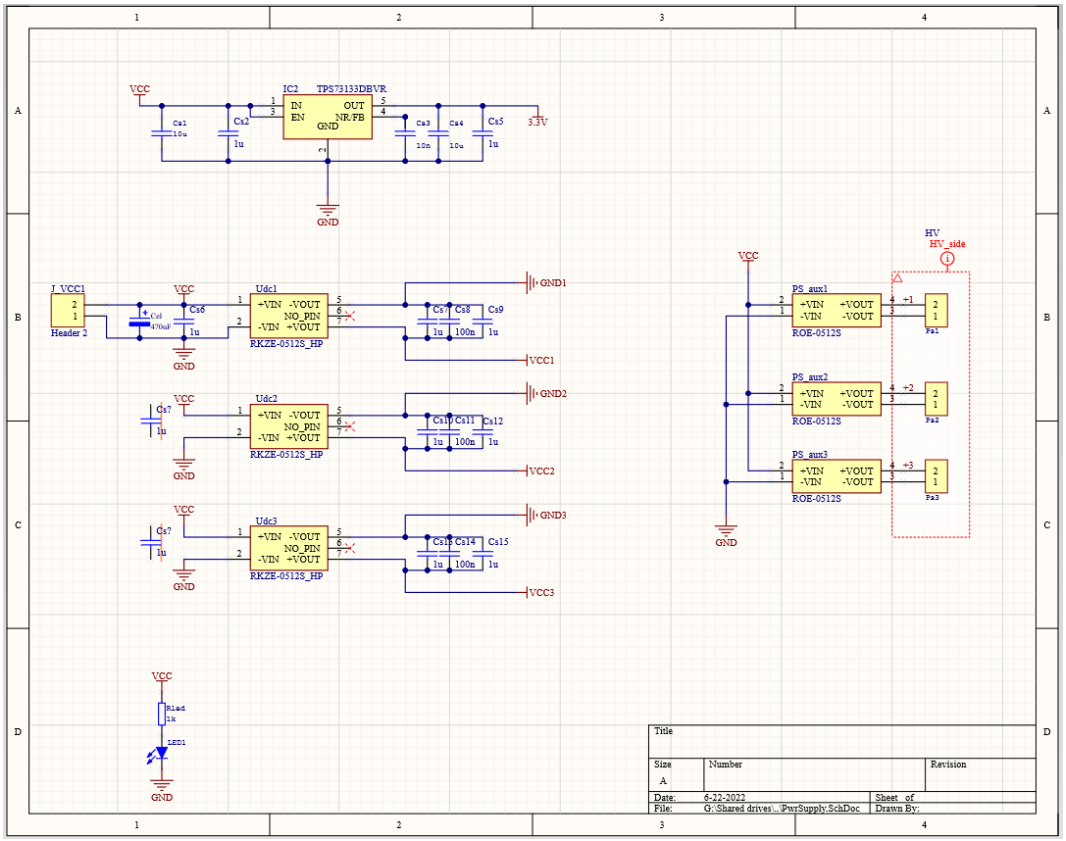


Figure B.3 Electronic diagram of the power supply circuit

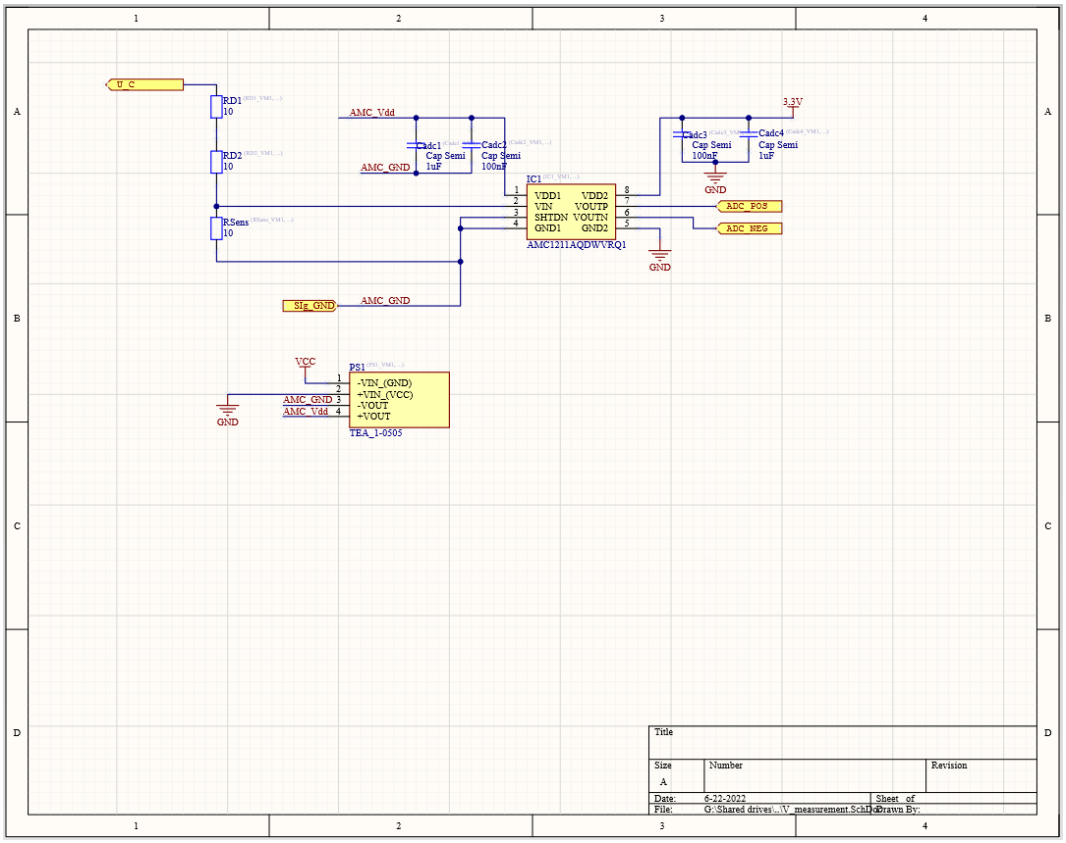
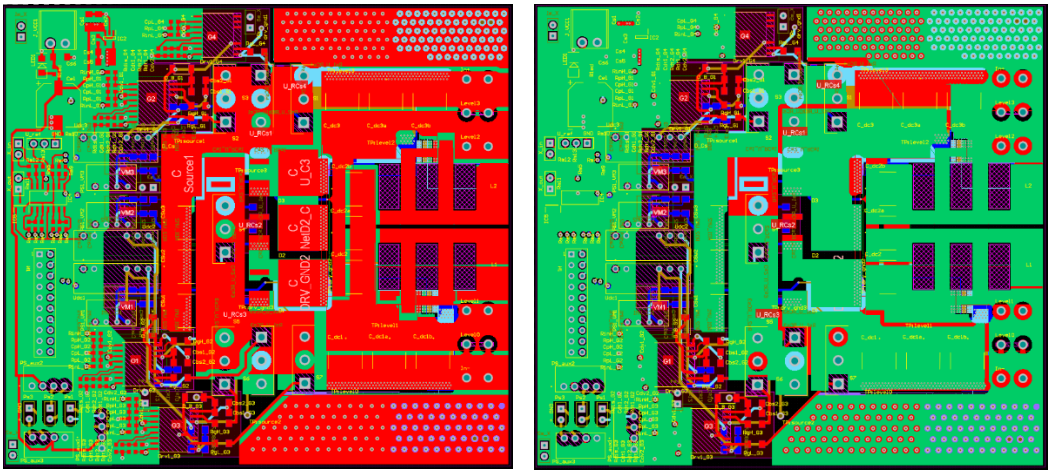
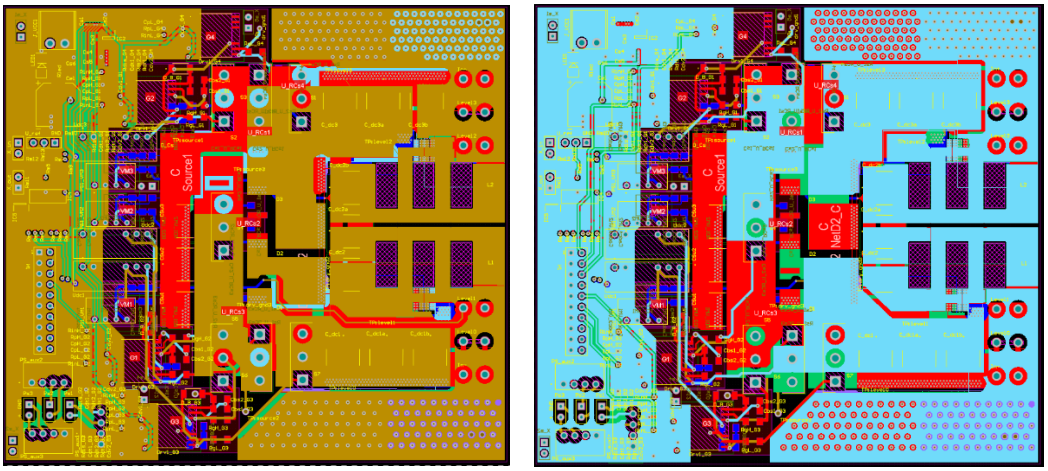


Figure B.4 Electronic diagram of the voltage measurement stage.

a) b)



c) d)



e) f)

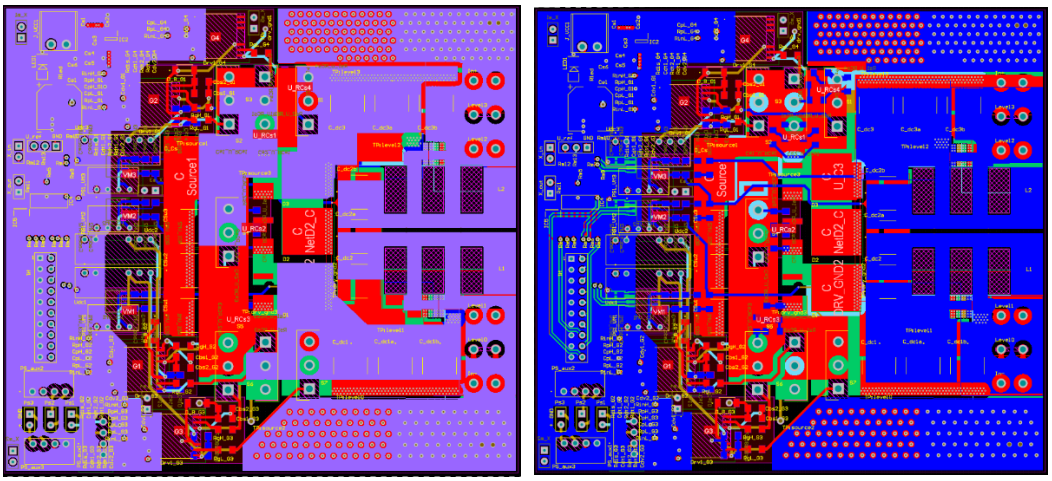


Figure B.5 The designed printed circuit board in which Figures a) to f) correspond to the copper layers 1 to 6.

References

[1.1] BP Statistical Review of World Energy 2021 | 70th edition (Accessed March 2022)

[1.2] https://www.ncdc.noaa.gov/sotc/global/2021 (accessed March 2022)

[1.3] State of the Climate in 2020 J. Blunden1 and T. Boyer2 (Accessed March 2022)

[1.4] Oil Information 2019; International Energy Agency https://doi.org/10.1787/553cdfcc-en (Accessed March 2022)

[1.5] Renewables 2021, Global Status Report, UN Environment Programme (Accessed March 2022)

[1.6] OECD (2022), Renewable energy (indicator). doi: 10.1787/aac7c3f1-en (Accessed March 2022)

[1.7] Global Market Outlook 2021-2025 https://www.solarpowereurope.org/ (accessed May 2022)

[1.8] Renewables 2020: Solar PV ; International Energy Agency (accessed May 2022)

[1.9] https://www.pv-magazine.com/2020/10/01/worlds-largest-solar-plant-goes-online-in-china/ (accessed May 2022)

[1.10] Rodriguez J., Franquelo L.G., Kouro S., Leon J.I., Portillo R.C., Prats M..M., Perez M.A., Multilevel converters: An enabling technology for high-power applications, Proceedings of the IEEE, 97(11), 1786–1817, 2009, ISSN 0018-9219, URL http://dx.doi.org/10.1109/JPROC. 2009.2030235.

[1.11] Wang C., Li Y., A survey on topologies of multilevel converters and study of two novel topologies, Power Electronics and Motion Control Conference, 2009. IPEMC ’09. IEEE 6th International, 860 – 865, 2009, URL http://dx.doi.org/10.1109/IPEMC.2009.5157505.

[1.12] Jose Rodriguez, Senior Member, IEEE, Steffen Bernet, Member, IEEE, Peter K. Steimer, Fellow, IEEE, and Ignacio E. Lizama, A Survey on Neutral-Point-Clamped Inverters, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 57, NO. 7, JULY 2010

[1.13] L. Zhang, K. Sun, L. Feng, H. Wu and Y. Xing, "A Family of Neutral Point Clamped Full-Bridge Topologies for Transformerless Photovoltaic Grid-Tied Inverters," in IEEE Transactions on Power Electronics, vol. 28, no. 2, pp. 730-739, Feb. 2013. doi: 10.1109/TPEL.2012.2205406.

[1.14] M. Trabelsi, H. Vahedi and H. Abu-Rub, "Review on Single-DC-Source Multilevel Inverters: Topologies, Challenges, Industrial Applications, and Recommendations," in IEEE Open Journal of the Industrial Electronics Society, vol. 2, pp. 112-127, 2021.

[1.15] M. N. H. Khan, M. Forouzesh, Y. P. Siwakoti, L. Li, T. Kerekes and F. Blaabjerg, "Transformerless Inverter Topologies for Single-Phase Photovoltaic Systems: A Comparative Review," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 1, pp. 805-835, March 2020.

[1.16] A. Salem, H. Van Khang, K. G. Robbersmyr, M. Norambuena and J. Rodriguez, "Voltage Source Multilevel Inverters With Reduced Device Count: Topological Review and Novel Comparative Factors," in IEEE Trans. on Power Electronics, vol. 36, no. 3, pp. 2720-2747, March 2021.

[1.17] Z. Zhang, J. Zhang, S. Shao and J. Zhang, "A High-Efficiency Single-Phase T-Type BCM Microinverter," in IEEE Transactions on Power Electronics, vol. 34, no. 1, pp. 984-995, Jan. 2019.

[1.18] Manel Hlaili1, Hfaiedh Mechergui1, Henrique Gonçalves2, Bruno Exposto2, João L. Afonso2, Single Phase NPC Inverter Controller with Integrated MPPT for PV Grid Connection, 17th international conference on Sciences and Techniques of Automatic control & computer engineering - STA'2016, Sousse, Tunisia, December 19-21, 2016

[1.19] Stala R., Individual mppt of photovoltaic arrays with use of single-phase three-level diode-clamped inverter, 2010 IEEE International Symposium on Industrial Electronics, 3456–3462, 2010, ISSN 2163-5137, URL http://dx.doi.org/10.1109/ISIE.2010.5637767.

[1.20] Sebastián Neira; Alonso Lizana; Javier Pereda, A Novel Three-Port NPC Converter for Grid-Tied Photovoltaic Systems with Integrated Battery Energy Storage, 2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)

[1.21] Liwei Zhou; Feng Gao; Tingting Yang, Neutral-point-clamped circuits of single-phase PV inverters: Generalized principle and implementation, 2015 IEEE Energy Conversion Congress and Exposition (ECCE)

[1.22] Kouro S., Wu B., Moya ., Villanueva E., Correa P., Rodr´ıguez J., Control of a cascaded h-bridge multilevel converter for grid connection of photovoltaic systems, 2009 35th Annual Conference of IEEE Industrial Electronics, 3976–3982, 2009, ISSN 1553-572X, URL http://dx.doi. org/10.1109/IECON.2009.5415332.

[1.23] Rodriguez J., Bernet S., Wu B., Pontt J.O., Kouro S., Multilevel voltage-source-converter topologies for industrial medium-voltage drives, IEEE Transactions on Industrial Electronics, 54(6), 2930–2945, 2007, ISSN 0278-0046, URL http://dx.doi.org/10.1109/TIE.2007.907044.

[1.24] M. Khazraei, D. Zupancic, “Solar Inverter Design. The Race to Design High-Efficiency, High-Power-Density Inverters”, Power Systems Design, pp. 9-12, May 2020.

[1.25] R. Stala, “Natural DC-link voltage balance in a single-phase NPC inverter with four-level legs and novel modulation method”. IET Power Electronics, 13: 3764-3776, 2020.

[1.26] R. Strzelecki, P. Szczepankowski, N. Strzelecka, “Four level diode-clamped back-to-back converter with active DC link voltage control”, Int. Conf.-Workshop Compatibility and Power Electron., Ljubljana, 2013, pp. 182– 187

[1.27] A. Shukla, A. Ghosh and A. Joshi, "Flying-Capacitor-Based Chopper Circuit for DC Capacitor Voltage Balancing in Diode-Clamped Multilevel

Inverter," in IEEE Trans. on Ind. Electron., vol. 57, no. 7, pp. 2249-2261, July 2010

[1.28] D. Cui and Q. Ge, "A Novel Hybrid Voltage Balance Method for Five-Level Diode-Clamped Converters," in IEEE Transactions on Industrial Electronics, vol. 65, no. 8, pp. 6020-6031, Aug. 2018.

[1.29] J. Zhao, Y. Han, X. He, C. Tan, J. Cheng and R. Zhao, "Multilevel Circuit Topologies Based on the Switched-Capacitor Converter and Diode-Clamped Converter," in IEEE Transactions on Power Electronics, vol. 26, no. 8, pp. 2127-2136, Aug. 2011.

[1.30] Stala R., Application of balancing circuit for dc-link voltages balance in a single-phase diode-clamped inverter with two three-level legs, IEEE Transactions on Industrial Electronics, 58(9), 4185–4195, 2011, ISSN 0278-0046, URL http://dx.doi.org/10.1109/TIE.2010.2093477

[1.31] Pou J., Pindado R., Boroyevich D., Voltage-balance limits in four-level diode-clamped converters with passive front ends, Industrial Electronics, IEEE Transactions on, 52(1), 190 – 196, 2005, ISSN 0278-0046, URL http://dx.doi.org/10.1109/TIE.2004.837915

[1.32] Pirog S., Stala R., Selection of parameters for balancing circuit of dc-dc and ac-ac multicell converters, Power Electronics and Applications, 2005 European Conference on, 910 pp.–P.10, 2005, URL http://dx.doi.org/10.1109/EPE.2005.219297.

[1.33] Pirog S., Energoelektronika. Układy o komutacji sieciowej i o komutacji twardej, Uczelniane Wydawnictwa Naukowo-Dydaktyczne AGH, 2006.

[1.34] Mohzani Z., McGrath B.P., Holmes D.G., The balancing properties of dc link compensation for 3-phase neutral point clamped (npc) onverter, Power Electronics and Motion Control Conference (IPEMC), 2012 7th International, tom 1, 574–579, 2012, URL http://dx.doi.org/10.1109/IPEMC.2012.6258809.

[1.35] Mohzani Z., McGrath B.P., Holmes D.G., A generalized natural balance model and balance booster filter design for three-level neutral-point-clamped converters, IEEE Transactions on Industry Applications, 51(6),4605–4613, 2015, ISSN 0093-9994, URL http://dx.doi.org/10.1109/TIA.2015.2448618.

[1.36] Mouton H.D.T., Natural balancing of three-level neutral-point-clamped pwm inverters, IEEE Transactions on Industrial Electronics, 49(5), 1017–1025, 2002, ISSN 0278-0046, URL http://dx.doi.org/10.1109/TIE.2002.803205.

[1.37] Stala R, A Four-Level Single-Phase Diode-Clamped Inverter with Natural DC-Link Capacitor Voltage Balance

[1.38] S. Busquets-Monge, J. Bordonau and J. Rocabert, "Extension of the Nearest-Three Virtual-Space-Vector PWM to the Four-Level DiodeClamped dc-ac Converter," 2007 IEEE Power Electronics Specialists Conference, Orlando, FL, 2007, pp. 1892-1898.

[1.39] M. Narimani, V. Yaramasu, B. Wu, N. Zargari, G. Cheng and G. Moschopoulos, "A simple method for capacitor voltages balancing of diode-clamped multilevel converters using space vector modulation," IECON 2013 -

39th Annual Conference of the IEEE Industrial Electronics Society, Vienna, 2013, pp. 310-315.

[1.40] F. B. Grigoletto and H. Pinheiro, "Generalised pulse width modulation approach for DC capacitor voltage balancing in diode-clamped multilevel converters," in IET Power Electronics, vol. 4, no. 1, pp. 89-100, January 2011.

[1.41] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, P. Ibanez, and J. L. Villate, "A comprehensive study of a hybrid modulation technique for the neutralpoint-clamped converter," IEEE Trans. Ind. Electron., vol. 56, no. 2, pp. 294–304, Feb. 2009.

[1.42] O. Bouhali, B. Francois, E. M. Berkouk, and C. Saudemont, "DC link capacitor voltage balancing in a three-phase diode clamped inverter controlled by a direct space vector of line-to-line voltages," IEEE Trans. Power Electron., vol. 22, no. 5, pp. 1636–1648, Sep. 2007.

[1.43] K. Yan, W. Wang, Z. Zhu, and Q. Lu, "Study on neutral-point balancing for three-level space voltage vector pulse-width modulation inverter," in Proc. ICEMS, Oct. 17–20, 2008, pp. 1571–1576

[1.44] C. Newton and M. Sumner, "Neutral point control for multi-level inverters: theory, design and operational limitations," in , Conference Record of the 1997 IEEE Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting, IAS '97, 1997, vol. 2, pp. 1336– 1343 vol.2.

[1.45] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2219–2230, 2010.

[1.46] Qiang Song, Wenhua Liu, Qingguang Yu, Xiaorong Xie, and Zhonghong Wang, "A neutral-point potential balancing algorithm for three-level NPC inverters using analytically injected zero-sequence voltage," in Eighteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2003. APEC '03, 2003, vol. 1, pp. 228– 233 vol.1.

[1.47] N. Celanovic and D. Boroyevich, "A comprehensive study of neutralpoint voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," IEEE Transactions on Power Electronics, vol. 15, no. 2, pp. 242–249, Mar. 2000.

[1.48] S. Busquets-Monge, S. Somavilla, J. Bordonau, and D. Boroyevich, "Capacitor Voltage Balance for the Neutral-Point- Clamped Converter using the Virtual Space Vector Concept With Optimized Spectral Performance," IEEE Transactions on Power Electronics, vol. 22, no. 4, pp. 1128–1135, Jul. 2007.

[1.49] Corzine, K. A. and Majeethia, S. K. (2000). Analysis of
a Novel Four-Level DC/DC Boost Converter. IEEE Transactions on Industry Applications, 36(5), pp. 1342–1350.

[1.50] Corzine, K. A., Yuen, J. and Baker, J. R. (2002). Analysis of a Four-Level DC/DC Buck Converter. IEEE Transactions on Industrial Electronics, 49(4), pp. 746–751.

[1.51] Boora A. A., Nami A., Zare F., Ghosh A. and Blaabjerg F.: Voltage-sharing converter to supply single-phase asymmetrical four-level diode-clamped inverter with high power factor loads, IEEE Trans. Power Electron., vol. 25, no. 10, pp. 2507-2520

[1.52] Strzelecki R., Szczepankowski P., Strzelecka N.: Four Level Diode-Clamped Back-To-Back Converter with

active DC link voltage control, 2013 Int. Conf.-Workshop Compatibility and Power Electron., Ljubljana, 2013, pp. 182-187

[1.53] Hasegawa K. and Akagi H.: Voltage balancing of the four split DC capacitors for a five-level diode clamped PWM inverter with a front-end diode rectifier, The 2010 International Power Electronics Conference -

ECCE ASIA -, Sapporo, 2010, pp. 734-739

[1.54] A. Shukla, A. Ghosh and A. Joshi, "Flying-Capacitor-Based Chopper Circuit for DC Capacitor Voltage Balancing in Diode-Clamped Multilevel Inverter," in IEEE Trans. on Ind. Electron., vol. 57, no. 7, pp. 2249-2261, July 2010.

[1.55] D. Cui and Q. Ge, "A Novel Hybrid Voltage Balance Method for Five-Level Diode-Clamped Converters," in IEEE Transactions on Industrial Electronics, vol. 65, no. 8, pp. 6020-6031, Aug. 2018.

[1.56] Z. Shu, X. He, Z. Wang, D. Qiu and Y. Jing, "Voltage Balancing Approaches for Diode-Clamped Multilevel Converters Using Auxiliary Capacitor-Based Circuits," in IEEE Transactions on Power Electronics, vol. 28, no. 5, pp. 2111-2124, May 2013.

[1.57] J. Zhao, Y. Han, X. He, C. Tan, J. Cheng and R. Zhao, "Multilevel Circuit Topologies Based on the Switched-Capacitor Converter and Diode-Clamped Converter," in IEEE Transactions on Power Electronics, vol. 26, no. 8, pp. 2127-2136, Aug. 2011, doi: 10.1109/TPEL.2010.2104330.

[1.58] A. Taghvaie, M. E. Haque, S. Saha and M. A. Mahmud, "A New Step-up Voltage Balancing Circuit for Neutral-Point-Clamped Multilevel Inverter," 2018 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES), 2018, pp. 1-6, doi: 10.1109/PEDES.2018.8707464.

[1.59] Sano K. and Fujita H.: Voltage-Balancing Circuit Based on a Resonant Switched-Capacitor Converter for Multilevel Inverters, IEEE Trans. on Industry Applications, vol. 44, no. 6, pp. 1768-1776 25, no. 10, pp. 2507-2520

[1.60] J. Zhang, T. Q. Zheng, X. Yang and M. Wang, "Single resonant cell based multilevel soft-switching DC-DC converter for medium voltage conversion," 2016 IEEE Energy Conversion Congress and Exposition (ECCE), 2016, pp. 1-5, doi: 10.1109/ECCE.2016.7855437.

[1.61] M. Uno and A. Kukita, "Cell voltage equalizer using series resonant inverter and voltage multiplier for series-connected supercapacitors," 2012 IEEE Energy Conversion Congress and Exposition (ECCE), 2012, pp. 672-677, doi: 10.1109/ECCE.2012.6342756.

[1.62] M. Uno and A. Kukita, "Bidirectional PWM Converter Integrating Cell Voltage Equalizer Using Series-Resonant Voltage Multiplier for Series-

Connected Energy Storage Cells," in IEEE Transactions on Power Electronics, vol. 30, no. 6, pp. 3077-3090, June 2015, doi: 10.1109/TPEL.2014.2331312.

[1.63] Pascual C. and Krein P. T.: Switched capacitor system for automatic series battery equalization, Proceedings of APEC 97 - Applied Power Electronics Conference, Atlanta, GA, USA, 1997, pp. 848-854 vol.2.

[1.64] Kim M., Kim C., Kim J. and Moon G.: A Chain Structure of Switched Capacitor for Improved Cell Balancing Speed of Lithium-Ion Batteries, IEEE Transactions on Industrial Electronics, vol. 61, no. 8, pp. 3989-3999

[1.65] Daowd M., Antoine, M., Omar N., van den Bossche P.; van Mierlo, J.: Single Switched Capacitor Battery Balancing System Enhancements, Energies 2013, 6, 2149-2174.

[1.66] Shang Y., Xia B., Lu F., Zhang C., Cui N. and Mi C. C.: A Switched-Coupling-Capacitor Equalizer for Series-Connected Battery Strings, IEEE Transactions on Power Electronics, vol. 32, no. 10, pp. 7694-7706

[1.67] Colino, Stephen L. and R. A. Beach. “Fundamentals of Gallium Nitride Power Transistors.” (2013).

[1.68] S. Khoshzaman and I. Hahn, "A Performance Comparison of GaN FET and Silicon MOSFET," 2021 22nd IEEE International Conference on Industrial Technology (ICIT), 2021, pp. 127-133, doi: 10.1109/ICIT46573.2021.9453693.

[2.1] C. Barth, T. Foulkes, I. Moon, Y. Lei, S. Qin and R. C. N. Pilawa-Podgurski, "Experimental Evaluation of Capacitors for Power Buffering in Single-Phase Power Converters", IEEE Transactions on Power Electronics. doi: 10.1109/TPEL.2018.2878825

[2.2] F. Ueno, T. Inoue, I. Oota, I. Harada, “Emergency power supply for small computer systems,” in Proc. IEEE Int. Symp. Circuits and Systems, pp. 1065-1068, June 1991.

[2.3] J. F. Dickson, “On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique,” IEEE J. SolidState Circuits, vol. 11, no. 3, pp. 374-378, June 1976.

[2.4] H. Morimura and N. Shibata, "A step-down boosted-wordline scheme for 1-V battery-operated fast SRAM's", IEEE Journal of Solid-State Circuits, vol. 33, no. 8, pp. 1220-1227, Aug. 1998, doi: 10.1109/4.705360

[2.5] F. Su and W. Ki, "Component-Efficient Multiphase Switched-Capacitor DC–DC Converter With Configurable Conversion Ratios for LCD Driver Applications", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 55, no. 8, pp. 753-757, Aug. 2008.

[2.6] Y. Allasasmeh and S. Gregori, "A performance comparison of dickson and fibonacci charge pumps," 2009 European Conference on Circuit Theory and Design, 2009, pp. 599-602, doi: 10.1109/ECCTD.2009.5275049.

[2.7] A. Ioinovici, H. S. H. Chung, M. S. Makowski and C. K. Tse, "Comments on “Unified Analysis of Switched-Capacitor Resonant Converters‖, IEEE Transactions on Industrial Electronics, vol. 54, no. 1, pp. 684-685, Feb. 2007. doi: 10.1109/TIE.2006.885454

[2.8] Y. P. B. Yeung, K. W. E. Cheng, S. L. Ho, K. K. Law and D. Sutanto, "Unified analysis of switched-capacitor resonant converters", IEEE Transactions on Industrial Electronics, vol. 51, no. 4, pp. 864-873, Aug. 2004, doi: 10.1109/TIE.2004.831743

[2.9] H. Taghizadeh, A. M. Cross, R. Whitehouse and C. Barker, "Switched capacitor DC-DC converters for HVDC applications," 11th IET International Conference on AC and DC Power Transmission, 2015, pp. 1-9, doi: 10.1049/cp.2015.0083.

[2.10] Kansagara, Kevin & Kittur, H. & Naidu K, Jagannadha. (2016). On-chip adaptive switched capacitor-based DC-DC converter. International Journal of Power Electronics. 8. 38. 10.1504/IJPELEC.2016.10002724.

[2.11] M. Evzelman and S. Ben-Yaakov, "Average-Current-Based Conduction Losses Model of Switched Capacitor Converters," in IEEE Transactions on Power Electronics, vol. 28, no. 7, pp. 3341-3352, July 2013, doi: 10.1109/TPEL.2012.2226060.

[2.12] M. S. Makowski and D. Maksimovic, “Performance limits of switchedcapacitor dc-dc converters,” in Proc. IEEE Power Electron. Spec. Conf., Jun. 1995, vol. 2, pp. 1215–1221.

[2.13] Mondzik, Z. Waradzyn, R. Stala and A. Penczek, “High efficiency switched capacitor voltage doubler with planar core-based resonant choke”, CPE-POWERENG 2016, 10th international conference on Compatibility, Power Electronics and Power Engineering, 402–409, (2016).

[2.14] Z. Waradzyn, R. Stala, A. Mondzik and S. Pirog, “Switched capacitor-based power electronic converter-optimization of high frequency resonant circuit components”, Chapter in: Advanced Control of Electrical Drives and Power Electronic Converters, Volume 75 of the series Studies in Systems, Decision and Control. Springer International Publishing AG, 361–378, (2017).

[2.15] Kawa, R. Stala, A. Mondzik, S. Pirog and A. Penczek, “High power thyristor-based DC-DC switched-capacitor voltage multipliers: basic concept and novel derived topology with reduced number of switches”, IEEE Transactions on Power Electronics,31, 6797–6813 (2016).

[2.16] Evzelman M. Ben-Yaakov S., "Average-current-based conduction losses model of switched capacitor converters," IEEE Transactions on Power Electronics, vol.28, no.7, pp.3341,3352, July 2013. [3]

[2.17] Ben-Yaakov S., "On the influence of switch resistances on switchedcapacitor converter losses," IEEE Transactions on Industrial Electronics, vol.59, no.1, pp.638,640, Jan. 2012.

[2.18] Alam M.K., Khan F.H., "Efficiency characterization and impedance modeling of a multilevel switched capacitor converter using pulse dropping switching scheme," IEEE Transactions on Power Electronics, vol.29, no.6, pp.3145,3158, June 2014.

[2.19] Zhiguo Pan, Fan Zhang, Peng F.Z., "Power losses and efficiency analysis of multilevel dc-dc converters," Twentieth Annual IEEE Applied Power

Electronics Conference and Exposition APEC 2005, vol.3, no., pp.1393,1398, 6-10 March 2005.

[2.20] Cervera A., Evzelman M., Mordechai Peretz M. Ben-Yaakov S., "A high efficiency resonant switched capacitor converter with continuous conversion ratio," IEEE Transactions on Power Electronics, vol.30, no.3, pp.1373,1382, March 2015.

[2.21] Zhang F., Du L., Peng F. Z., Qian Z., "A New Design Method for HighPower High-Efficiency Switched-Capacitor DC–DC Converters," IEEE Transactions on Power Electronics, vol. 23, no. 2, pp. 832,840, March 2008.

[2.22] A. Mondzik, Z. Waradzyn, R. Stala and A. Penczek, "High efficiency switched capacitor voltage doubler with planar core-based resonant choke," 2016 10th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), 2016, pp. 402-409, doi: 10.1109/CPE.2016.7544222.

[3.1] https://toshiba.semicon-storage.com/info/docget.jsp?did=13415 (accessed May 2022)

[3.2] Kolar J. W., Krismer F., Lobsiger Y., Mühlethaler J., Nussbaumer T., Miniböck J., "Extreme Efficiency Power Electronics", Proceedings of the International Conference of Integrated Power Electronics Systems (CIPS 2012), Nuremberg, Germany, March 6-8, 2012

[3.3] Vencislav Cekov Valchev, Alex Van den Bossche; "Inductors and Transformers for Power Electronics"; CRC Press, 2018; ISBN 142002728X

[3.4] A. Ayachit and M. K. Kazimierczuk, "Steinmetz Equation for Gapped Magnetic Cores," in IEEE Magnetics Letters, vol. 7, pp. 1-4, 2016, Art no. 1302704, doi: 10.1109/LMAG.2016.2540609.

[3.5] G. Zulauf, S. Park, W. Liang, K. N. Surakitbovorn and J. Rivas-Davila, "COSS Losses in 600 V GaN Power Semiconductors in Soft-Switched, High- and Very-High-Frequency Power Converters," in IEEE Transactions on Power Electronics, vol. 33, no. 12, pp. 10748-10763, Dec. 2018, doi: 10.1109/TPEL.2018.2800533.

[3.6] M. Guacci et al., "On the Origin of the Coss -Losses in Soft-Switching GaN-on-Si Power HEMTs," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 2, pp. 679-694, June 2019, doi: 10.1109/JESTPE.2018.2885442.

[4.1] https://www.mathworks.com/help/physmod/sps/specialized-power-systems.html?s_tid=CRUX_lftnav (accessed May 2022)

[5.1] https://www.mathworks.com/help/stateflow/index.html?searchHighlight=stateflow&s_tid=srchtitle_stateflow_1 (accessed May 2022)

[5.2] Pereda, J.; Dixon, J.; High-Frequency Link: A Solution for Using Only One DC Source in Asymmetric Cascaded Multilevel Inverters. IEEE Trans. on Ind. Electron 2011, 58, 3884-3892. DOI: 10.1109/TIE.2010.2103532.

[5.3] Jiwanjot Singh; Ratna Dahiya; Lalit Mohan Saini; Recent research on transformer based single DC source multilevel inverter: A review. Renewable

and Sustainable Energy Reviews 2018, 82, 3207-3224. https://doi.org/10.1016/j.rser.2017.10.023.

[5.4] Sun, X.; Wang, B.; Zhou, Y.; Wang, W.; Du, H.; Lu, Z. A Single DC Source Cascaded Seven-Level Inverter Integrating Switched-Capacitor Techniques. IEEE Trans. on Industrial Electronics 2016, 63, 7184-7194. DOI: 10.1109/TIE.2016.2557317.

[5.5] https://www.transphormusa.com/en/products/ (accessed May 2022)

[5.6] http://ferroxcube.home.pl/prod/assets/e22616r.pdf (accessed May 2022)

[5.7] https://tmi.yokogawa.com/eu/solutions/discontinued/wt3000-precision-power-analyzer/ (accessed May 2022)

[6.1] Li S., Qi W., Tan S.C., Hui S.Y.(R.), Integration of an Active Filter and a Single-Phase AC/DC Converter With Reduced Capacitance Requirement and Component Count, IEEE Transactions on Power Electronics, vol. 31, no. 6, pp. 4121–4137 (2016).

[6.2] M., Xiong W., Yang J., Review of Active Power Decoupling Topologies in Single-

Phase Systems, IEEE Transactions on Power Electronics, vol. 31, no. 7, pp. 4778–4794 (2016).

[6.3] Method for Single-Phase AC–DC Converters, IEEE Transactions on Industrial Informatics, vol. 10, no. 1, pp. 461–468 (2014).

[6.4] Zhang H., Li X., Ge B., Balog R.S., Capacitance, dc Voltage Utilization, and Current Stress: Comparison of Double-Line Frequency Ripple Power Decoupling for Single-Phase Systems, IEEE Industrial Electronics Magazine, vol. 11, no. 3, pp. 37–49 (2017).

[6.5] Stawiarski Ł., Minimizing the energy parameters of the decoupling capacitor in a single phase AC–DC converter, Electrical Review (in Polish), vol. 90, no. 10, pp. 192–198 (2014).

[6.6] Stawiarski Ł., Piróg S., Minimizing the energy parameters of the decoupling capacitor and elimination of a double frequency component on the DC side in a single phase DC–AC converter, Electrical Review (in Polish), vol. 91, no. 5, pp. 80–87 (2015).

[6.7] Xia Y., Roy J., Ayyanar R., A Capacitance-Minimized, Doubly Grounded Transformer less Photovoltaic Inverter with Inherent Active-Power Decoupling, IEEE Transactions on Power Electronics, vol. 32, no. 7, pp. 5188–5201 (2017).

[6.8] Liu C., Lai J.S., Low Frequency Current Ripple Reduction Technique with Active Control in a FuelCell Power System with Inverter Load, IEEE Transactions on Power Electronics, vol. 22, no. 4, pp. 1429–1436 (2007).

[6.9] Shimizu T., Wada K., Nakamura N., Flyback-Type Single-Phase Utility Interactive Inverter with Power Pulsation Decoupling on the DC Input for an AC Photovoltaic Module System, IEEE Transactions on Power Electronics, vol. 21, no. 5, pp. 1264–1272 (2006).

[6.10] Tan G.H., Wang J.Z., Ji Y.C., Soft-switching flyback inverter with enhanced power decoupling for photovoltaic applications, IET Electric Power Applications, vol. 1, no. 2, pp. 264–274 (2007).
[6.11] Wang R. et al., A High Power Density Single-Phase PWM Rectifier with Active Ripple Energy Storage, IEEE Transactions on Power Electronics, vol. 26, no. 5, pp. 1430–1443 (2011).
[6.12] Łukasz Stawiarski, Stanisław Piróg, Active power decoupling topology for AC-DC and DC-AC single-phase systems with decoupling capacitor minimization, Archives Of Electrical Engineering VOL. 67(1), pp. 193–205 (2018), DOI 10.24425/119001