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### **Ważniejsze publikacje doktoranta:**

- J. Szyduczyński, D. Kościelnik, M. Miśkiewicz, "A Successive Approximation Time-to-Digital Converter with Single Set of Delay Lines for Time Interval Measurements", *Sensors* 19, no. 5: 1109, 2019
- D. Kościelnik, D. Rzepka and J. Szyduczyński, "Sample-and-Hold Asynchronous Sigma-Delta Time Encoding Machine," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 4, pp. 366-370, April 2016
- J. Szyduczyński, D. Kościelnik, K. Jurasz and M. Miśkiewicz, "Successive Approximation Time-to-Digital Converters," *Proceedings of 2020 6th International Conference on Event-Based Control, Communication, and Signal Processing (EBCCSP)*, Krakow, Poland, 2020, pp. 1-7,
- J. Szyduczyński, V. Nguyen, F. Schembari, R. B. Staszewski, D. Kościelnik and M. Miśkiewicz, "Behavioral Modelling and Optimization of a Cyclic Feedback-Based Successive Approximation TDC with Dynamic Delay Equalization," *Proceedings of 2019 5th International Conference on Event-Based Control, Communication, and Signal Processing (EBCCSP)*, Vienna, Austria, 2019, pp. 1-9.
- J. Szyduczyński, D. Kościelnik and M. Miśkiewicz, "Dynamic equalization of logic delays in feedback-based successive approximation TDCs," *Proceedings of 2017 3rd International Conference on Event-Based Control, Communication and Signal Processing (EBCCSP)*, Funchal, Portugal, 2017, pp. 1-6.
- D. Kościelnik, J. Szyduczyński, D. Rzepka, W. Andrysiewicz and M. Miśkiewicz, "Optimized design of successive approximation time-to-digital converter with single set of delay lines," *Proceedings of 2016 Second International Conference on Event-based Control, Communication, and Signal Processing (EBCCSP)*, Krakow, 2016, pp. 1-8.
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- D. Kościelnik, M. Miśkiewicz, J. Szyduczyński and D. Rzepka, "Optimizing time-to-digital converter architecture for successive approximation time measurements," *Proceedings of 2013 IEEE Nordic-Mediterranean Workshop on Time-to-Digital Converters (NoMe TDC)*, Perugia, 2013, pp. 1-8.