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Design and optimization of architectures for successive approximation time-to-digital converters

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Projektowanie i optymalizacja architektur przetworników analogowo-cyfrowych do przetwarzania interwałów czasu metodą sukcesywnej aproksymacji

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Abstract

Microelectronics and integrated circuit designs are heavily driven by technology scaling. With a reduction of the supply voltage in deep-submicron CMOS technologies, the resolution of encoding signal edges in the time domain is enhanced, while the resolution of encoding the voltage amplitude is decreased. In Time-Mode Signal Processing (TMSP), which is an alternative to classical signal processing performed in the voltage domain, the information is represented by the time interval between digital events. Time-to-digital converters (TDCs) are key building blocks of digitally intensive time-mode circuits and enablers for digital processing of analog signals encoded in time.

The research objective of this dissertation is focused on the design and implementation of the successive approximation time-to-digital converters (SA-TDCs). The dissertation includes the original enhancements for SA-TDCs either with feedforward, or feedback-based architectures. The proposition to optimize the feedforward SA-TDC architecture is based on a reduction of the number of sets of delay lines to one at the expense of a slight increase of logic complexity. The use of only one instead of two sets of delay lines allows to reduce twice the number of inverters in the high resolution feedforward SA-TDC architecture. The optimized SA-TDC topology with single set of delay lines has been implemented in 180 nm CMOS technology with additional enhancements aimed to improve the time resolution and reduce INL and DNL nonlinearities.

The other part of the dissertation concerns the design of SA-TDCs with the feedback-based architecture. For this purpose, the relevant system enhancements have been proposed to meet the challenges associated with the design of high-resolution feedback-based SA-TDCs. To improve the TDC performance weakened by circuit non-idealities, two calibration protocols have been presented. The proposed feedback-based SA-TDC with built-in fast self-calibration engine has been fabricated in 28 nm LP CMOS and verified by the measurements results. In addition, an innovative concept of the dynamic delay equalization for feedback-based SA-TDC was presented, which allows to minimize its conversion time to the theoretical limit. Furthermore, the thesis includes the comprehensive analysis of the conversion time of the SA-TDC converter both for feedforward and feedback-based architectures.

Streszczenie

Rozwój mikroelektroniki i metod projektowania układów scalonych jest określany przez systematyczną redukcję współczynnika charakterystycznego fabrykacji technologii CMOS. Wraz ze zmniejszeniem napięcia zasilania w submikronowych technologiach CMOS zwiększa się rozdzielczość kodowania zboczy sygnału w dziedzinie czasu, natomiast zmniejszeniu ulega rozdzielczość kodowania amplitudy w dziedzinie napięcia. Jedną z nowych technik projektowania układów analogowych stało się odwzorowanie przyrostów napięcia elektrycznego w postaci interwałów czasu (TMSP - *Time Mode Signal Processing*). W systemach TMSP informacja jest reprezentowana przez interwał czasu między dyskretnymi zdarzeniami. Kluczowym blokiem systemów TMSP jest układ przetwornika analogowo-cyfrowego do przetwarzania interwałów czasu (TDC - *Time-to-Digital Converter*), który umożliwia przetwarzanie sygnałów zakodowanych w czasie przy użyciu techniki cyfrowej.

Zakres niniejszej rozprawy dotyczy projektowania i implementacji przetworników analogowo-cyfrowych do przetwarzania interwałów czasu metodą sukcesywnej aproksymacji (SA-TDCs). Praca zawiera szereg udoskonaleń zarówno dla architektury kaskadowej przetwornika SA-TDC, jak i architektury ze sprzężeniem zwrotnym. W przypadku optymalizacji architektury kaskadowej przetwornika SA-TDC, w pracy przedstawiono nowatorską koncepcję systemu z pojedynczym zestawem linii opóźniających oraz dekodowaniem wyjściowego słowa cyfrowego. Zastosowanie pojedynczego zamiast podwójnego, jak to jest w podstawowej wersji układu, zestawu linii opóźniających pozwala przy dużej rozdzielczości bitowej na redukcję o niemal połowę złożoności układowej, wyrażonej w liczbie inwerterów wykorzystywanych do budowy przetwornika. Zoptymalizowana topologia przetwornika SA-TDC z pojedynczym zestawem linii opóźniających została zaimplementowana w technologii CMOS o parametrze charakterystycznym 180 nm wraz z dodatkowymi rozwiązaniami układowymi mającymi na celu poprawę rozdzielczości czasowej oraz zmniejszenie błędów nieliniowości różniczkowej i całkowej.

Dalsza część rozprawy dotyczy projektowania przetworników SA-TDC w architekturze ze sprzężeniem zwrotnym. Przedstawione zostały istotne rozwiązania układowe związane z projektowaniem przetworników SA-TDC o wysokiej rozdzielczości z dwoma algorytmami kalibracji w celu zmniejszenia błędów nieliniowości różniczkowej i całkowej. Zaprojektowany przetwornik SA-TDC ze

sprzężeniem zwrotnym wraz z wbudowanym układem kalibracji został sfabrykowany w technologii CMOS o parametrze charakterystycznym 28 nm, a następnie zweryfikowany eksperymentalnie poprzez pomiary prototypu. Ponadto dla przetwornika SA-TDC ze sprzężeniem zwrotnym przedstawiono nową koncepcję architektury z dynamiczną korekcją opóźnień, która umożliwia skrócenie czasu przetwarzania tego przetwornika do wartości minimalnej, wynikającej z samej metody przetwarzania. Jednym z istotnych aspektów zawartych w rozprawie jest ponadto analiza czasu przetwarzania przetwornika SA-TDC oraz przedstawienie analitycznej zależności pomiędzy czasem przetwarzania a długością przetwarzanego interwału czasu.

1. Motivation and Aim of Dissertation

The primary benefit of CMOS technology scaling is a reduction of the intrinsic gate delay of digital circuits. The improved switching characteristics of MOS transistors offer an excellent timing accuracy such that the time resolution of digital circuits has well surpassed the voltage resolution of analog circuits implemented in nanoscale CMOS technologies. The technique of encoding signals in time instead of in amplitude is expected to be further improved by advances in CMOS technology. Time-mode signal processing (TMSP) is an emerging signal processing technique developed as an alternative to classical signal processing performed in voltage domain. The TDCs are devices that convert time domain information into a digital representation, so they act as analog-to-digital converters for time-mode signal processing systems.

Nowadays, the time-to-digital converters find a broad spectrum of applications such as digital storage oscillators, laser-based vehicle navigation systems, medical imaging and instrumentation, infinite and finite impulse response filters, all digital phase-locked loops, clock data recovery, and channel select filters for software-defined radio.

The delay line and Vernier delay line TDCs are the most popular TDC architectures that employ the propagation delay of CMOS logic gates to achieve a fine resolution of time. The TDC architectures either with delay lines or based on Vernier technique have two significant drawbacks. For a wide input full scale, the *n*-bit TDC requires a number of 2^n -1 flip-flops and this number doubles with an increase of the converter resolution by one bit. Furthermore, the conversion result is obtained in the thermometer code which needs extra logic for transcoding it to a binary form. These disadvantages can be alleviated by successive approximation TDCs (SA-TDCs). However, recent works reporting design and implementations of SA-TDC are suboptimal in terms of the trade-off between circuit complexity, die area, and conversion time.

The dissertation is focused on the time-to-digital converters based on successive approximation, and its objective is to introduce and demonstrate new approaches to SA-TDC designs and analysis. The dissertation presents a comprehensive study of feedforward and feedback-based architectures for the SA-TDC and proposes design optimizations in terms of removing redundancy of delay lines, compensations of logic propagation delays, and increase of energy efficiency. The new design concepts have been implemented in integrated chips in 180 nm CMOS and 28 nm LP CMOS

processes, and verified using SPECTRE simulations in Cadence^{TM} Virtuoso as well as by the measurement results of fabricated SA-TDC chip in TSMC 28-nm LP CMOS.

2. Hypotheses

In the dissertation, the following hypotheses have been formulated:

I. The successive approximation time-to-digital converter (SA-TDC) with feedforward architecture may be designed with the use of a single set of binary-scaled delay lines by exploiting the effect of swapping the signal paths and additional decoding the output codeword. The adoption of the single set instead of the double set of delay lines reduces the number of transistors needed to design the converter and die area of the integrated circuit. The reduction of the number of transistors grows with the converter resolution and equals almost twice for high resolutions.

II. The techniques of matching the propagation delays of digital logic (e.g., by symmetrized design of multiplexers) in two signal paths propagating the events that define respectively a start and a stop of input time interval in SA-TDCs allow to reduce the INL and DNL errors and enhance the converter resolution.

III. The conversion time T_{Conv_b} of the ideal *n*-bit feedforward or feedback-based SA-TDC with zero logic propagation delays adopted for the bipolar input time interval $T_{In} \in (-FSR/2\,, FSR/2)$ is a linear function of the T_{In} given by the formula:

$$T_{Conv\_b} = \frac{FSR}{4} + \frac{|T_{In}|}{2} + \min\{-T_0 - t_{BHf}, t_{BHf}\}$$

where FSR is the full scale range of SA-TDC,

$T_0 = \frac{FSR}{2^n}$ is the duration of *LSB*,

$t_{BHf} = \begin{cases} \frac{t_B}{2};\ \text{for: } b_0 = 0 \\ \frac{t_B - T_0}{2};\ \text{for: } b_0 = 1 \end{cases}$,

t_B is the quantization error,

b_0 is the bit of digital code word $B=b_{n-1},\ldots, b_0$.

In particular for $n\to\infty$, the conversion time varies from the quarter (if $T_{In}\to 0$) to the half (if $T_{In}\to FSR/2$ or $T_{In}\to -FSR/2$) of the full-scale range *FSR* according to:

$$\lim_{n\to\infty}(T_{Conv\_b}(T_{In})) = \frac{FSR}{4} + \frac{|T_{In}|}{2}.$$

IV. The conversion time T_{Conv} of the ideal *n*-bit feedforward or feedback-based SA-TDC with zero logic propagation delays adopted for the unipolar input time interval $T_{In} \in (0, FSR)$ is given by the formula:

$$T_{Conv} = \frac{FSR}{2} + \frac{T_{In}}{2} + \min\{-T_0 - t_{BHf}, t_{BHf}\}$$

where FSR is the full scale range of SA-TDC,

$T_0 = \frac{FSR}{2^n}$ is the duration of *LSB*,

$$t_{BHf} = \begin{cases} \frac{t_B}{2};\ \text{for: } b_0 = 0 \\ \frac{t_B - T_0}{2};\ \text{for: } b_0 = 1 \end{cases},$$

t_B is the quantization error,

b_0 is the bit of digital code word $B=b_{n-1},\ldots, b_0$.

In particular for $n\to\infty$, the conversion time varies from the half (if $T_{In}\to 0$) to the total value (if $T_{In}\to FSR$) of the full-scale range *FSR* according to:

$$\lim_{n\to\infty}\left(T_{Conv}(T_{In})\right) = \frac{FSR}{2} + \frac{T_{In}}{2}.$$

V. The conversion time T'_{Conv_b} of the real *n*-bit SA-TDC with non-zero logic propagation delays ($T_m>0$) and feedforward architecture adopted for the bipolar input time interval T_{In} is expressed by the formula:

$$T'_{Conv\_b} = (n-1)T_m + T_{Conv\_b}$$

where T_{Conv_b} is the conversion time of the ideal bipolar *n*-bit SA-TDC defined in Hypothesis III.

In turn, for the real *n*-bit feedforward SA-TDC adopted for the unipolar input time interval T_{In}, the conversion time T'_{Conv} is given by the formula:

$$T'_{Conv} = (n-1)T_m + T_{Conv}$$

where T_{Conv} is the conversion time of the ideal unipolar *n*-bit SA-TDC defined in Hypothesis IV.

VI. In order to guarantee the correct operation of monotone approximation algorithm, the fixed offset time T_m in the real *n*-bit feedback-based SA-TDC adopted for bipolar input time interval T_{In} should be longer than a quarter of the full-scale range (*FSR*/4):

$$T_m > FSR/4$$

and its conversion time is then according to Hypothesis V:

$$T'_{Conv\_b} > (n-1)\frac{FSR}{4} + T_{Conv\_b}.$$

In turn, to guarantee the correct operation of monotone approximation algorithm for the real unipolar *n*-bit feedback-based SA-TDC, T_m should be longer than a half of the full-scale range (*FSR*/2):

$$T_m > FSR/2$$

and its conversion time is then according to Hypothesis V:

$$T'_{Conv} > (n-1)\frac{FSR}{2} + T_{Conv}\ .$$

VII. The use of dynamic delay equalization technique gives the possibility to guarantee the correct operation of monotone approximation algorithm with the fixed offset time $T_m < FSR/4$ in the real bipolar *n*-bit feedback-based SA-TDC.

In turn, for *n*-bit unipolar feedback-based SA-TDC the use of dynamic delay equalization technique allows to apply $T_m < FSR/2$.

VIII. The use of dynamic delay equalization technique allows to reduce the conversion time of the real bipolar *n*-bit feedback-based SA-TDC from at least $(n-1)\frac{FSR}{4} + T_{Conv\_b}$ to $(n-1)T_m + T_{Conv\_b}$ which is equivalent to

the reduction of the conversion time to that of feedforward SA-TDC defined in Hypothesis V.

In turn, for the real unipolar *n*-bit feedback-based SA-TDC the use of dynamic delay equalization technique allows to reduce the conversion time from at least $(n-1)\frac{FSR}{2} + T_{Conv}$ to $(n-1)T_m + T_{Conv}$ which is equal to the conversion time of feedforward SA-TDC defined in Hypothesis V.

3. Summary

In the dissertation, the contribution to the development of time-to-digital converters based on successive approximation (SA-TDCs—Successive Approximation TDCs) using binary-scaled delay lines either in the feedforward or feedback-based architecture has been presented. The effort has been focused on the TDCs based on the monotone successive approximation, which is the most common conversion algorithm in SA-TDCs.

The study of the feedforward SA-TDC architecture shows that the converter can be optimized in terms of circuit complexity and die area. The main design improvement relies on removing one of two sets of delay lines from the SA-TDC feedforward architecture. A novel feedforward SA-TDC architecture with a single set of delay lines using the effect of swapping the signal paths and decoding the output codeword has been proposed in this thesis (Hypothesis I). The analysis shows that the reduction of complexity of proposed SA-TDC for 8 bits is around 20–30%, while for 12 bits respectively almost 50% compared to classical SA-TDC topology. Additionally, the improvement of converter performance in the implementation of 8-bit SA-TDC with a time resolution of 25 ps in 180 nm CMOS technology obtained by asymmetrical design of pair of inverters and symmetrized multiplexer control has been reported (Hypothesis II).

The further research has concerned the implementation of 10-bit feedback-based SA-TDC with a fast self-calibration engine in 28 nm LP CMOS technology. For this purpose, several system and circuit level innovations have been presented to address challenges in the design of high-resolution and high-speed TDCs. Fine-precision, large range DTCs with improved power-efficiency have been introduced, while the proposed digital control architecture enables speed up of conversion times for feedback-based SA-TDCs. To mitigate the impact of mismatch in the internal differential delay

elements as well as their nonlinearity, the built-in fast self-calibration procedures with low hardware overhead has been realized.

The other contribution is the proposition of a novel feedback-based SA-TDC architecture with dynamic delay equalization. The objective of this concept is to reduce the redundant conversion time of feedback-based SA-TDC to the theoretical limit defined by the conversion algorithm, and to get not worse conversion rate than achieved by the feedforward counterpart, at the cost of increasing the complexity of the converter architecture.

A significant effort has been put into the analysis of conversion time of the *n*-bit SA-TDC, which is one of the most important TDC parameters. The analytical evaluation of the conversion time for SA-TDC versus input time interval, which is valid either for feedforward, or for feedback-based architecture, has been formulated.

In particular, it has been shown that the conversion time of an ideal SA-TDC with zero logic propagation delays is a linear function of the length of the input time interval and varies from quarter (half) to the half (total) value of the full-scale range for the bipolar (unipolar) input time interval (Hypotheses III and IV). In turn, for real *n*-bit feedforward SA-TDC with non-zero logic propagation delays (T_m>0), the conversion time is extended by (n-1)T_m compared to the conversion time for the ideal SA-TDC (Hypothesis V). Furthermore, it has been proven that the valid time-to-digital conversion based on successive approximation in the real bipolar (unipolar) feedback-based SA-TDC requires the fixed offset time T_m to be longer than a quarter (half) of the full-scale range (Hypothesis VI). On the other hand, the use of the dynamic delay equalization technique enables the correct conversion of real bipolar (unipolar) feedback-based SA-TDC with fixed time offset $T_m < FSR/4$ ($T_m < FSR/2$) (Hypothesis VII). Finally, with the dynamic delay equalization technique, the conversion time of feedback-based SA-TDC architecture can be the same as for the counterpart with feedforward architecture (Hypothesis VIII).

In the view of the above listed achievements, it can be concluded that all the hypotheses have been proven to be true.

The most important publications

- J. Szyduczyński, D. Kościelnik, M. Miśkowicz, "A Successive Approximation Time-to-Digital Converter with Single Set of Delay Lines for Time Interval Measurements", *Sensors* 19, no. 5: 1109, 2019

- K. Jurasz, D. Kościelnik, J. Szyduczyński, M. Miśkowicz, "Systematization and comparison of the binary successive approximation variants", *Sensors* 21, no. 24: 8267, 2021

- J. Szyduczyński, D. Kościelnik, K. Jurasz and M. Miśkowicz, "Successive Approximation Time-to-Digital Converters," *Proceedings of 2020 6th International Conference on Event-Based Control, Communication, and Signal Processing (EBCCSP)*, Krakow, Poland, 2020, pp. 1-7,

- J. Szyduczyński, V. Nguyen, F. Schembari, R. B. Staszewski, D. Kościelnik and M. Miśkowicz, "Behavioral Modelling and Optimization of a Cyclic Feedback-Based Successive Approximation TDC with Dynamic Delay Equalization," *Proceedings of 2019 5th International Conference on Event-Based Control, Communication, and Signal Processing (EBCCSP)*, Vienna, Austria, 2019, pp. 1-9.

- J. Szyduczyński, D. Kościelnik and M. Miśkowicz, "Dynamic equalization of logic delays in feedback-based successive approximation TDCs," *Proceedings of 2017 3rd International Conference on Event-Based Control, Communication and Signal Processing (EBCCSP)*, Funchal, Portugal, 2017, pp. 1-6.

- D. Kościelnik, J. Szyduczyński, D. Rzepka, W. Andrysiewicz and M. Miśkowicz, "Optimized design of successive approximation time-to-digital converter with single set of delay lines," *Proceedings of 2016 Second International Conference on Event-based Control, Communication, and Signal Processing (EBCCSP)*, Krakow, 2016, pp. 1-8.

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