Abstract

Low noise integrated circuits for radiation imaging with high-speed digital interface

Semiconductor detectors are widely used in various applications, such as radiation imaging (position sensitive X-ray detectors) or High-Energy Physics Experiments. The progress in the experimental physics field is associated with necessity to develop more and more technically advanced detection systems. The trend in the research development in the experiments such as ALICE (A Large Ion Collider Experiment) in CERN (Switzerland) or CBM (Compressed Baryonic Matter) in FAIR (Germany), is the increase of the measurements resolution of the deposited charge and the hit event time. To make it possible, the parameters of the sensor itself, but also of the readout electronics, should be improved. One of the most important challenges for the readout electronics designers from the analog electronics point of view, is the noise level reduction (stemming from the electronics, but also from some external elements or power supply interference), enabling operation with the high input rate (250 kHit/s/channel), making the circuits immune to the harsh environment (radiation and radiation-related damage, temperature change, leakage currents). The requirements for the digital part include primarily enabling the transmission to the top-level data acquisition system of the large amount of data (for example 40 MHit/s, 320 Mbps per link) providing the information about the registered event. This practically means an increase in the link throughput and faster electronics operation (in the order of GHz). Additionally, the multichannel readout circuits, usually highly integrated, are required to dissipate low power (in the order of 10 mW/channel) and be immune to the crosstalk, both between adjacent channels and within a single channel – between analog and digital parts.

In this work, the author conducted research towards the possibility to improve the parameters of the readout integrated circuits basing on the requirements for the electronics dedicated to the silicon strip sensors used in the STS (*Silicon Tracking System)* detector in the CBM experiment. The main goal of the research was to lower the noise level in the readout system, ensure better flexibility of adjusting the readout channels to changing operation conditions related to the variable noise contribution of the readout system elements (both internal, related to the electronics, as well as stemming from the external components), variable temperature, presence of the leakage currents and changing operation parameters of the system due to radiation-related effects. The topic of employing differential charge processing in the readout system was also raised in this work. The differential processing manner, although characterized by higher noise, power consumption and occupied area than single-ended architectures, allows for reduction of the power supply interference coupling and significantly decrease the total noise level of a charge processing chain. Another important issue discussed in this dissertation is testability of the multichannel integrate circuits operation parameters uniformity, included in the complex readout system in the number of up to more than ten thousand. This can be achieved by the design of a circuit for measurements of the internal biasing potentials and supply voltages integrated within a device under test.

The requirements concerning data transmission throughput increase continuously, while limiting the number of the transmission lines (cables) in the radiation detector readout systems are the reason, why so many of the High-Energy Physics electronics designers have been considering employing newer submicron technologies (transistor channel length is less than 100 nm) in order to speed up the operation of the transceivers integrated in the digital part of the readout electronics. The author conducted the research towards use of the newer technologies than used before in the Experimental Physics applications (usually 0.35 0.35 μm, 0.18 μm or 0.13 μm due to availability, price as well as stability and maturity of the process, verified in terms of performance in the presence of radiation) for the design of the multi-gigabit transceiver. The investigations were focused on the 28 nm technology capabilities and design of the most important part of the data transmission circuit – Phase Locked Loop (PLL) with particular attention paid to the radiation damage immunity.

The presented work includes description of a few solutions for the most important problems in the radiation detectors readout circuits. These are namely leakage current compensation circuit, for the first time combined with a fast reset of the charge sensitive amplifier, a circuit for monitoring of the internal biasing potentials of an integrated circuit, and extended models of the sensors and other components of the system, that can be employed for the simulation optimization of the readout electronics.

The result of the research work are three integrated circuits. Two of them are multichannel, analog readout circuits with the configurable operation parameters (as for example shaping filter type and shaping time), comprising both the single-ended type channels as well as differential ones. These circuits were designed and fabricated in the 180 nm CMOS technology and implement the developed methods of leakage current compensation and some other solutions improving the noise performance, as well as those increasing the circuit immunity to the supply interferences and radiation effects. The measurements results are presented and discussed. The third project is a phase locked loop circuit designed in the 28 nm CMOS technology, with special attention paid to the possibility to be employed in the design of a transceiver dedicated for operation in the presence of high radiation field.