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PH.D. DISSERTATION

Low noise integrated circuits for radiation imaging with high-speed digital interface

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KATEDRA METROLOGII I ELEKTRONIKI

ROZPRAWA DOKTORSKA

Niskoszumowe scalone układy z szybkim interfejsem cyfrowym do obrazowania promieniowania

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Abstract

Low noise integrated circuits for radiation imaging with high-speed digital interface

Semiconductor detectors are widely used in various applications, such as radiation imaging (position sensitive X-ray detectors) or High-Energy Physics Experiments. The progress in the experimental physics field is associated with necessity to develop more and more technically advanced detection systems. The trend in the research development in the experiments such as ALICE (A Large Ion Collider Experiment) in CERN (Switzerland) or CBM (Compressed Baryonic Matter) in FAIR (Germany), is the increase of the measurements resolution of the deposited charge and the hit event time. To make it possible, the parameters of the sensor itself, but also of the readout electronics, should be improved. One of the most important challenges for the readout electronics designers from the analog electronics point of view, is the noise level reduction (stemming from the electronics, but also from some external elements or power supply interference), enabling operation with the high input rate (250 kHit/s/channel), making the circuits immune to the harsh environment (radiation and radiation-related damage, temperature change, leakage currents). The requirements for the digital part include primarily enabling the transmission to the top-level data acquisition system of the large amount of data (for example 40 MHit/s, 320 Mbps per link) providing the information about the registered event. This practically means an increase in the link throughput and faster electronics operation (in the order of GHz). Additionally, the multichannel readout circuits, usually highly integrated, are required to dissipate low power (in the order of 10 mW/channel) and be immune to the crosstalk, both between adjacent channels and within a single channel – between analog and digital parts.

In this work, the author conducted research towards the possibility to improve the parameters of the readout integrated circuits basing on the requirements for the electronics dedicated to the silicon strip sensors used in the STS (*Silicon Tracking System)* detector in the CBM experiment. The main goal of the research was to lower the noise level in the readout system, ensure better flexibility of adjusting the readout channels to changing operation conditions related to the variable noise contribution of the readout system elements (both internal, related to the electronics, as well as stemming from the external components), variable temperature, presence of the leakage currents and changing operation parameters of the system due to radiation-related effects. The topic of employing differential charge processing in the readout system was also raised in this work. The differential processing manner, although characterized by higher noise, power consumption and occupied area than single-ended architectures, allows for reduction of the power supply interference coupling and significantly decrease the total noise level of a charge processing chain. Another important issue discussed in this dissertation is testability of the multichannel integrate circuits operation parameters uniformity, included in the complex readout system in the number of up to more than ten thousand. This can be achieved by the design of a circuit for measurements of the internal biasing potentials and supply voltages integrated within a device under test.

The requirements concerning data transmission throughput increase continuously, while limiting the number of the transmission lines (cables) in the radiation detector readout systems are the reason, why so many of the High-Energy Physics electronics designers have been considering employing newer submicron technologies (transistor channel length is less than 100 nm) in order to speed up the operation of the transceivers integrated in the digital part of the readout electronics. The author conducted the research towards use of the newer technologies than used before in the Experimental Physics applications (usually 0.35 μm, 0.18 μm or 0.13 μm due to availability, price as well as stability and maturity of the process, verified in terms of performance in the presence of radiation) for the design of the multi-gigabit transceiver. The investigations were focused on the 28 nm technology capabilities and design of the most important part of the data transmission circuit – Phase Locked Loop (PLL) with particular attention paid to the radiation damage immunity.

The presented work includes description of a few solutions for the most important problems in the radiation detectors readout circuits. These are namely leakage current compensation circuit, for the first time combined with a fast reset of the charge sensitive amplifier, a circuit for monitoring of the internal biasing potentials of an integrated circuit, and extended models of the sensors and other components of the system, that can be employed for the simulation optimization of the readout electronics.

The result of the research work are three integrated circuits. Two of them are multichannel, analog readout circuits with the configurable operation parameters (as for example shaping filter type and shaping time), comprising both the single-ended type channels as well as differential ones. These circuits were designed and fabricated in the 180 nm CMOS technology and implement the developed methods of leakage current compensation and some other solutions improving the noise performance, as well as those increasing the circuit immunity to the supply interferences and radiation effects. The measurements results are presented and discussed. The third project is a phase locked loop circuit designed in the 28 nm CMOS technology, with special attention paid to the possibility to be employed in the design of a transceiver dedicated for operation in the presence of high radiation field.

Abstrakt

Niskoszumowe scalone układy z szybkim interfejsem cyfrowym do obrazowania promieniowania

Detektory półprzewodnikowe stosowane są w różnych aplikacjach, takich jak obrazowanie (detektory pozycyjne promieniowania X) czy eksperymenty Fizyki Wysokich Energii. Rozwój fizyki eksperymentalnej związany jest z koniecznością projektowania coraz bardziej zaawansowanych technicznie systemów detekcyjnych. Tendencją w rozwoju badań w tej dziedzinie na przykładzie na przykład eksperymentów takich jak ALICE (*A Large Ion Collider Experiment*) w centrum badawczym CERN (Szwajcaria), czy CBM (*Compressed Baryonic Matter*) w ośrodku FAIR (Niemcy), jest zwiększenie rozdzielczości pomiaru wielkości ładunku zdeponowanego w detektorze półprzewodnikowym i czasu wystąpienia zdarzenia. Aby było to możliwe, konieczna jest poprawa parametrów zarówno samego detektora, jak i elektroniki odczytu. Wśród najważniejszych wyzwań stawianych projektantom elektroniki odczytu od strony części analogowej jest redukcja szumów (związanych z samą elektroniką, ale też elementami zewnętrznymi czy sprzęganiem zakłóceń od zasilania), zapewnienie pracy z dużą częstotliwością rejestrowanych cząstek (250 tyś. zdarzeń/s/kanał), uodpornienie na długotrwałą pracę w niekorzystnym środowisku (promieniowanie i związane z nim uszkodzenia radiacyjne, zmiany temperatury, prądy upływu). Wymagania dotyczące części cyfrowej to przede wszystkim umożliwienie transmisji bardzo dużej ilości danych (np. 40 milionów zdarzeń na sekundę, 320 Mbps na łącze) zawierających informację o zarejestrowanym zdarzeniu do nadrzędnego systemu akwizycji danych, co w praktyce oznacza zwiększenie przepustowości łącza oraz łączy się z szybszą pracą elektroniki (rzędu GHz) . Oprócz tego wielokanałowe układy odczytowe, najczęściej zintegrowane muszą charakteryzować się niskim poborem mocy (rzędu 10 mW/kanał) i odpornością na efekty przesłuchów zarówno pomiędzy sąsiednimi kanałami jak i w obrębie kanałów, pomiędzy częściami analogowymi i cyfrowymi.

W niniejszej pracy Autorka przeprowadziła badania nad możliwością poprawienia parametrów pracy układów odczytowych bazując na wymaganiach stawianych elektronice przeznaczonej do krzemowych detektorów paskowych w detektorze STS (*Silicon Tracking System)* w eksperymencie CBM. Głównym celem przeprowadzonych badań było obniżenie szumów w systemie odczytowym, zapewnienie większej elastyczności w dostosowywaniu poszczególnych kanałów odczytowych do zmiennych warunków pracy związanych ze zmiennym udziałem kontrybucji szumowych od różnych elementów systemu odczytowego (zarówno wewnętrznych, związanych z elektroniką, jak i pochodzących od zewnętrznych komponentów), zmienną temperaturą, obecnością prądów upływu oraz zmiennymi parametrami pracy układu w związku z efektami wywołanymi przez promieniowanie. W pracy podjęty został również temat wykorzystania przetwarzania różnicowego w kanale odczytowym, który, chociaż charakteryzuje się wyższymi szumami, poborem mocy oraz zajmowaną powierzchnią niż

architektury typu „*single-ended”*, pozwala zredukować wpływ zakłóceń od zasilania i znacząco zmniejszyć sumaryczny poziom szumów toru przetwarzania ładunku. Inną istotną kwestią poruszaną w niniejszej rozprawie jest zapewnienie testowalności jednorodności parametrów pracy wielokanałowych układów scalonych, których w rozbudowanym systemie odczytowym może być nawet kilkanaście tysięcy, poprzez opracowanie zintegrowanego układu do pomiaru potencjałów oraz napięć zasilania wewnątrz układu.

Wymagania dotyczące zwiększania przepustowości transmisji danych, przy równoczesnym ograniczeniu na ilość linii transmisyjnych (przewodów) w systemach odczytowych detektorów promieniowania są przyczyną, dla której wielu projektantów elektroniki przeznaczonej do celów Fizyki Wysokich Energii rozważa możliwość wykorzystania nowszych technologii submikronowych (w których długość kanału tranzystora jest poniżej 100 nm) w celu przyśpieszenia pracy nadajników integrowanych w części cyfrowej elektroniki odczytu. Autorka przeprowadziła również badania w kierunku wykorzystania nowszych technologii niż dotychczas używane w elektronice przeznaczonej do zastosowań w Fizyce Eksperymentalnej (najczęściej 0.35 μm, 0.18 μm lub 0.13 μm ze względu na dostępność, cenę, a także stabilność i dojrzałość procesu i weryfikację pod kątem zachowania w obecności promieniowania) do zaprojektowania nadajnika (*transceiver)* pozwalającego na Multi-Gigabitową transmisję danych. Badania skupiły się na możliwościach technologii 28 nm i zaprojektowaniu najważniejszej części układu transmisji danych, czyli pętli fazowej (*Phase Locked Loop, PLL)*, z zapewnieniem odporności na uszkodzenia radiacyjne.

Praca zawiera opis kilku rozwiązań istotnych problemów występujących w układach odczytowych detektorów promieniowania, takich jak układ kompensacji prądów upływu, po raz pierwszy w połączeniu z szybkim resetem wzmacniacza ładunkowego, projekt układu do monitorowania wewnętrznych potencjałów w układzie scalonym, a także opracowane rozszerzone modele sensorów i innych elementów systemu, wykorzystywane w celu optymalizacji symulacyjnej elektroniki odczytu.

Rezultatem prac badawczych są trzy układy scalone. Dwa z nich to wielokanałowe, analogowe układy odczytowe o konfigurowalnych parametrach pracy (jak np. typ filtra kształtującego i czasu kształtowania), zawierające zarówno kanały o architekturze unipolarnej, jak i różnicowe. Zostały one zaprojektowane i wyprodukowane w technologii 180 nm CMOS. W układach tych zaimplementowane zostały opracowane metody kompensacji prądu upływu oraz kilka innych rozwiązań pozwalających poprawić parametry szumowe, jak również uodpornić układ na zakłócenia z linii zasilania oraz na efekty radiacyjne. Praca przedstawia i omawia wyniki pomiarów tych układów. Trzeci projekt to układ analogowej pętli fazowej zaprojektowany w technologii 28 nm CMOS, pod kątem wykorzystania w projekcie nadajnika przeznaczonego do pracy w obecności silnych pól radiacyjnych.

1. Dissertation theses

1. Differential charge processing can be efficient in low-noise systems with the tight area and specific environmental constraints. Differential charge processing in the read-out electronics for detectors is rarely used due to higher power dissipation, larger area occupancy and intrinsically higher noise. However, this assumption is true only if the clean supply voltage can be provided. There are applications where the use of differential or pseudo-differential charge processing architectures may become beneficial. These applications include tracking detection stations where the power supply induced interference coupling is not negligible, cannot be externally filtered due to magnetic field and influences the electronics performance significantly. – The expected radiation dose and high magnetic field prevents the use of the commercial off-the-shelf low noise DC-DC converters/linear voltage regulators and ferrite-based inductors.
2. It is possible to improve the noise performance in the harsh and variable environment with varying and complex dominant noise sources contribution by in-depth analysis and simulation of the longitudinal and transverse architecture of the detector and connection to the read-out electronics and by employing configurability in the read-out electronics, especially in the shaping filters to adapt and a better match to the external conditions.
3. Stable operation of the Charge Sensitive Amplifier (CSA) with high feedback resistance while providing fast input charges processing in the presence of extensive leakage current of the unknown and variable amount and flowing direction, can be obtained by the combination of digitally-assisted fast reset with the leakage current compensation techniques.
4. Using newer technologies in the design of data transmitting circuitry is beneficial in terms of speeding up the operation and data transmission which is required in the complex read-out systems generating a huge amount of data but also can decrease the sensitivity of the circuit to the radiation-related effects (Total Irradiation Dose) and enable employing acceptably effective Single Event Effects mitigation techniques without compromising the available area and possible operating speed.

2. Summary and conclusions

The works included in this doctoral project were focused on the design of the low-noise analog front-end for the readout of the silicon strip sensors and the research towards new technologies and solutions application in the circuits for fast data transmission in the radiation environments. As a result of the research, the author designed three prototype integrated circuits: two analog front-ends and a PLL circuit aimed for the application in the High-Energy Physics Experiments. The main achievements and goals leading to the conclusions and Dissertation Theses confirmation are listed below:

- Design, simulation, layout and performance verification of the multichannel SMX_mini read-out ASIC.
- Design, simulation, layout and performance verification of the multichannel PRINCSA read-out ASIC.

The optimization of the analog charge processing circuitry included the following tasks:

- Measurements, analyses and circuits design for the full-size prototype readout circuit for the CBM experiment (SMX2.1 and SMX2.2).
- Design of on-chip internal bias potentials monitoring circuit that can withstand extended temperature and supply voltage variations.
- Implementation of double-polarity leakage current compensation method (switchable Krummenacher circuit) in combination with the CSA fast reset for high input count rate.
- Detailed noise studies including all the system components: internal (related to the read-out electronics) and external (concerning the sensor, power-supply network, interconnect etc.) basing on the sensor and cables models for the CBM experiment modified and evaluated for this purpose.
- Optimization of the read-out electronics towards lower noise (ENC) in the varying environment (various cables' and sensors' lengths). Development of new readout architectures adjustable to external conditions by employing a wide range of configurability in the charge processing channel such as switchable shapers architecture using a minimum number of the passive component divided into small components for better matching.
- Evaluation of the differential/pseudo-differential charge processing advantages in the specific conditions of high power supply interference coupling and minimization of crosstalk in mixed-mode designs.
- Implementation of internal CSA input transistor bias filters and study on the maximum achievable read-out electronics noise mitigation.

- Implementation of an improved internal calibration circuit for the pseudo-single polarity charge studies (with a minimum injection of the opposite polarity charge to the read-out channel) and more flexible characterization of the charge processing circuits.
- Study on the possibility to speed-up the charge processing capabilities in the presence of leakage current while providing stable, low noise performance of the CSA

The research towards faster data transmission and increased link throughput to be implemented in the radiation environment applications was summarized by designing and simulation verification of a radiation-tolerance improved Phase-Locked Loop for future use in the read-out systems for data transmission. The works included the following tasks:

- Study on fast data transmission, towards the development of a transceiver in newer technology (still rarely employed in the ICs for the HEP experiments), evaluation of the technology limits and possibilities to ensure radiation-hardened performance.

1. Thesis: Differential charge processing can be efficient in low-noise systems with the tight area and specific environmental constraints. Differential charge processing in the read-out electronics for detectors is rarely used due to higher power dissipation, larger area occupancy and intrinsically higher noise. However, this assumption is true only if the clean supply voltage can be provided. There are applications where the use of differential or pseudo-differential charge processing architectures may become beneficial. These applications include tracking detection stations where the power supply induced interference coupling is not negligible, cannot be externally filtered due to magnetic field and influences the electronics performance significantly. – The expected radiation dose and high magnetic field prevents the use of the commercial off-the-shelf low noise DC-DC converters/linear voltage regulators and ferrite-based inductors. **In the complex tracking detectors readout systems, where it is impossible to provide a clean power supply, a differential or pseudo-differential charge processing manner can prove useful. As shown by the measurements, differential channels, that in the laboratory conditions with the clean power supply show higher output noise level than the single-ended ones, are almost insensible to the external interference coupling, while in the single-ended channels a significant noise growth is observed. In the tracking detectors where external noise filters are not feasible, differential charge processing is worth considering at the expense larger area, power dissipation.**
2. Thesis: It is possible to improve the noise performance in the harsh and variable environment with varying and complex dominant noise sources contribution by in-depth analysis and simulation of the longitudinal and transverse architecture of the detector and connection to the read-out electronics and by employing configurability in the read-out electronics, especially in the shaping filters to adapt and a better match to the external conditions. **– The improvement**

of the noise performance by detailed models analysis based on both calculations and simulations of various combinations of environmental variables: going beyond the standard approach and classical optimization for the particular detector capacitance (matching the CSA input transistor size to obtain C_{in} = 1/3 C_{det}), as there are various detector lengths and therefore capacitances (together with the interconnect capacitance), and taking into account all noise contributions of the entire readout system, adding configurability in filter type and shaping time (while not complicating the design more than adding few more switches in the shapers' feedback network).

3. Thesis: Stable operation of the Charge Sensitive Amplifier (CSA) with high equivalent feedback resistance while providing fast input charges processing in the presence of excessive leakage current of the unknown and variable amount and flowing direction, can be obtained by the combination of digitally-assisted fast reset with the leakage current compensation techniques. - **For the Compressed Baryonic Matter experiment, for example, an incoming charges average hit rate assuming Landau-distribution is equal to 250 kHit/s/channel is required. The combination of the CSA feedback resistance with the digitally assisted fast reset (employing externally triggered switch) helps to achieve processing speed high enough to handle the rate of the incoming hits up to 1 MHit/s/channel. If there is no leakage current present in the readout system, it can be easily achieved. However, in the presence of even 1 nA leakage, the processing speed is degraded to 375 kHit/s/channel, while if the leakage grows to 5 nA, the maximum achievable channel occupancy falls to 150 kHit/s/channel.**

4. Using newer technologies in the design of data transmitting circuitry is beneficial not only in terms of speeding up the operation and data transmission which is required in the complex read-out systems generating a huge amount of data but also can decrease the sensitivity of the circuit to the radiation-related effects (Total Irradiation Dose) and enable employing acceptably effective Single Event Effects mitigation techniques without compromising the available area and possible operating speed. - **The radiation-hardening by design (RHBD) techniques applied in the high-speed circuitry unavoidably cause degradation of the maximum circuit operating frequency. The use of for example 28 nm, according to the simulated behaviour of the circuit implemented in this technology, is promising for future use in the SERDES circuits dedicated for the HEP experiments and development of the new facilities. The main advantage of the use of newer technology nodes is higher data transmission speed and throughput while providing radiation-immunity of the transceiver circuit. Such circuits can be employed especially in self-triggered or event-based readout systems.**

The results of the ongoing work were presented by the author at various international conferences, such as the IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), International Workshop on Radiation Imaging Detectors (iWoRiD), International

Conference Mixed Design of Integrated Circuits and Systems (MIXDES), MOS-Ak India, IEEE-SPIE Joint Symposium on Photonics, Web Engineering, Electronics for Astronomy and High Energy Physics Experiments, CBM Collaboration Meeting. The author published her work in the international journals from the JCR list, such as Journal of Instrumentation (2 articles - [75], [118]) or Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment (one article published [37], one being revised and will be published soon) and many other papers (SPIE [66], [80], [128], CBM collaboration reports – e.g. [52], [129]) and conference proceedings ([130], [131]) – 18 articles in total during the PhD project duration.

The future works will focus on the development of the circuitry for the fast data transceivers dedicated to future HEP experiments. The Phase-Locked Loop performance will be tested with the use of the radiation and evaluated for further improvement. The study on the radiation-immune SERDES circuits is also considered.

3. The most important publications

The articles published by the Author in the journals from the JCR list:

[1] **Weronika ZUBRZYCKA**, Krzysztof KASIŃSKI, "All-programmable low noise readout ASIC for silicon strip sensors in tracking detectors", Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 988, 164892. https://doi.org/https://doi.org/10.1016/j.nima.2020.164892

[2] **Weronika ZUBRZYCKA**, Krzysztof KASIŃSKI, "Prototype single-ended and pseudo-differential charge processing circuit for micro-strip silicon and gaseous sensors read-out", Journal of Instrumentation 2019, vol. 14 art. no. C11030, https://doi.org/10.1088/1748-0221/14/11/C11030

[3] **Weronika ZUBRZYCKA**, Krzysztof KASIŃSKI, "Leakage current-induced effects in the silicon microstrip and gas electron multiplier readout chain and their compensation method ", Journal of Instrumentation 2018 vol. 13 art. no. T04003, https://doi.org/10.1088/1748-0221/13/04/T04003

[4] Krzysztof KASIŃSKI, Adrian RODRIGUEZ-RODRIGUEZ, Jörg LEHNERT, **Weronika ZUBRZYCKA**, Robert SZCZYGIEL, Piotr OTFINOWSKI, Rafal KLECZEK, Christian J. SCHMIDT, "Characterization of the STS/MUCHXYTER2, a 128-Channel Time and Amplitude Measurement IC for Gas and Silicon Microstrip Sensors", Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, https://doi.org/10.1016/j.nima.2018.08.076

[5] Krzysztof KASIŃSKI, **Weronika ZUBRZYCKA**, "Overview of microelectronic circuits designed at AGH University for the CBM experiment", Acta Physica Polonica. B, Proceedings Supplement ; ISSN 1899-2358. — 2020 vol. 13 no. 4, s. 885–891. 45th Congress of Polish physicists : Kraków, September 13–18, 2019. https://www.actaphys.uj.edu.pl/fulltext?series=Sup&vol=13&page=885