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Low noise integrated circuits for radiation imaging with high-speed digital interface

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KATEDRA METROLOGII I ELEKTRONIKI

ROZPRAWA DOKTORSKA

Niskoszumowe scalone układy z szybkim interfejsem cyfrowym do obrazowania promieniowania

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Abstract

Low noise integrated circuits for radiation imaging with high-speed digital interface

Semiconductor detectors are widely used in various applications, such as radiation imaging (position sensitive X-ray detectors) or High-Energy Physics Experiments. The progress in the experimental physics field is associated with necessity to develop more and more technically advanced detection systems. The trend in the research development in the experiments such as ALICE (A Large Ion Collider Experiment) in CERN (Switzerland) or CBM (Compressed Baryonic Matter) in FAIR (Germany), is the increase of the measurements resolution of the deposited charge and the hit event time. To make it possible, the parameters of the sensor itself, but also of the readout electronics, should be improved. One of the most important challenges for the readout electronics designers from the analog electronics point of view, is the noise level reduction (stemming from the electronics, but also from some external elements or power supply interference), enabling operation with the high input rate (250 kHit/s/channel), making the circuits immune to the harsh environment (radiation and radiation-related damage, temperature change, leakage currents). The requirements for the digital part include primarily enabling the transmission to the top-level data acquisition system of the large amount of data (for example 40 MHit/s, 320 Mbps per link) providing the information about the registered event. This practically means an increase in the link throughput and faster electronics operation (in the order of GHz). Additionally, the multichannel readout circuits, usually highly integrated, are required to dissipate low power (in the order of 10 mW/channel) and be immune to the crosstalk, both between adjacent channels and within a single channel – between analog and digital parts.

In this work, the author conducted research towards the possibility to improve the parameters of the readout integrated circuits basing on the requirements for the electronics dedicated to the silicon strip sensors used in the STS (*Silicon Tracking System)* detector in the CBM experiment. The main goal of the research was to lower the noise level in the readout system, ensure better flexibility of adjusting the readout channels to changing operation conditions related to the variable noise contribution of the readout system elements (both internal, related to the electronics, as well as stemming from the external components), variable temperature, presence of the leakage currents and changing operation parameters of the system due to radiation-related effects. The topic of employing differential charge processing in the readout system was also raised in this work. The differential processing manner, although characterized by higher noise, power consumption and occupied area than single-ended architectures, allows for reduction of the power supply interference coupling and significantly decrease the total noise level of a charge processing chain. Another important issue discussed in this dissertation is testability of the multichannel integrate circuits operation parameters uniformity, included in the complex readout system in the number of up to more than ten thousand. This can be achieved by the design of a circuit for measurements of the internal biasing potentials and supply voltages integrated within a device under test.

The requirements concerning data transmission throughput increase continuously, while limiting the number of the transmission lines (cables) in the radiation detector readout systems are the reason, why so

many of the High-Energy Physics electronics designers have been considering employing newer submicron technologies (transistor channel length is less than 100 nm) in order to speed up the operation of the transceivers integrated in the digital part of the readout electronics. The author conducted the research towards use of the newer technologies than used before in the Experimental Physics applications (usually 0.35 μm, 0.18 μm or 0.13 μm due to availability, price as well as stability and maturity of the process, verified in terms of performance in the presence of radiation) for the design of the multi-gigabit transceiver. The investigations were focused on the 28 nm technology capabilities and design of the most important part of the data transmission circuit – Phase Locked Loop (PLL) with particular attention paid to the radiation damage immunity.

The presented work includes description of a few solutions for the most important problems in the radiation detectors readout circuits. These are namely leakage current compensation circuit, for the first time combined with a fast reset of the charge sensitive amplifier, a circuit for monitoring of the internal biasing potentials of an integrated circuit, and extended models of the sensors and other components of the system, that can be employed for the simulation optimization of the readout electronics.

The result of the research work are three integrated circuits. Two of them are multichannel, analog readout circuits with the configurable operation parameters (as for example shaping filter type and shaping time), comprising both the single-ended type channels as well as differential ones. These circuits were designed and fabricated in the 180 nm CMOS technology and implement the developed methods of leakage current compensation and some other solutions improving the noise performance, as well as those increasing the circuit immunity to the supply interferences and radiation effects. The measurements results are presented and discussed. The third project is a phase locked loop circuit designed in the 28 nm CMOS technology, with special attention paid to the possibility to be employed in the design of a transceiver dedicated for operation in the presence of high radiation field.

Abstrakt

Niskoszumowe scalone układy z szybkim interfejsem cyfrowym do obrazowania promieniowania

Detektory półprzewodnikowe stosowane są w różnych aplikacjach, takich jak obrazowanie (detektory pozycyjne promieniowania X) czy eksperymenty Fizyki Wysokich Energii. Rozwój fizyki eksperymentalnej związany jest z koniecznością projektowania coraz bardziej zaawansowanych technicznie systemów detekcyjnych. Tendencją w rozwoju badań w tej dziedzinie na przykładzie na przykład eksperymentów takich jak ALICE (*A Large Ion Collider Experiment*) w centrum badawczym CERN (Szwajcaria), czy CBM (*Compressed Baryonic Matter*) w ośrodku FAIR (Niemcy), jest zwiększenie rozdzielczości pomiaru wielkości ładunku zdeponowanego w detektorze półprzewodnikowym i czasu wystąpienia zdarzenia. Aby było to możliwe, konieczna jest poprawa parametrów zarówno samego detektora, jak i elektroniki odczytu. Wśród najważniejszych wyzwań stawianych projektantom elektroniki odczytu od strony części analogowej jest redukcja szumów (związanych z samą elektroniką, ale też elementami zewnętrznymi czy sprzęganiem zakłóceń od zasilania), zapewnienie pracy z dużą częstotliwością rejestrowanych cząstek (250 tyś. zdarzeń/s/kanał), uodpornienie na długotrwałą pracę w niekorzystnym środowisku (promieniowanie i związane z nim uszkodzenia radiacyjne, zmiany temperatury, prądy upływu). Wymagania dotyczące części cyfrowej to przede wszystkim umożliwienie transmisji bardzo dużej ilości danych (np. 40 milionów zdarzeń na sekundę, 320 Mbps na łącze) zawierających informację o zarejestrowanym zdarzeniu do nadrzędnego systemu akwizycji danych, co w praktyce oznacza zwiększenie przepustowości łącza oraz łączy się z szybszą pracą elektroniki (rzędu GHz) . Oprócz tego wielokanałowe układy odczytowe, najczęściej zintegrowane muszą charakteryzować się niskim poborem mocy (rzędu 10 mW/kanał) i odpornością na efekty przesłuchów zarówno pomiędzy sąsiednimi kanałami jak i w obrębie kanałów, pomiędzy częściami analogowymi i cyfrowymi.

W niniejszej pracy Autorka przeprowadziła badania nad możliwością poprawienia parametrów pracy układów odczytowych bazując na wymaganiach stawianych elektronice przeznaczonej do krzemowych detektorów paskowych w detektorze STS (*Silicon Tracking System)* w eksperymencie CBM. Głównym celem przeprowadzonych badań było obniżenie szumów w systemie odczytowym, zapewnienie większej elastyczności w dostosowywaniu poszczególnych kanałów odczytowych do zmiennych warunków pracy związanych ze zmiennym udziałem kontrybucji szumowych od różnych elementów systemu odczytowego (zarówno wewnętrznych, związanych z elektroniką, jak i pochodzących od zewnętrznych komponentów), zmienną temperaturą, obecnością prądów upływu oraz zmiennymi parametrami pracy układu w związku z efektami wywołanymi przez promieniowanie. W pracy podjęty został również temat wykorzystania przetwarzania różnicowego w kanale odczytowym, który, chociaż charakteryzuje się wyższymi szumami, poborem mocy oraz zajmowaną powierzchnią niż architektury typu „*single-ended”*, pozwala zredukować wpływ zakłóceń od zasilania i znacząco zmniejszyć sumaryczny poziom szumów toru przetwarzania ładunku. Inną istotną kwestią poruszaną w niniejszej rozprawie jest zapewnienie testowalności

jednorodności parametrów pracy wielokanałowych układów scalonych, których w rozbudowanym systemie odczytowym może być nawet kilkanaście tysięcy, poprzez opracowanie zintegrowanego układu do pomiaru potencjałów oraz napięć zasilania wewnątrz układu.

Wymagania dotyczące zwiększania przepustowości transmisji danych, przy równoczesnym ograniczeniu na ilość linii transmisyjnych (przewodów) w systemach odczytowych detektorów promieniowania są przyczyną, dla której wielu projektantów elektroniki przeznaczonej do celów Fizyki Wysokich Energii rozważa możliwość wykorzystania nowszych technologii submikronowych (w których długość kanału tranzystora jest poniżej 100 nm) w celu przyśpieszenia pracy nadajników integrowanych w części cyfrowej elektroniki odczytu. Autorka przeprowadziła również badania w kierunku wykorzystania nowszych technologii niż dotychczas używane w elektronice przeznaczonej do zastosowań w Fizyce Eksperymentalnej (najczęściej 0.35 μm, 0.18 μm lub 0.13 μm ze względu na dostępność, cenę, a także stabilność i dojrzałość procesu i weryfikację pod kątem zachowania w obecności promieniowania) do zaprojektowania nadajnika (*transceiver)* pozwalającego na Multi-Gigabitową transmisję danych. Badania skupiły się na możliwościach technologii 28 nm i zaprojektowaniu najważniejszej części układu transmisji danych, czyli pętli fazowej (*Phase Locked Loop, PLL)*, z zapewnieniem odporności na uszkodzenia radiacyjne.

Praca zawiera opis kilku rozwiązań istotnych problemów występujących w układach odczytowych detektorów promieniowania, takich jak układ kompensacji prądów upływu, po raz pierwszy w połączeniu z szybkim resetem wzmacniacza ładunkowego, projekt układu do monitorowania wewnętrznych potencjałów w układzie scalonym, a także opracowane rozszerzone modele sensorów i innych elementów systemu, wykorzystywane w celu optymalizacji symulacyjnej elektroniki odczytu.

Rezultatem prac badawczych są trzy układy scalone. Dwa z nich to wielokanałowe, analogowe układy odczytowe o konfigurowalnych parametrach pracy (jak np. typ filtra kształtującego i czasu kształtowania), zawierające zarówno kanały o architekturze unipolarnej, jak i różnicowe. Zostały one zaprojektowane i wyprodukowane w technologii 180 nm CMOS. W układach tych zaimplementowane zostały opracowane metody kompensacji prądu upływu oraz kilka innych rozwiązań pozwalających poprawić parametry szumowe, jak również uodpornić układ na zakłócenia z linii zasilania oraz na efekty radiacyjne. Praca przedstawia i omawia wyniki pomiarów tych układów. Trzeci projekt to układ analogowej pętli fazowej zaprojektowany w technologii 28 nm CMOS, pod kątem wykorzystania w projekcie nadajnika przeznaczonego do pracy w obecności silnych pól radiacyjnych.

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Acronyms and abbreviations

CBM – Compressed Baryonic Matter

CCP – Complex Conjugate Poles

CSA – Charge Sensitive Amplifier

DLL – Delay Locked Loop

ENC – Equivalent Noise Charge

INL - Integral Non-Linearity

MBU – Multiple Bit Upset

PLL – Phase-Locked Loop

PS – Power Supply

PSRR - Power Supply Rejection Ratio

RHBD – Radiation-Hardened-by-Design

RHBP – Radiation-Hardened-by-Process

SEB – Single Event Burnout

SEE – Single Event Effect

SEFI – Single Event Function Interrupt

SEGR – Single Event Gate Rupture

SEL – Single Event Latch-up

SES – Single Event Snapback

SET – Single Event Transient

SEU – Single Event Upset

TID – Total Irradiation Dose

Introduction

Semiconductor detectors are widely used in various applications for example in the High-Energy Physics Experiments, that have been developing recently creating a need for more and more technically advanced and complex detection systems. Such systems, being currently built for such experiments as ALICE (A Large Ion Collider Experiment) in the European Organization for Nuclear Research (CERN) (Geneva, Switzerland) or CBM (Compressed Baryonic Matter) in Facility for Anti-Proton and Ion Research (FAIR) (Darmstadt, Germany) require an increase in the charge and time measurements resolution as well as faster data transmission, especially in the self-triggered systems. This research work conducted as the PhD project was focused on the requirements for the readout electronics based on the example of the CBM experiment, being developed as one of four experiments at FAIR. The most challenging requirements for this application include providing high operation speed of the readout channels (to process the interactions occurring at up to 10 MHz rate for high beam energies), even at the presence of large leakage currents, good parameters uniformity among the channels (a large number of multichannel readout integrated circuits), low noise, good immunity to temperature variations, interference coupling, magnetic and radiation fields and a possibility to adjust to the variation of the environmental conditions. Additionally, the power dissipation and occupied area are also limited, which makes meeting of all of the requirements even more difficult. The event-based charge processing applied in this experiment requires a high data throughput and fast transmission to the top-level data acquisition system. The number of data links should be preferably low, which requires even faster transceivers operation. As these circuits will also operate within a high radiation field, they should be robust to the radiation-induced effects as well.

This work aimed to design a prototype, multichannel integrated circuit implementing some of the novel ideas to meet all of the requirements for the CBM silicon strip sensors readout. The test ASICs were designed to provide lower noise, better adaptability to variable external conditions and to mitigate some of the effects, for example, those related to the leakage current and making achieving the high charge processing rates impossible. The second part of the doctoral project was research towards a further increase in the data transmission speed for High-Energy Physics experiments by employing newer technologies (below 100 nm). The research towards radiation-immune and still very fast data transmission was done basing on the most important circuit for the SERDES transceivers for such applications - a Phase Locked Loop (PLL).

The thesis is divided into six chapters, that are shortly described below, and contains one Appendix. The chapters content is as follows:

Chapter 1 presents the background for the theses and the concepts presented in the dissertation, the application field as well as the principles of radiation measurements. It contains also a short introduction into radiation-related effects in the electronic devices and defines the most common problems and

challenges for the design of the readout electronics dedicated to the semiconductor strip sensors basing on the Compressed Baryonic Matter experiment (Darmstadt, Germany) example. The literature overview both related to the analog charge processing and the phase-locked loops for the fast data transmission in a harsh environment are also included.

Chapter 2 addresses the challenges discussed in the first chapter and shows the possible solutions that can be applied in the front-end analog electronics for the silicon strip sensors readout.

Chapter 3 concerns the design of the first multi-channel prototype (SMX_mini) for the silicon sensors readout that is based on the requirements for the CBM experiments and implements some of the concepts presented in the previous chapter. The description of the Application Specific Integrated Circuit together with the measurements results is presented.

Chapter 4 is a description of a second ASIC (PRINCSA) designed and fabricated as part of the PhD project. This integrated circuit contains additional features implemented for further performance and noise level optimization. The simulation and measurements results are shown.

In **Chapter 5** a design and simulations of the Phase Locked Loop (PLL) for the Multi-Gigabit Transceivers dedicated for data transmission in the detectors readout systems is presented. Simulated performance in the presence of Single Event Effects on various sensitive nodes is also verified and the results are included in this chapter.

The summary of the works included in this PhD project, some conclusions and possible chances for the future development of the presented concepts are included in **Chapter 6.**

Appendix A is a list of the PRINCSA ASIC configuration registers.

Chapter 1 Radiation detection systems

1.1. Physical principles of radiation detection systems

1.1.1. Radiation environments and interaction with matter

Since many decades, integrated circuits (ICs) have been widely employed not only in commercial and every-day usable electronics, but also special applications for space, High-Energy Physics, military and medical devices, or nuclear industry. Each of these environments contains specific sources of radiation of various types. The radiation environments can be divided into natural (terrestrial and space environments) and man-made (nuclear power plants, high-energy physics experiments).

1. **Space:**
    - Trapped electrons and protons in the Earth's radiation belts,
    - Protons and heavy ions produced by the solar particle events (SPE),
    - Galactic cosmic rays (GCR) protons and heavy ions,
    - Particles trapped within planets magnetospheres [1], [2], [3];
2. **Terrestrial environment**
    - Atmospheric neutrons,
    - Alpha particles (radioactive contaminants in chip materials) [1];
3. **High-Energy Physics:**
    - High energy protons and electrons (e.g. 100 MRad[Si]/year – LHC [1]),
    - Neutrons (e.g. $5x10^{14}$ neutrons per cm^2 after 10 years of operation [4])
        - Examples of research centres: Organization for Nuclear Research (CERN), Switzerland, Facility for Antiproton and Ion Research (FAIR), Germany, Variable Energy Cyclotron Centre (VECC), Kolkata, India, Argonne National Laboratory or Fermi National Accelerator Laboratory (Fermilab), Chicago, United States ;
4. **Nuclear Applications:**
    - **Radiation type**: neutrons, X-rays, gamma-rays,
    - **Sources:** fuel fabrication plants, fission reactors, fuel reprocessing facilities, radioactive waste storage, power plants decommissioning [3];
5. **Military Applications:**
    - **Radiation type:** X-rays, gamma-rays, neutrons,
    - Nuclear explosions – an electromagnetic pulse (EMP), initial or residual nuclear radiation (INR/RNR) in the Earth atmosphere;
6. **Medical and Industrial Applications:**
    - Proton therapy and hadrontherapy (cyclotron radiation),
    - Medical irradiation (sterilization),
    - Food, water and waste irradiation,

- Microelectronics fabrication – ion implantation [3].

In the High-Energy Physics (HEP) experiments, a detection station contains from tens to tens of thousands readout chips, which is equivalent to up to millions of readout channels. The radiation produced by particle accelerators can be of various types and very high rates, that can cause serious damage for detectors and electronic components. The detectors and front-end electronics are very often located close to the interaction point and are required to maintain the parameters within the entire experiment time (for example 10 years, depending on the dose rate [5]).

For a better understanding of radiation measurement and imaging principle as well as damaging effects of the radiation sensors and readout electronics in these applications, the interaction of radiation with matter basics are discussed below. Figure 1 presents the classification of radiation types according to the mechanism of interaction with matter. The main two categories are ionizing and non-ionizing radiation. Ionizing radiation causes direct ionization of the matter atoms by temporal separation of their electrons, that as a result become free electrons. This happens when the energy transferred by a charged particle is higher than the ionization energy of the atom, which is equal to 3.6 eV for silicon. The ionizing radiation effects can be further divided into directly and indirectly ionization phenomena. Directly ionizing radiation like alpha or beta particles interacts with matter through Coulomb forces between those charged particles and electrons of the target material. The indirectly ionizing radiation, like neutral particles (neutrons, neutrinos) or photon radiation does not interact with the electrons in the atoms. For neutrons interaction, different mechanisms occur - “neutron capture”, which converts the nuclei to different isotopes, that as a result of instability may decay to lighter elements emitting secondary radiation (heavy charged particles) [6]. Photons interact with atoms in a different way than Coulomb forces due to lack of weight and charge. Instead, as a result of these interactions, secondary electrons appear that can act similarly to the fast electron radiations [7]. The low energy electromagnetic radiation (i.e. radiation with frequencies below 1016 Hz corresponding to 30 eV [8]) does not interact with the matter due to low energy per quantum (photon energy) and is known as non-ionizing radiation [9].

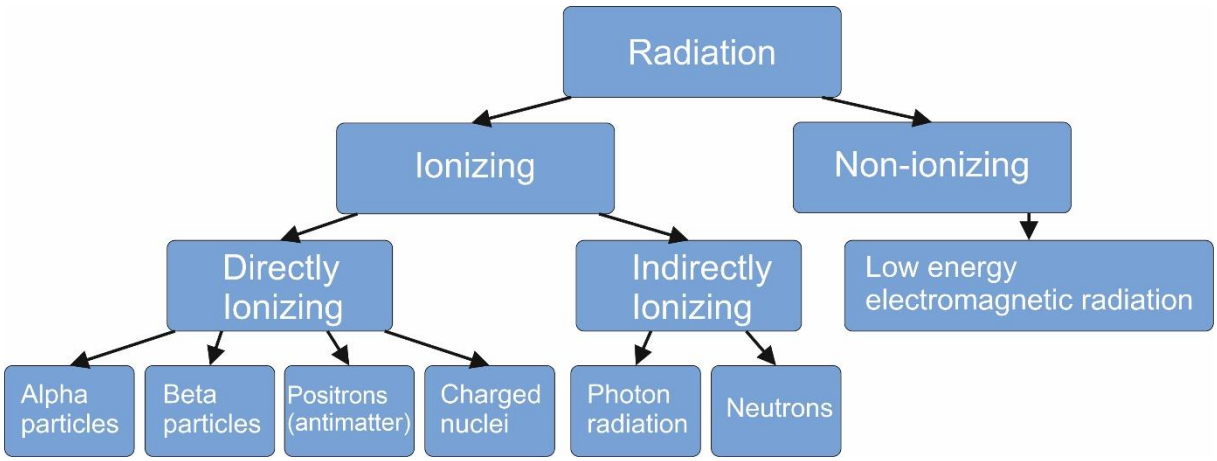


Figure 1 Radiation interaction with matter - classification.

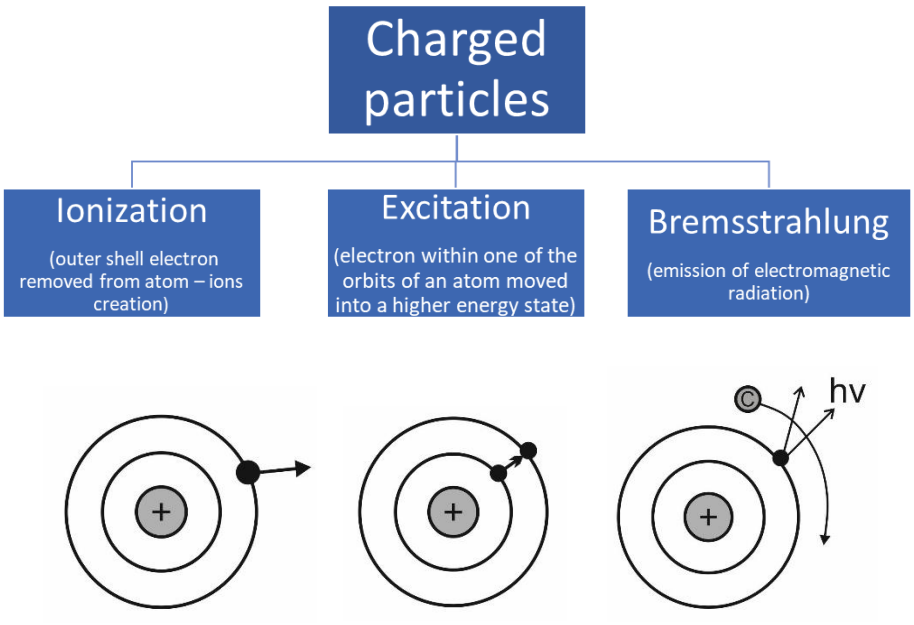


Figure 2 Charged particles interaction with matter - direct ionization. [6], [10].

Charged particles such as alpha, beta particles, electrons or recoil atoms can interact with matter leading to ionization or excitation of atoms (Figure 2). The main difference between these two phenomena is that in the first one the electron from the outer shell is removed from the atom and two ions are created, whereas the second one consists in moving an electron within one of the orbits into a higher energy state. The free electron resulting from ionization carries energy from the interaction and it can travel in the medium leading to ionization of other atoms in the matter, while the positively charged atom will eventually attract some free electron returning to its neutral state. The excitation leads to emission of a photon with energy equal to a difference in the energy states when the affected electron returns to its original state [10]. Another way of interaction of charged particles with matter is caused by their movements in a potential field – due to the electric forces, the trajectories of these particles bend leading to the emission of electromagnetic radiation known as "bremsstrahlung" and as a consequence secondary ionization effects [6]. This kind of electromagnetic radiation is classified neither an X-ray nor gamma-ray because of its different origin [10].

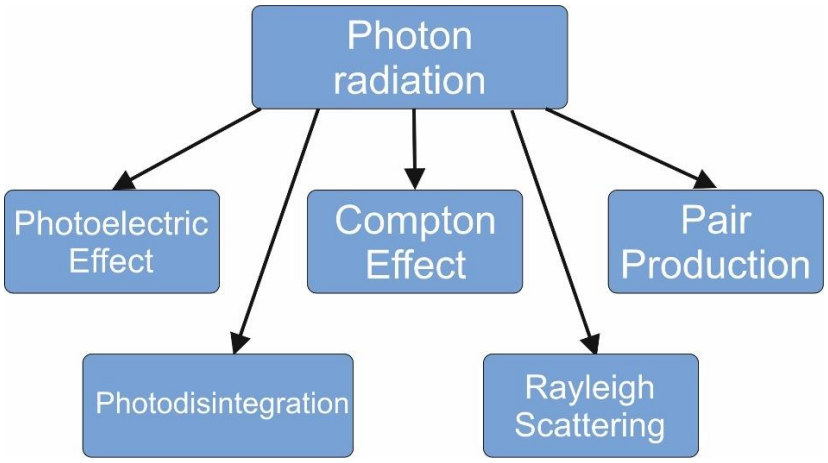


Figure 3 Photon radiation interaction with matter - indirect ionization. [10], [11].

Photon radiation can interact with the material in various ways and the most important processes for radiation detection and imaging are photoelectric absorption, Compton effect and pair production (Figure 3) [7], [11], [12]. As shown in Figure 4, the dominant effect depends on the photon energy and is also related to the material atomic number (Z). Photoelectric effect dominates for the lowest photon energies (for Silicon with Z=14 up to several tens keV), for medium energies (up to approximately 10 MeV for silicon), and for the highest values, the dominant process is electron-hole pairs production [7].

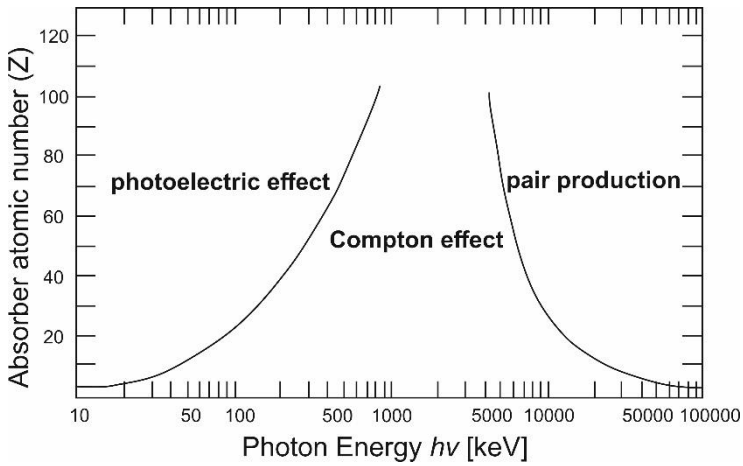


Figure 4 The three major types of electromagnetic radiation interactions with matter (based on [7]*).*

The phenomena discussed above are schematically illustrated in Figure 5. In the photoelectric absorption (Figure 5 a)), the surface electrons are ejected and the energy of the incident photon is completely absorbed. The interacting photon disappears and a photoelectron is created. The photoelectron is further ejected from one of the atom shells (usually K-shell) with energy equal to the of incoming photon minus binding energy for electrons in this particular shell (for low Z-material around few keV [7]). The vacancy in the atom-shell is filled by the capture of a free electron or by an electron from next shell (electrons rearrangement) and a characteristic X-ray photon is released. Sometimes, an Auger electron may appear, instead of X-ray, that carries away the energy of excitation [7], [13].

The Compton effect, or Compton scattering (Figure 5 b)), occurs between the photon and a loosely bounded electron from the atom. The photon passes a part of its energy to the electron and is deflected by an angle θ. The resting before collision electron receives a portion of energy related to the θ angle and is rejected from the atom (a recoil electron) [7], [12], [13].

Photons carrying energy, that is twice the rest mass of the electron (0.511 MeV) can interact with the material and as a result, the electron-positron pairs are created [12] as shown in Figure 5 c). If the interaction occurs within the atomic nucleus field, the electron-positron pair with the kinetic energy of the gamma-ray photon minus approximately 1.02 MeV replaces the incident photon. When the positron recombines with an electron in the material (annihilation process), two photons are emitted [7], [12].

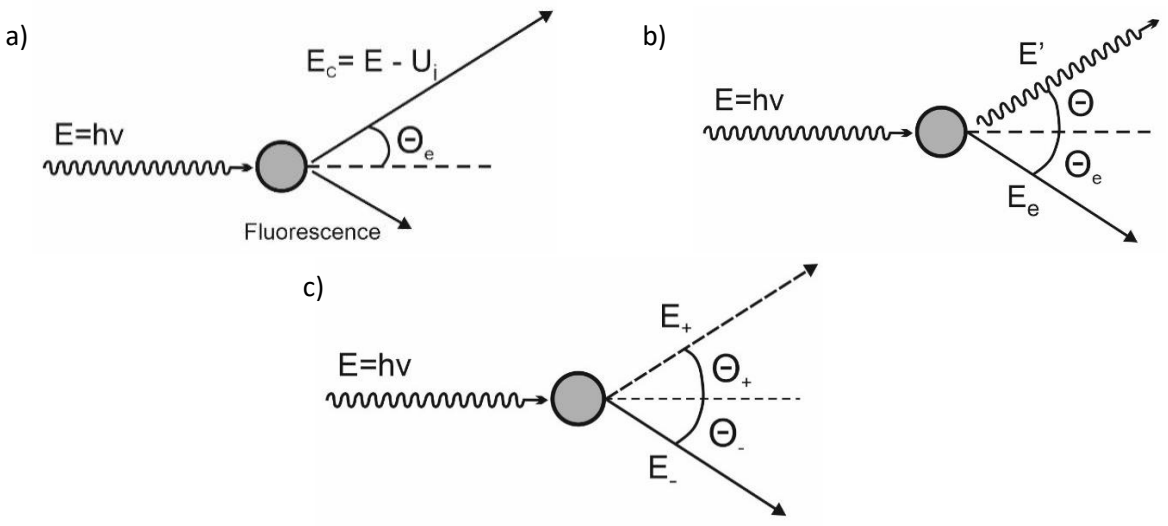


Figure 5 Mechanisms of the photon radiation interaction with matter; a) photoelectric effect, b) Compton effect, c) pair production.

Additionally, two different phenomena may occur. In the coherent or Rayleigh scattering the gamma radiation interacts with all the electrons in the atom without exciting or ionizing the atom. The gamma-ray photon does not change its original energy, so no energy is transferred and this process may be neglected [7]. Photodisintegration is a type of a photonuclear reaction. In this reaction, a photon is captured by the nucleus, resulting in nucleus de-excitation with the emission of neutrons typically. Similarly, as in the photoelectric effect, the energy of incident photon should exceed a threshold value (binding energy of a nucleon) significantly [12], [13].

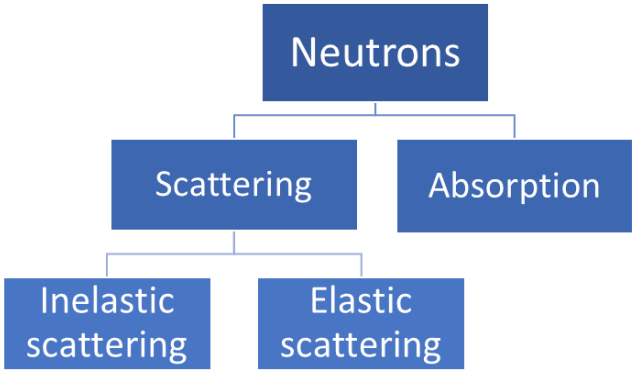


Figure 6 Neutrons radiation interaction with matter - indirect ionization.

Neutrons interact with matter through two main types of reactions: scattering and absorption (Figure 6). Scattering can be divided into inelastic and elastic. In inelastic scattering, an incident neutron excites a nucleus in the material. The neutron is absorbed by the nucleus and immediately emitted, causing a return to the neutral state of the nucleus, and emission of photons (gamma rays) [13]. The threshold for this kind of interaction is usually around few MeV and the cross-section is typically low [10].

During elastic scattering, fast neutrons slow down scattering off various nuclei and reaching eventually thermal energies. Such thermal neutrons can be the most likely captured and the scattered nuclei turn into ionizing particles (typically H nuclei – fast protons) [10].

Absorption process occurs when the nucleus absorbs the neutron and enters excited state. During the return to the primary state, a photon or a particle is released. The first process is a radiative capture, whereas the second one is called a charged particle reaction [13]. The absorbed neutron may cause various radioactive disintegration reactions [10].

1.1.2.Principles of radiation measurements and imaging

In semiconductors, the valence band, corresponding to the electrons bound in the crystal lattice, and the conduction band representing the free electrons, are separated by the bandgap (Figure 7). In the case of silicon, the bandgap is equal to 1.12 eV [7]. Any temperature different than 0 K increases the probability, that a valence electron gains thermal energy that is sufficient to elevate it to the conduction band. In this excitation process, an electron in the conduction band and a hole (a vacancy) in the valence band are created. The applied electric field causes these electron-hole pair to move and each charge migrates to the opposite direction. This effect can be observed as an increase of the material conductivity [7].

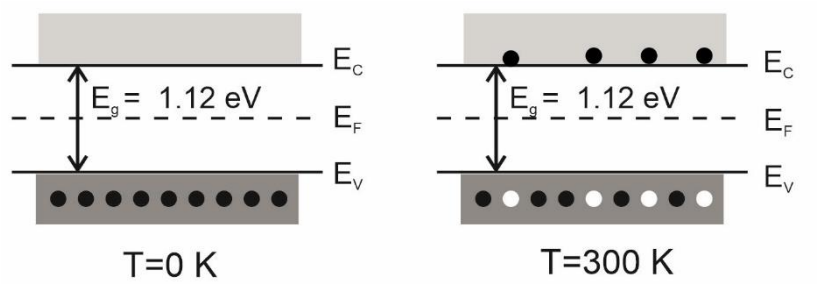


Figure 7 Band structure of silicon with the electron population in two different temperatures.

The assumption, that all electrons in the conduction band and an equal number of holes in the valence band are due to thermal excitation, is true only for ideally pure semiconductors (known as "intrinsic semiconductors"). In practice, each material contains a small level of impurities (even silicon, that is available in the highest purity), that determine its electrical properties [7]. Intentionally introduced impurities that are trivalent or pentavalent (whereas silicon is tetravalent), create localized energy levels in the bandgap (Figure 8). These atoms are called acceptor and donor impurities respectively. The acceptor atoms increase the probability of recombination between introduced holes and conduction electrons, whereas donor atoms introduce additional electrons in the bandgap, that can easily move to the conduction band [7], [14]. Semiconductor doped with acceptor atoms becomes a p-type semiconductor, whereas the material containing donor atoms is called an n-type semiconductor.

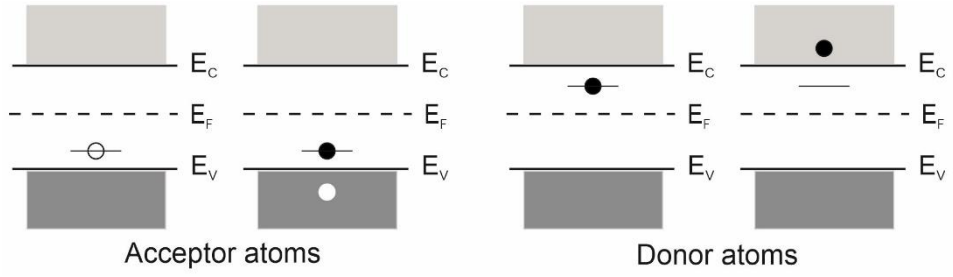


Figure 8 Creations of states in the silicon bandgap.

A semiconductor detector is a reverse-biased junction of n- and p-type semiconductor, and the active sensing volume is a depletion region created at the junction. Free charge carriers migrate across the junction causing net charge (space-charge also known as depletion region) formation, that can be further extended across the silicon wafer bulk by a reverse bias voltage [15]. The radiation interacts with semiconductors causing the creation of electron-hole pairs. The radiation energy fraction that is converted into generated charges is weakly dependent on the radiation energy and type, assuming energy values higher than the bandgap. The created electron-hole pairs move in the electric field towards the electrodes connected to the semiconductor material. The movement of generated charge carriers contributes to a current pulse, according to Shockley-Ramo theorem [16], that is a principle of deposited charge measurements as an electric signal [7], [14], [15]. The measured signal fluctuates around a mean value N for a particular radiation energy E, where ϵ is the mean energy spent for creating a single electron-hole pair :

$$N = \frac{E}{\epsilon} \quad (1)$$

In Silicon, in presence of the relatively low field, the mobility of charges is constant and is equal around 1350 cm^2/Vs and 480 cm^2/Vs for electrons and holes respectively (at T = 300 K) [17].

1.1.3. Sensors and readout electronics

Semiconductor detectors used in radiation detection and measurements applications such as particle physics experiments, X-ray imaging (for example medical imaging or material science). Taking into account the criteria for detector material selection, such as economic issues, a possibility for integration with readout electronics, radiation hardness and low leakage current at room temperature, other good examples are Germanium (Ge), Gallium Arsenide (GaAs), Cadmium Telluride (CdTe), Cadmium Zinc Telluride (CdZnTe) and Diamond. The most widely used material for semiconductor detectors, especially in tracking detection stations, is silicon, thanks to its low atomic number, well-known and stable fabrication technology. Silicon application is however limited for X-ray applications to only low energy photons [7], [12], [17]. Reasonably high charge carriers mobility in silicon at room temperature (1350 cm^2/Vs for electrons and 480 cm^2/Vs in case of holes) allows achieving short charge collection times (in the order of 10 ns for 100 μm thickness), which makes it a good choice for high-rate experiments application [7]. However, some materials, like for example germanium (3900 cm^2/Vs – electrons and 1900 cm^2/Vs – holes) or gallium arsenide (8000 cm^2/Vs – electrons, 400 cm^2/Vs - holes), provide faster charge mobilities, but also a higher atomic number, so the selection of particular material is dictated by the specific application [14], [17]. Depending on the specific application and related spatial and energy resolution requirements, Position-Sensitive Detectors (PSD) can be fabricated in various geometries [17], [18], [19]:

- Single-sided (Figure 9) and double-sided (Figure 10) strip detectors;
- Pixel detectors: Charge-Coupled Device (CCD), monolithic pixel detectors, silicon on insulator (SOI) pixel detectors, hybrid pixel detectors (Figure 11);
- Pad detectors.

The PSD sensors comprise many individual sensors placed in an array, usually readout by single analog front-end electronics channel separately. Detectors differ not only in shape but also in thickness, pitch, type of bulk silicon (p or n) and its resistivity, biasing structure, coupling (AC or DC) or readout connection type [15].

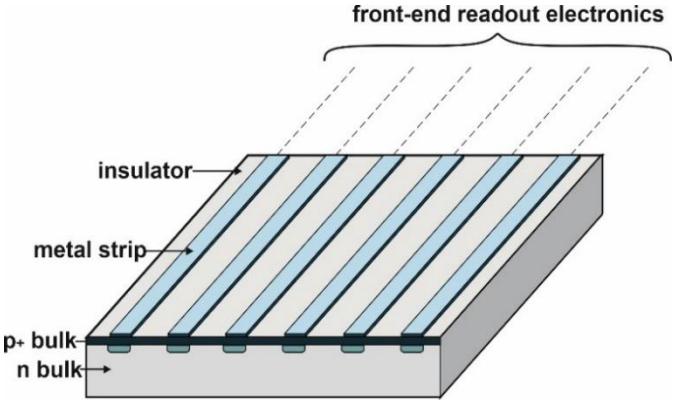


Figure 9 Single-sided semiconductor strip sensor with AC coupling.

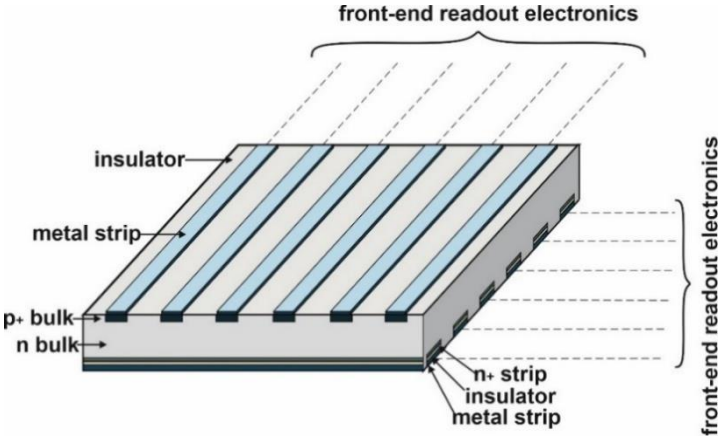


Figure 10 Double-sided semiconductor strip sensor with the orthogonal layout.

Single-sided strip sensors used for particle physics and X-ray spectroscopy and imaging systems, contain a small number of channels and provide one-dimensional measurements [17], [18]. A typical strip pitch is from around 10 μm to 200 μm. The strip sensors are usually AC-coupled to prevent from quite large leakage currents [18]. To provide two-dimensional tracking measurements, several layers of microstrip sensors with certain stereo angle can be applied, or a double-sided detector (with tilted strips on two sides, Figure 10) can be used [19]. The problem of "ghost hits" limits the usage of crossed-strips 2D detectors to only low-intensity radiation applications [17], [20]. The two-dimensional sensor provides n^2 hits acceptance fields, where n-number of strips per single side, so multiple simultaneous hits can cause ambiguities and n^2-n false hits ("ghosts") [20].

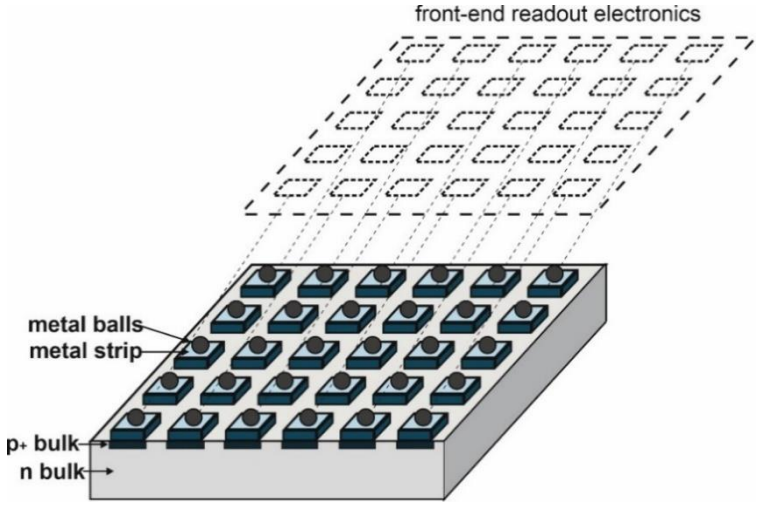


Figure 11 Hybrid pixel sensor.

To eliminate "ghosting" problem and enable true two-dimensional measurements, pad and pixel detectors were developed. The difference between these two geometries is only the size of a single electrode, but the exact distinction is arbitrary. Generally, the segmentation of pad sensors is coarse and the number of channels is limited, whereas for pixel detectors, the sensing elements are much smaller and each of them is directly connected to one readout electronics channel (this kind of detector is known as a hybrid pixel detector – see Figure 11). An area of a single pixel is between approximately 50 μm x 50 μm [21] to around 200 μm x 200 μm [22]. In the case of pixel sensors, the leakage current is usually small, so AC-coupling is not required [18].

The signal from the detector in the form of a current pulse is processed by front-end electronics, that provides pulse amplification and shaping for further acquisition and processing by a top-level data acquisition (DAQ) system. Depending on the application and type of acquired information (hits counting, time or amplitude measurements) there are a few possibilities of the readout electronics design [17], [23]:

- **Current mode** – the input stage time constant is shorter than the charge collection time (small input resistance); the current pulse is being processed by the readout electronics in its original shape (True Current Mode) or is forwarded in the modified form ensuring that the maximum signal power is not changed (Semi-Current Mode);
- **Voltage mode -** the input time constant is significantly longer than the charge collection time (high input resistance); the shape of the current pulse from the detector is not preserved and its amplitude can be higher than in the current mode,
- **Mode with charge sensitive amplifier (CSA)** – current signal generated in the detector is integrated and amplified, the amplitude of the CSA output signal (a voltage step) is proportional to the total charge generated in the sensor material by an ionizing particle.

The CSA is followed by a shaping amplifier that provides signal shaping given the timing performance requirements and noise filtering for better signal to noise ratio (SNR). The shaper output signal can be processed afterwards in various ways such as [15], [17]:

- **Binary readout** – provides 1-bit yes/no information about the incoming hit, usable in the applications where no energy information is required for each hit; in the single-photon counting applications additional energy information is provided by the implementation of energy window for each pixel employing more than one discriminator with different threshold levels,
- **Analog-to-digital conversion (ADC)** – for measurements of signal amplitude (generated charge),
- **Time-to-digital conversion (TDC)** – for measurements of hit occurrence time [15], [17], for example Time-of-Flight (ToF) measurements employing Time-of-Arrival (ToA) counter [24].

Usually, each detector element (strip or pixel) is connected to one front-end electronics channel. For the strip sensor readout, multichannel analog front-end integrated circuits are dedicated and the whole detection system is comprised of multiple sensor-readout electronics modules.

After a current pulse is integrated in the mode with Charge Sensitive Amplifier, its feedback capacitor needs to be discharged for further incoming charges processing. Various types of CSA feedback configuration can be employed, depending on the specific requirements regarding charge processing linearity, desired noise level (as the feedback is directly connected to the input of the charge processing chain and its noise contribution should be minimized), input hits processing rate and allowed maximum leakage current that may appear in the system. Generally, the CSA feedback can be realized using two different methods for capacitor discharge: switched (discrete) or continuous. The first approach (Figure 12a) can be realized through a MOS switch triggered externally (for example derived from the system clock) or internally using a signal generated in the individual channel at the end of charge processing phase [17] or its version used in the active pixel sensor configuration (APS) [25]. The simplest version of the continuous discharge is a large resistor (in the range of tens to hundreds of megaohms) – see Figure 12b. This is, however, usually not applicable in nanometer-scale multichannel ICs, due to integration difficulties like for example large area or parasitic capacitance of a resistor on silicon bulk. A practical implementation is a single MOS transistor working in triode or saturation region (Figure 12c). Other possibilities include a controlled current source (for example slew-rate limited feedback based on a current mirror and a current source, Figure 12d), R-scaling circuits (current conveyor feedback, Figure 12e) [17], [25]. Another way of feedback implementation is by using a differential stage, known as a leakage compensation Krummenacher circuit (Figure 12f) [17].

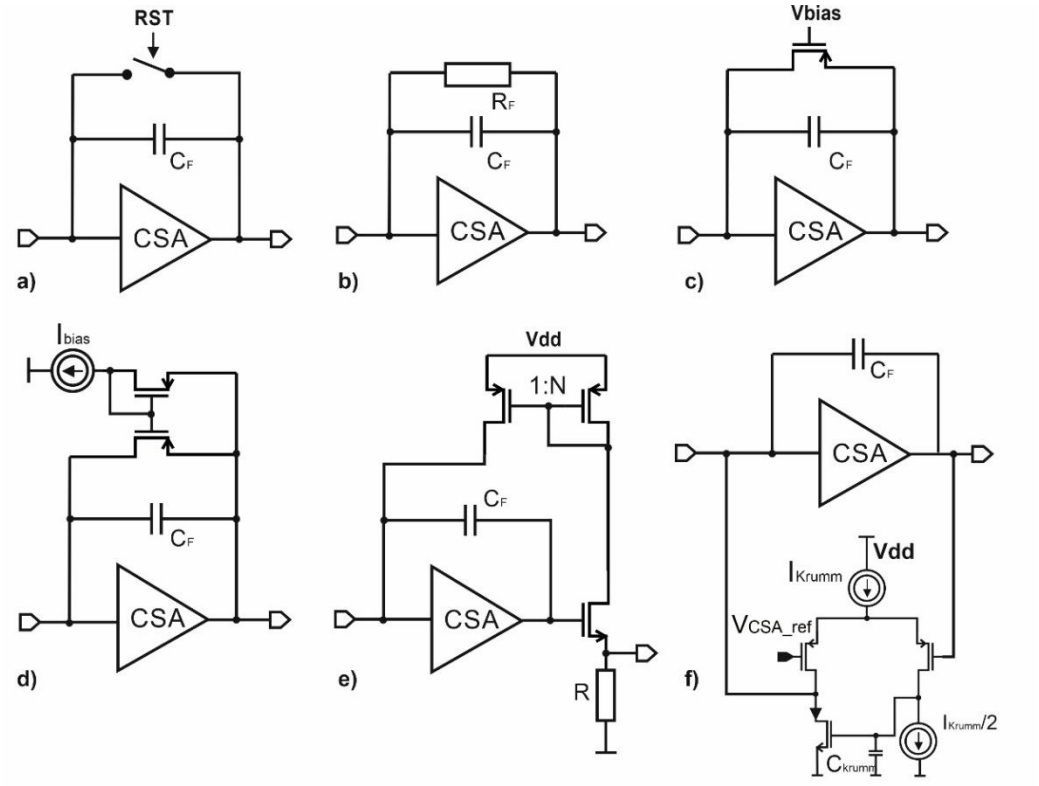


Figure 12 Integrated reset configurations for periodic and continuous reset.

1.2. Compressed Baryonic Matter experiment at FAIR

The Compressed Baryonic Matter (CBM) experiment is one of the four experiments that are currently under development at the Facility for Anti-Proton and Ion Research (FAIR) in Darmstadt, Germany [5] - Figure 13.

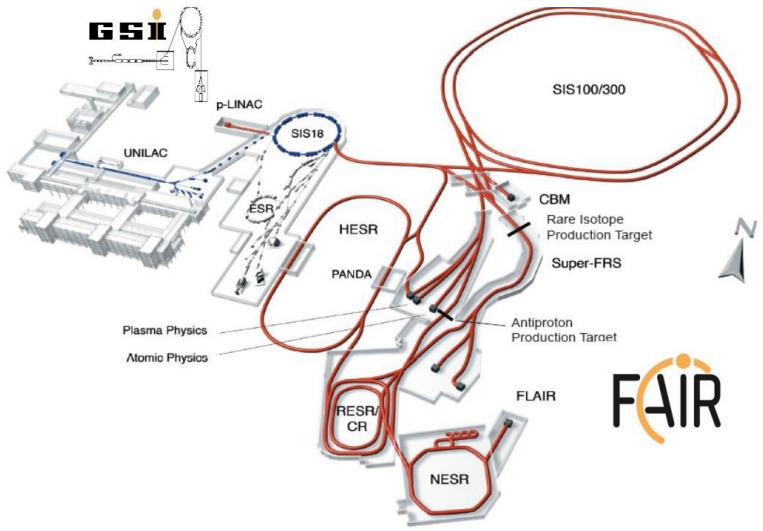


Figure 13 The Facility for Antiproton and Ion Research in Darmstadt, Germany. https://fair-center.de

The aim of this experiment is the exploration of the QCD (Quantum Chromodynamics) phase diagram of matter at high baryon-net densities and for moderate temperatures [26], [27]. The heavy-ion

collisions will occur at an unprecedented rate – up to 10 MHz interactions at high beam energies [26]. The CBM experiment setup consists of a superconducting 1 Tm (field integral) dipole magnet and the following detection stations:

- Micro Vertex Detector (MVD),
- Silicon Tracking System (STS),
- Time-of-Flight (TOF),
- Ring Imaging Cherenkov Detector (RICH),
- Transition Radiation Detector (TRD),
- Muon Chamber (MuCh),
- Projectile Spectator Detector (PSD).

The experimental setup contains also a First-Level-Event-Selection (FLES) system dedicated for online selection and reconstruction of events [5], [26]. The STS detection station for tracking, momentum determination of the charged particles and particles decays identification [28], comprises of 8 tracking stations located within a dipole magnet and placed in the distances between 30 cm and 100 cm from the target [5]. Each station will be built of 320 μm thick micro-strip double-sided silicon sensors of lengths ranging from 22 mm to 124 mm, containing 1024 strip per side (p-strips and n-strips) and segmented with a strip pitch of 58 μm. The strips on one side will be tilted by 7.5◦ stereo angle with respect to strips on the other side. The entire STS tracking station will comprise approximately 1.8 million readout channels. Each detector will be connected with the readout electronics boards via application-specific micro-cables of different lengths ranging from a few centimetres to approximately 55 cm [5], [28]. The silicon sensors will be placed on a lightweight carbon fiber ladders with front-end electronics attached at the top and bottom ends. To minimize the material placed in the detector's acceptance, the heavier electronics is attached outside the active area [26]. High interaction rates pose good radiation tolerance from all the system components. The increase in detector leakage current due to absorbed high irradiation doses may subsequently lead to the device thermal runaway. Therefore a proper cooling system is mandatory, to provide cooling of the sensors as well as the fast readout electronics, producing approximately 30-40 kW of thermal power that has to be dissipated. Taking into account also the space limitations, application of bi-phase CO_2 cooling is considered [26].

The readout chain of the STS detector consists of front-end boards (FEB) containing Application Specific Integrated Circuits (ASICs) dedicated for this experiment, readout boards (ROB) with GBTx chips (designed at CERN [29]), that provide control commands, reference clock and data acquisition and a common readout interface (CRI) for initial processing of acquired data. Hit data are subsequently transferred to the First Level Event Selector (FLES) computing system for tracks reconstruction [28].

1.3. Challenges for readout electronics for High-Energy Physics Experiments

A very high number of readout channels and count rate of the STS detector require the most careful and system-level-conscious front-end electronics design of the CBM experiment detection stations. The readout multichannel ASIC should enable a self-triggered operation within a harsh environment with high radiation doses (up to 100 krad per year [27]) and processing the input hits with very low Equivalent Noise Charge (ENC) for high track reconstruction efficiency (below 1000 e^- rms). Analog front-end electronics should provide amplitude (analog-to-digital conversion, ADC) and time (timing discriminator) measurements and digitization in each channel for charges of both polarities up to 10 fC, while keeping low-power operation (10 mW per channel at maximum) [5], [30]. As many of the requirements for the readout electronics are common for the STS and MuCh detectors, the readout ASIC can be designed for both of them. Extending the functionality of the front-end ASIC dedicated for the STS system poses, however, some difficulties – the sparks generated in gaseous detectors (GEM) from the MuCh station may be dangerous for sensitive electronics, so each channel should be protected from the electrostatic discharge (ESD). Design of an effective ESD circuit adapted for operation at various temperatures is challenging to provide as low as possible leakage from the used structure, low capacitance and enough protection at the same time. The analog front-end should be optimized in terms of intrinsic noise for a wide range of detector capacitances and to mitigate the influence of external noise sources by a set of filters with proper order and peaking time. The digital back-end should provide register access, data streaming and readout. Self-triggered system is particularly challenging for the data transfer design and poses requirements concerning faster transmission and higher throughput. Data is processed „on-the-fly" and sorted by the timestamp (resolution of 3.125 ns). Taking into considerations a large amount of ASICs operating simultaneously in the experiment, the time synchronization is required. The back-end should be also equipped with some diagnostic features like for example test hit generator, counting of missed events or masking of malfunctioning channels. The dedicated protocol for data transfer should be fully synchronous (deterministic) and based on for example 8b/10b encoding (as the data readout will be AC-coupled). Both analog front-end and digital back-end should be well protected from the radiation-induced effects. In the case of the analog part, the majority of issues are related to Total Irradiation Dose induced leakage. Both parts should be protected from the latch-up risk by proper radiation-immunity improving techniques on the layout level. The digital part should be made more immune to the Single Event Effects, by selecting the configuration memory cells architecture. The whole system is complex in terms of assembly and biasing, the readout electronics should be designed to maintain good parameters and enable the possibility of tuning to provide good uniformity between various channels [30].

1.4. Overview of existing designs for HEP experiments

Integrated circuits for radiation imaging and measurements applications, like for example HEP experiments, are required to keep their parameters while working in harsh radiation environment and being exposed to varying temperature and leakage current conditions. The research towards new solutions in the analog front-end electronics design and exploration of the benefits and drawbacks of more modern submicron technologies are driven by the system noise, chip area and TID-sensitivity minimization. Various radiation imaging and measurement applications share some common requirements regarding radiation-immunity and low noise, but a detailed analysis is necessary for each system due to sensors variety, desired charge processing channel sensitivity, input hit rate, timing performance, power and area limitations. Some of the most recent examples of silicon strip sensors read-out electronics are summarized in Table 1. The technology scaling and lower power supply limits the achievable gain of analog amplifiers and worsens the noise performance. To overcome these limitations and take advantage of increased speed, lower power and smaller area, some authors suggested employing gain-boosting techniques [31] - [32]**.** Depending on the dominating noise type contribution and timing requirements the architecture and shaper peaking time should be carefully selected [33] or, to provide more flexibility, made configurable. Some applications that require a very low noise performance and are dedicated for operation with low input hit rate use longer shaping times, for example [34], but most of the designs employ shaping times in the range of few tens up to few hundreds of ns, like [35]**,** [36]**,** [37]**.** Long shaper peaking times (μs range) can provide noise performance slightly above 100 e^- rms for an input capacitance of 4 pF [34], whereas values in the ns range usually reach noise levels of few hundreds e^- rms, exceeding 1000 e^- rms for very short times (for example 50 ns in [36]).

Table 1 Silicon strip sensors read-out examples

	[32] **(2013)**	[31] **(2014)**	**STS XYTER (2018)**	[36] **(2020)**	[34] **(2019)**	[35] **(2020)**
Technology	130 nm	90 nm	180 nm	180 nm	AMS 0.35 μm 3.3/5 V Mixed Signal	0.25 μm
Power supply	1.2 V	1.2 V	1.8 V / 1.2 V	1.8 V / 1.1 V	±2.5 V	2.5 V
Application	N/A	HYDE detector, FAIR, Darmstadt, Germany	Silicon Tracking System detector, GSI, Darmstadt, Germany	the J-PARC muon $g-2$/EDM experiment	TRacking Array for light Charged Ejectiles (TRACE) -a study of nuclear shell structure moving away from the valley of β stability	Silicon Vertex Tracker (SVT) for the CLAS12
Sensor type	Silicon strip	Silicon strip	Silicon strip	Silicon strip	Double-Sided Silicon Strip Detectors)	Single-sided microstrip sensors (by Hamamatsu Photonics)
Sensor capacitance	5 pF	5 pF	Up to 40 pF	17 pF	4 pF	20 pF (45 pF strip + bonds+ pitch adapter)
Charge processing manner	CSA (gain-enhanced), PZC, complex shaper with Gm-C topology	CSA, PZC, CR-RC shaper	CSA, fast CR-RC shaper, slow CR-RC^2, polarity selection circuit (PSC), fat path – comparator, slow path – 5-bit ADC	charge sensitive amplifier (CSA), a preamplifier, a CR–RC shaper, a differentiator, comparators for the CR–RC shaper and the differentiator with a reference voltage set by a 6-bit Digital-to-Analog Converter (DAC).	CSP with fast reset (Schmitt trigger + current source), semi-Gaussian shaping amplifier	self-triggered, time-stamped; a preamplifier, a CR-$(RC)_2$ shaper, a baseline restorer (BLR), and a 3-bit ADC
Power dissipation	4.4 mW/channel	750 μW/channel	<10 mW/channel (128 channels)	0.44 W total	11 mW/channel	4 mW/channel
Area	N/A	N/A	10.0 mm × 6.75 mm	6.58 mm × 7.24 mm	3.3 mm × 1.5 mm	7.5 mm x 5 mm
ENC	671 e^- rms (@ C_{det} = 5 pF), 122 e^- /pF	970 e^- rms (@ C_{det} = 5 pF)	673 e^- rms (@ C_{det} = 5 pF), 27e^- /pF + 538 e^- rms	1746 ± 57 e- rms (@ Cdet = 33 pF)	130 e− rms (@ C_{det} = 4 pF) – anodic ch/ 143 e− rms (@ C_{det} = 4 pF) – cathodic ch	375 e^- rms (@ C_{det} = 5 pF, t_p = 65 ns), 295 e^- rms (@ C_{det} = 5 pF, t_p = 125 ns) Max 1500-1600 e^- rms for C_{tot}
Peaking time	75, 150, 300 ns	75 ns	Slow: 90/180/262/332 ns	50 ns	10 μs	65, 85, 100, 125 ns
Sensitivity	N/A	N/A	Fast: 73 mV/fC, Slow: 32.7 mV/fC	N/A	0.2/0.5/0.7/1.0 mV/fC	120-160 mV/fC

1.5. Critical design issues and possible modifications

Design of the front-end electronics for radiation detectors readout should include handling of the critical design issues. The most challenging ones are ensuring low noise level, handling the leakage current, acceptable Power Supply Rejection Ratio (PSRR) and providing radiation-hardened architecture, that can withstand high radiation fields during the expected system lifetime. The aspects mentioned above will be shortly discussed in the following sections.

1.5.1. Radiation-related issues in sensors and readout electronics

Nuclear radiation, as discussed in Section 1.1, interacts with electron clouds and lattice nuclei of the material. Interaction with electrons, a transient effect, is the principle of radiation detection and measurements, but the interaction with the lattice can permanently change the material properties [14]. The phenomena that can be observed in all types of silicon devices due to irradiation are generally divided into three groups: bulk defects, surface defects and single-event effects (Figure 14).

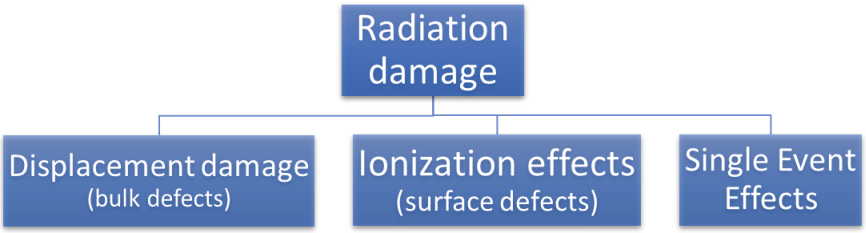


Figure 14 Radiation-induced damage in semiconductors

Silicon sensors are prone to bulk defects and surface defects. The first group is caused by high energy particles in a Non-Ionizing Energy Loss (NIEL) and leads to crystal atoms displacement (defects: interstitials – additional atoms between the lattice nodes and vacancies – missing lattice atoms) and generation-recombination centres resulting in additional energy levels in the silicon bandgap. Defects are mobile at room temperature and can be annealed partially, as there is a probability that an interstitial fills the vacancy, or they can be diffused out of the surface. Unfortunately, by interaction with other defects, stable defect complex may appear, that can alter the electrical performance of the sensor [14]. The most common phenomena in the semiconductor detectors are [14], [15], [17], [18]:

- increase of **leakage current** (the additional energy levels in a band-gap act as a generation-recombination centres that can emit and capture charges),
- **lower output signal amplitude** due to lowered mobility limiting the collected charge amount within the charge collection time (caused by charge trapping centres holding a part of the signal charge for a longer time) – a decrease of charge collection efficiency,
- **change of effective doping concentration** (n-type silicon bulk turns less n-type, in p-type silicon the positive carrier density grows),

- change of the detector **full depletion voltage** value (at the beginning decreases, once a type inversion is reached, that is an inversion of space charge sign, the voltage increases; change in the effective net impurity concentration),
- increase of the **interstrip/interpixel capacitance**, worse isolation between electrodes (especially in the case of double-sided sensors),
- increased current and operation voltage leading to increased power dissipation and heating of the sensor – proper cooling is mandatory, otherwise may lead to thermal runaway.

The surface defects are caused by Ionization Energy Loss and are related to the creation of electron-hole pairs in the covering dielectrics (e.g. the silicon oxide) and the silicon-dielectric interface [18]. The holes, that are lower mobility than electrons in the oxide, and may form permanent traps in the interface area, building up positive oxide charges [18]. Although these phenomena have no direct effect on the performance of the radiation sensors itself, they can alter the operation of the whole detector, causing for example [14], [15], [18]:

- increase of inter-sensors capacitance (and therefore increased noise level),
- flat band voltage shift,
- growth of the dark current,
- decreased immunity to breakdown.

The radiation-interaction mechanisms and damage effects for the readout electronics are similar to these appearing in the silicon sensors, as the technology used for both of these devices groups is also similar. The differences in the observed effects are related to different doping concentrations levels and different operating principles [14]. The radiation-induced effects differ for various devices groups, namely MOS transistors, bipolar transistors and JFETs. The main two groups of phenomena occurring in the MOS transistors are those related to Total Irradiation Dose (TID) and Single Event Effects (SEEs) - Figure 15.

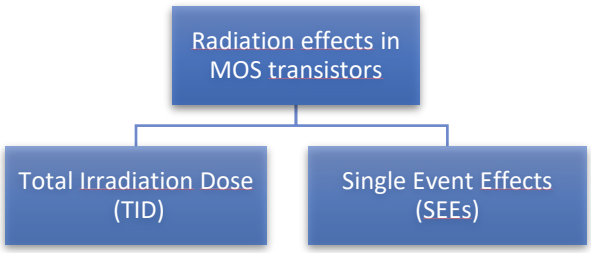


Figure 15 Main two groups of radiation effects in MOS transistors.

The first group of radiation-induced effects in MOS devices is caused by charge trapping in the transistors oxide (silicon dioxide, SiO_2) and on the Si/SiO_2 interface due to existing anomalies [38]. These effects are particularly harmful to the performance of analog circuits because they change the characteristics of the transistors and affect the whole device area. TID-related damage is a long term process, that is caused

by a cumulative dose of ionizing radiation, which leads to drift of the device parameters. Two mechanisms lead to a change of the transistor threshold voltage: charges generation in the oxide and a buildup of traps at the SiO_2/Si interface. Ionization of SiO_2 atoms and the amount of created electron-hole pairs depends on the particles energy and the minimum energy necessary to produce charge characteristic for a particular material. For the silicon, the minimum energy that is necessary to produce electron-hole pair is equal to 3.6 eV, whereas in the silicon dioxide this value is much higher and equals 18 eV [39]. Part of generated charge recombines almost immediately without any effect on the transistors' performance. As the mobility of electrons and holes in the silicon dioxide differs significantly (10^{-4} to 10^{-11} cm^2/Vs for holes and around 20 cm^2/Vs for electrons), the remaining electrons move fast towards the positively biased gate (considering NMOS transistor and p-type bulk), leaving the holes in the oxide. The positive oxide charges slowly migrate via localized states towards the silicon interface through a mechanism known as hopping, that is triggered by thermal phenomena and electric field across the oxide – see Figure 16. The positive charges remain trapped in the transistor material near the silicon/silicon dioxide interface and change the threshold voltage by a value inversely proportional to the gate oxide capacitance and directly proportional to the gate thickness (Eq. (2), (3)) [6], [17]:

$$V_{ot} = -\frac{Q_{ot}}{C_{ox}} \tag{2}$$

$$V_{ot} \propto {t_{ox}}^2 \tag{3}$$

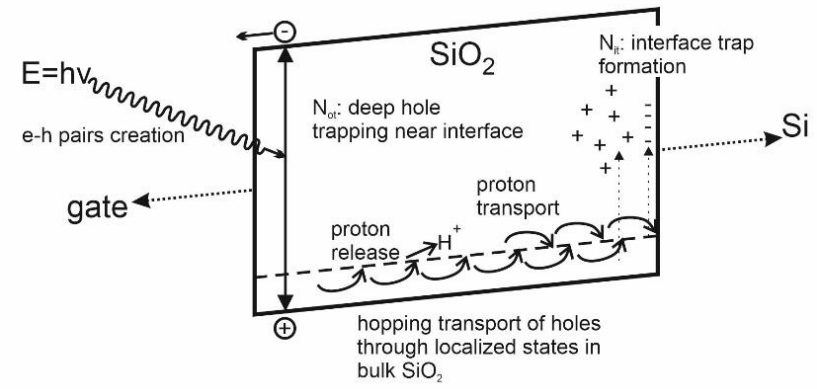


Figure 16 Mechanisms of charge trapping in MOS devices. [40]

Another effect caused by radiation is a buildup of traps near the interface, that can be of neutral, donor or acceptor type, depending on the transistor type. For NMOS transistors fabricated on a p-substrate, the energy levels of the bandgap are the most likely to be trapped by negative charges, since the fermi potential is below the mid-band energy. In the case of PMOS transistors placed in the n-well (n-type substrate), the positive charges are trapped, because the fermi potential is above the mid-band energy [6]. The overall threshold shift, including the oxide and interface charges, is expressed by Equation (4) :

$$V_{tot} = V_{ot} + V_{it} = -\frac{Q_{ot} + Q_{it}}{C_{ox}} \tag{4}$$

According to Equation (4), it can be observed that for PMOS transistors the threshold voltage moves towards larger (negative) values because both gate oxide and interface traps have the same sign (Figure 17). For NMOS transistor the threshold voltage shift depends on the dominating charge trapped in the gate oxide or interface. Initially, the voltage shifts toward lower values as oxide traps dominate, while with the growing impact of the interface traps, it starts increasing [17].

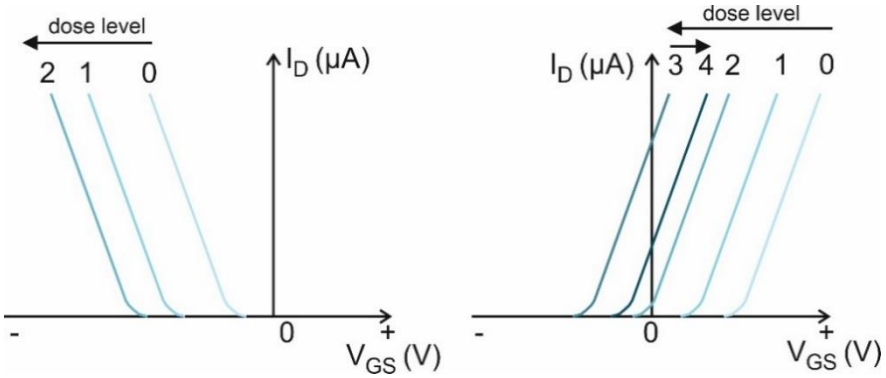


Figure 17 Threshold voltage shift for a) PMOS, b) NMOS.

As a consequence of the decrease in the NMOS threshold voltage, the leakage current increases significantly [6]. Due to interface traps (especially so-called border traps, that can exchange charge with the underlying channel), the flicker noise increases [3]. Reduced carriers mobility in the channel cause drop in the transistor transconductance, that leads to a growth of thermal noise (the spectral density inversely proportional to the channel transconductance) [3]. As the voltage shift is directly proportional to the oxide thickness, it has a significant impact mostly on older technologies (transistors length larger than approximately 130 nm [33]). For example, in 0.35 μm the threshold voltage shift for the total accumulated dose of 300 krad equals -18.7 mV and -60.3 mV for PMOS and NMOS transistors respectively, each of them of minimum channel length [41], whereas in 28 nm technology for the standard V_{th} NMOS with the minimum channel length (30 nm) the voltage shift is around -20 mV for 100 Mrad [42].

Among other effects induced by the accumulative radiation dose, two are important particularly in newer technologies and are related to narrow channel and short channel of the transistors. Narrow channel effects, known as RINCE (Radiation-Induced Narrow Channel Effects), are more pronounced for NMOS transistors and are related to STI (Shallow Trench Isolation) oxide, that defines the channel width. The mechanism of charge trapping in the STI oxide is similar to the one for gate oxide, however, the STI is considerably thicker than the gate oxide and therefore, traps more charge. The impact of this phenomenon is noticeable mostly at the wide transistor edges but can affect the channel potential significantly when the width is decreased.

The second effect mentioned above is more dangerous for PMOS devices. It is related to the existence of an LDD (Local Drain Diffusion), used for the reduction of the electrical field in the channel and protect from the hot carrier injection, improving yield and reliability. The LDDs are spacers at the gate edges that

contain thin oxide, resulting in low-doped p- region at the edges of high-doped p+ source and drain areas. Trapping positive charge in these thin oxides leads to change in the LDD internal potential and, as a result, reduction of the local doping in the p- area. This phenomenon causes an increase of the LDD spacers resistance, that for short channels can dominate the channel conductivity [43]. In the case of NMOS transistors, stronger n- LDD implants can be no more effective leading to increased hot carrier injection [44].

To summarize, the long-term radiation-related effects on MOS transistors performance are:

- threshold voltage shift,
- transconductance reduction (change of carriers' mobility in the channel),
- increase of the leakage current,
- increase in noise,
- reduction of the breakdown voltage,
- degradation of the parameters matching,
- functional failure.

A second group of radiation-induced damage (Figure 15) are Single Event Effects (SEE), that, in contrary to TID, are short-term effects, and occur in silicon, instead of oxide. These phenomena are more relevant to digital circuits, where transistors operate as switches and usually affect only a small part of the device. The SEEs, caused by high LET (Linear Energy Transfer) particles, are stochastic processes and, therefore, a rate of occurrence is used as a measure. The number of electron-hole pairs generated is the highest when the hit of a high-energy particle is located on either of the MOS junctions (drain or source) [6]. The charges generated by a particle affect the NMOS and PMOS transistors differently. In NMOS transistors, the capture of electrons by junction implant leads to a current from the source/drain into the substrate (bulk), whereas in PMOS transistors this effect is reversed – p+ doped junctions capture holes, which results in current from the substrate (N-well) towards the drain/source. For the CMOS inverter this leads to a conclusion, that for the output equal to logic 0, transient currents originating from the PMOS transistor can cause 0 to 1 transition, whereas those from the NMOS device result in 1 to 0 transition [6]. As a result of transient currents, the following soft (non-destructive) and hard (destructive) errors can occur [6], [38], [13]:

Soft errors:

- **SEU** – Single Event Upset; a change of a device, circuit or system state caused by an energetic particle; usually happens in digital circuits like memories, latches and flip-flops; affect the performance of finite state machines (FSM), dynamic read access memory (DRAM) or static read access memories (SRAM);
- **SET** - Single Event Transient; is caused by transient voltages or currents originating from the currents generated by a charged particle; in analog circuits may temporarily disturb the

operation of the circuit and cause an excess noise with extremely high amplitude; affects also the biasing point of the circuit (can lead to slowing down the circuit operation, because of required recovery time); in digital circuits generates a temporarily wrong digital value;

- **MBU** – Multiple Bit Upset; more than a single upset at one time in a device, circuit or system; can happen in various ways: 1. Particle crosses the sensitive volume of several devices (particle hit is parallel to the device surface), 2. Particle hits the surface of the circuit perpendicularly and deposits a large amount of energy, and the amount of the charge is shared among different devices, 3. Two or more different particles upset two adjacent nodes at the same moment defined as a single clock cycle in a digital circuit [19];
- **SEFI** – Single Event Function Interrupt; is an upset of a device, circuit or system (for example Field Programmable Gate Array, FPGA), may cause malfunction of control logic or corrupt a data path; the device or system can be recovered by an external reset.

Hard errors:

- **SEL** – Single Event Latch-up; phenomenon associated with parasitic bipolar transistors (PNP or NPN) in the CMOS devices, that forms a thyristor structure, which is activated by high-LET particle and leads to a large current flowing through a low-impedance path, may lead to overheating and device breakdown, the only way to stop this process is switching off the power supply;
- **SES** – Single Event Snapback; similar to SEL, but does not require the presence of parasitic bipolar structures, the high current induced by a single-event particle, causing avalanche multiplication of charge carriers, present in NMOS transistors, bipolar junction transistors (BJT) and heterojunction bipolar transistors (HBT);
- **SEB** – Single Event Burnout; dangerous for high-power MOS transistors, especially if they are in disabled mode (large voltage drop across source-drain); can also occur in parasitic BJT, leads to excessive junction heating and device burnout;
- **SEGR** – Single Event Gate Rupture; can occur in a parasitic BJT or a power MOS device, rupture of gate dielectric caused by a high electric field, that leads to increase in oxide leakage current and growing temperature, that can locally destroy the oxide;
- **SHE** – Single Event Hard Error; highly energetic particle deposits locally in the gate oxide of a MOS transistor a high dose, that causes a threshold voltage shift too large to use the transistor; in memory circuits that causes a state change or so-called „stuck bits".

1.5.2. Radiation-tolerant Integrated Circuit's design

In the design of a radiation-hardened circuit, simulation of radiation effects prove helpful. In some complex systems, however, like memories, readout electronics (especially sensitive first analog stage) or low-jitter clock reference circuits, is more complicated. Making an electronic circuit immune to radiation

and mitigating the radiation-induced effects on the system performance, can be achieved on various levels and by various techniques. The possible approaches to the radiation-hardening are presented in Figure 18.

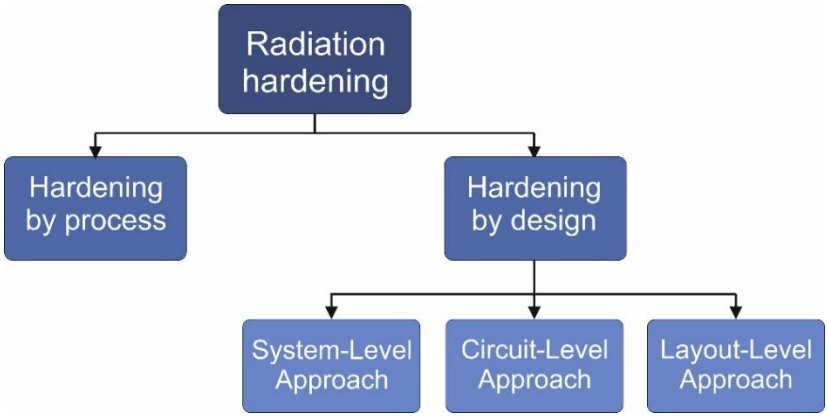


Figure 18 Radiation hardening of electronics on various levels.

1. **Radiation hardening by process (RHBP)**
    - **Substrate hardening techniques:**
        - Silicon-on-Insulator (SOI) technologies – reducing transient induced current and charge collection areas [38], helps to mitigate SEUs, SETs, SELs, also proven to improve the performance scaling in general-purpose CMOS technologies [13];
        - Silicon-on-Sapphire (SOS) technologies – a hetero-epitaxial process where a thin layer of silicon is grown on an Al_2O_3 (sapphire) wafer, this technology is used mostly for space and military applications, sapphire as a perfect insulator prevents from spreading radiation-induced currents to surrounding circuit elements [13];
        - Silicon-on-Diamond (SOD) – thanks to excellent thermal properties, improves the SEL immunity (reducing the active device temperature as it serves as heat distributor) [13];
        - Silicon-on-Nothing (SON) – forming a silicon device layer without the substrate layer; the main advantage – no interaction of particles with a wafer substrate, so no charge carriers are generated [13].
    - **Oxide hardening techniques –** controlling the oxide quality is crucial for radiation hardening; among the most common techniques are fluorination of oxide (reducing the positive oxide charge density [13]), gate oxide thickness reduction (related to technology scaling, the threshold voltage due to the trapped charges is smaller for thinner oxides), LOCOS isolation hardening methods, like for example introducing a metal layer in the isolation to change the electrical potential below [13] (in older technologies) and STI hardening (reduction of parasitic devices effects, increasing of the latch-up immunity) [13].
    - **Techniques improving SEE tolerance:**

- Reduction of the substrate and the epitaxial layer thickness to reduce the charge collection volume (against SEL, SEU) [45],
- Substrate doping increase to reduce the charge collection (against SEL, SEU) [46],
- Minority carrier lifetime reduction - suppressing the parasitic bipolar behaviour (against SEL) [47],
- Increasing the minimum allowed distance between p and n diffusions [19].

2. Radiation hardness by design (RHBD)

Choosing a dedicated CMOS technology for radiation-hardened designs is not always possible, due to accessibility and costs. Additionally, the same technology node provided by different manufacturers and in different process versions may not provide identical radiation hardness, because it is not the most important parameter to be monitored by foundries. Moreover, the RHBP techniques are not included within the devices models for simulation purposes and the circuit or system performance cannot be properly simulated and verified against the radiation-immunity, which makes the design process more difficult and increases the risk of system failure. Another approach is employing Radiation Hardening-by-Design (RHBD) techniques on various levels (Figure 19) to ensure reliability and stability of system performance even under very high radiation level.

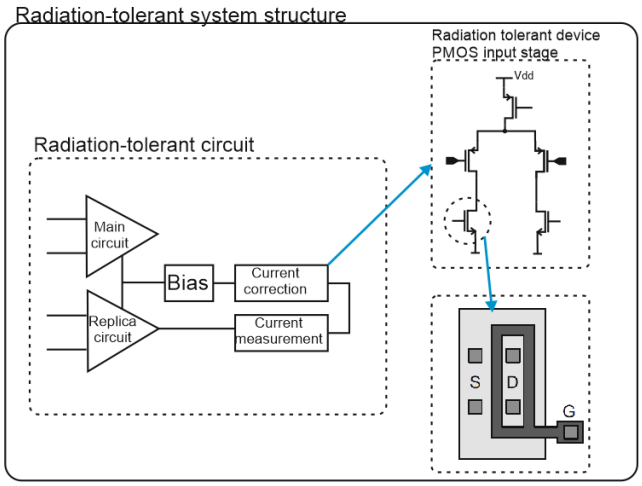


Figure 19 Radiation-hardening-by-design techniques on various levels [2].

Radiation-hardening on the top-level, or system-level, provides the most effective radiation-immunity improvement of the device, by identification of the most radiation-sensitive elements and selecting a proper architecture to implement the certain function (for example an analog-to-digital converter, ADC, or a phase-locked loop, PLL, elements architecture). In digital circuits, it is also the selection of the most effective way for errors handling (control or data path, memory errors) by providing, for example, system-level redundancy like Dual- or Triple Modular Redundancy, which means a multiplication of sensitive component and using a voter for errors detection or/and correction. The system-level radiation hardening-by-design includes also important decisions at the design phase, such as:

- selection of the operation mode - generally, synchronous operation is preferred over asynchronous, to mitigate effects from TID such as transition time variations and drifts in electrical parameters),
- selection of error correction techniques (ECTs (for example Hamming or Reed-Solomon codes, parity checking, rectangular codes),
- selection of the circuit speed and determination of the maximum speed that can be achieved without compromising the immunity to SETs (increased critical transistors width – higher load capacitances) [38].

The circuit-level approach is ensuring good radiation-tolerance of all susceptible system components and checking if the required performance can be met even under high radiation fields. This approach is associated with circuitry architecture selection. Several examples can be: the implementation of the charge pump and its bias for PLL, hardened bandgap reference circuit, employing redundant latches in the SRAM cells (or implementing it as Dual-Interlocked Cell, DICE [48]) or maximizing the number of transistors directly connected to supply or ground nodes in digital cells [38], [49].

Radiation-hardening on device-level bases on the selection of appropriate transistor type and geometry (width and length) for circuit implementation. It is believed, that PMOS transistors are generally more radiation-tolerant than NMOS ones, due to the fact, that the threshold voltage shift leads to performance alteration but not to functional failure. Also, the transistor width and length should be taken into consideration and chosen properly, to prevent from narrow channel and short channel effects [2].

The most detailed level of device hardening against radiation effects is the layout-level approach. It can be considered as the most important step in the device or system design in some cases, as any mistake in laying out the circuit may lead to significant problems caused by radiation. The leakage current caused by charge trapped in the STI in case of NMOS transistor can be reduced by drawing it as Enclosed Layout Transistor (ELT, see Figure 20) – closed gate shape separates the drain and the source regions [2], [6], [50].

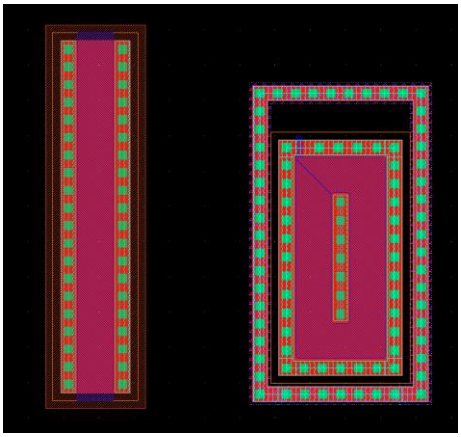


Figure 20 Comparison of single-finger, the straight NMOS transistor (left) and ELT NMOS transistor with guard ring (right) in 180 nm.

SEL immunity can be increased by minimization of the parasitic resistances associated with the PNPN bipolar structure by providing a large number of substrate contacts and placing both n-well and bulk contacts as close as possible to the n-well/p-substrate junctions, to reduce the resistive path. An example of this approach is shown in Figure 21.

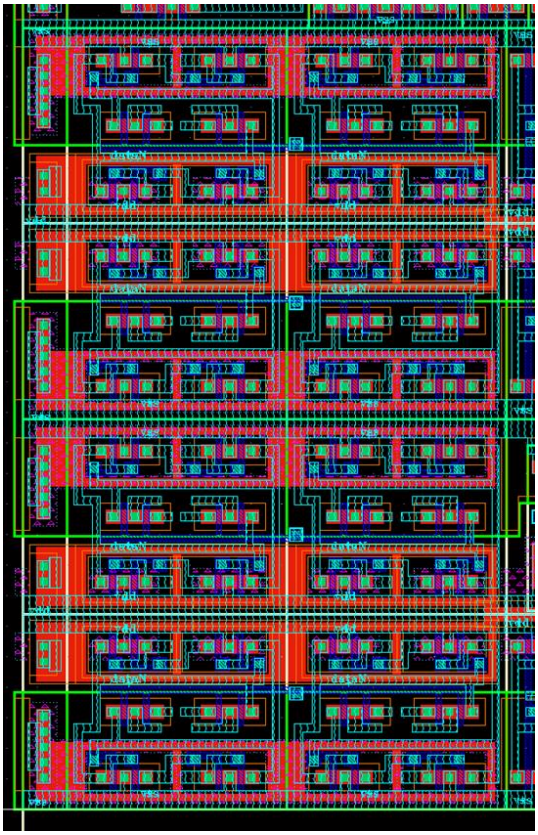


Figure 21 Placement of additional substrate/well contacts in an exemplary layout [51].

The SEU immunity of individual DICE memory cells can be improved if the number of contacts to guard rings is large enough and they are placed as close to the cells as possible [52], [49]. Other rules that can help to improve circuits' radiation-tolerance are for example:

- n+ regions on different potentials for series connection of NMOS devices must be separated by a p+ guard ring,
- for the series connection of two devices, placing them within one guard ring is possible only if the inner terminals are used (due to very high parasitic capacitance of the intermediate node),
- each device should be placed in its separate guard ring [52].

1.5.3. Sensors and interconnect modelling

The main building block of the STS detection station is a detector module, shown in Figure 22, comprising a sensor connected to the readout electronics on dedicated PCBs through a shielded application-specific cables bundle. Each sensor is a double-sided array of 1024 micro-strips on each side with 58 µm

pitch and a stereo angle of 7.5º [5], [28]. The detectors are AC-coupled to prevent from the leakage current flow through the readout electronics by a coupling capacitor formed from a metal strip deposited over a diffusion strip with an isolation layer between them. A single side of the detector is connected via tab-bonded ultra-light micro cables to 8 readout chips (two cables for one ASIC) assembled using wire-bonding on a dedicated front-end board (FEB) [53]–[55]. Signals are transferred between the sensor and the front-end (FE) electronics through the cables, that contain also two additional traces for each sensor side to be used for high voltage sensor biasing [56]. The application-specific custom micro-cables contain 128 thin (15 µm thickness) aluminium trace line each with 116 µm pitch and 35 µm width placed on two polyimide signal layers [52]–[59]. The cross-talk reduction and inter-layer capacitance are reduced by applying a polyimide foil insulating meshed spacer between the cable layers in the bundle. The entire stack is built of four micro-cable layers and shielded additionally against an external interference coupling.

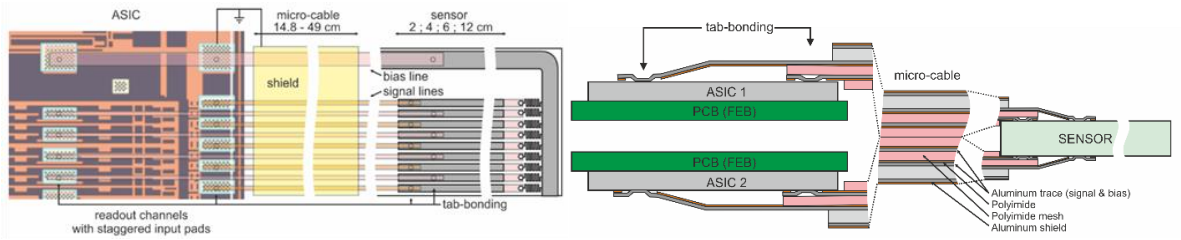


Figure 22 Detailed view of the detector – micro-cable – ASIC assembly: a) top view of a single sensor side tab-bonded to two-layer micro-cable attached to the ASIC. Signal traces, biasing traces and shielding layer are visible. b) side view of the assembly showing two FEB modules with attached ASICs connected to both sides of the sensors [60].

Figure 23 shows a cross-section of the sensor and application-specific micro-cable with marked the most important of the parasitic capacitances and resistances used in the simulation model (Figure 24). In the CBM experiment, application of sensors from two different manufacturers was considered, so the parameters characteristic for both of them were used for the prepared models to evaluate differences in their performance in terms of parasitic components.

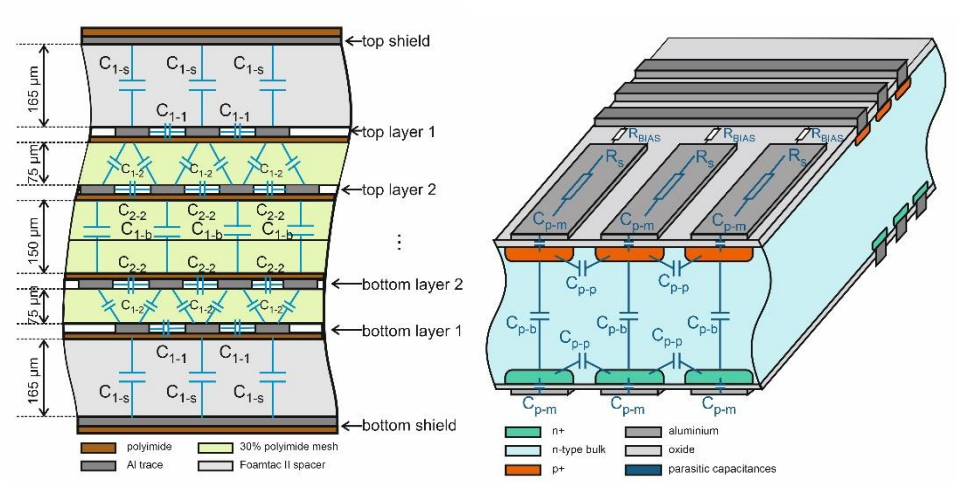


Figure 23 Cross-section and parasitic capacitances of a) ultra-light micro-cable assembly [21-22], b) double-sided detector.

The parameters of the application-specific micro-cable and double-sided sensor used for the SPICE models in the simulations and marked in Figure 23 Cross-section and parasitic capacitances of a) ultra-light micro-cable assembly [21-22], b) double-sided detector. as parasitic passive components are presented in Table 2 [58], [61], [62].

Table 2 Micro-cable and double-sided sensor parameters.

Sensor parameter	**Value**		**Cable parameter**	**Value**
	FAB1	**FAB2**		
strip to strip $C_{p\text{-}p}$ (p+)	0.36 pF/cm	0.43 pF/cm	trace material & dimensions	Al 35 µm × 14 µm
strip to strip $C_{p\text{-}p}$ (n+)	0.37 pF/cm	0.57 pF/cm	capacitance to same-layer neighbor $C_{2\text{-}2}$=$C_{1\text{-}1}$= $C_{S\text{-}S}$	0.119 pF/cm
strip to metal strip $C_{p\text{-}m}$	10 pF/cm	18 pF/cm	capacitance to a neighbour on adjacent layer $C_{1\text{-}2}$	0.139 pF/cm
strip to bulk $C_{p\text{-}b}$	0.18 pF/cm	0.21 pF/cm	to ground plane $C_{2\text{-}G}$	0.38 pF/cm
metal (Al) strip R_{sm}	10.5 Ω/cm	10.5 Ω/cm	to ground plane $C_{1\text{-}G}$	0.29 pF/cm
strip $R_{sp\ (p+)}$	66 kΩ/cm	66 kΩ/cm	trace series resistance R_s (signal)	0.635 Ω/cm
strip $R_{sp\ (n+)}$	44 kΩ/cm	44 kΩ/cm	trace series resistance R_s (bias)	0.618 Ω/cm
Bias resistance $R_{bias\ (p\text{-}side)}$	500 kΩ/strip	450 kΩ/strip		
Bias resistance $R_{bias\ (n\text{-}side)}$	500 kΩ/strip	1700 kΩ/strip		
Sensor thickness	285 µm	320 µm		
Total strip capacitance				
p-side	1.02 pF/cm	1.74 pF/cm	**Total cable capacitance**	0.382 pF/cm
n-side	1.02 pF/cm	1.52 pF/cm		

The electrical models of the double-sided sensor containing 5 strips per side (Figure 24 a)) and a micro-cable with separate sections for signal traces and bias traces (Figure 24 b)) were implemented using passive components (resistors and capacitors) with values based on Table 2. The designed models represent transverse as well longitudinal structure of the devices. The cable is a distributed model comprised of 10 sections. The models for the sensor and the cable as well include both sides to accurately reflect the conditions in the whole detector system.

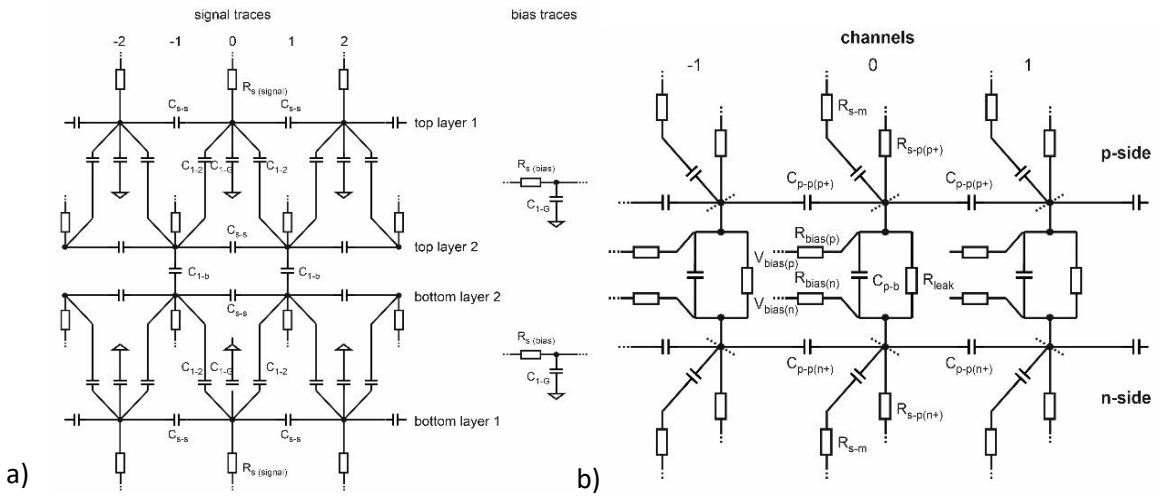


Figure 24 Models for simulation for a) application-specific cable, b) double-sided sensor.

The transfer function for different cable lengths (from 14.8 cm to 49 cm) was obtained in simulations and the acquired characteristics (output current to input current), are plotted in Figure 25 a). The cable was loaded with an ideal load (Z_{in} = 0 Ω). The simulated cable bandwidth ranges from 0.59 GHz to 6.6 GHz for the longest and shortest cable respectively. Figure 25 b) shows transfer characteristics obtained for both sides (p and n) of the sensors of the same length (6 cm) provided by two different vendors. Looking at these characteristics and parameters summarized in Table 2 it can be concluded, that the lower cutoff frequency of the cable transfer function is affected by the bias resistor – the higher the resistance the wider the bandwidth. Small differences in higher frequencies may be attributed to some strip-to-strip capacitance differences between p and n side, that for FAB2 sensor are up to 31%, whereas for FAB1 this difference is less than 3%.

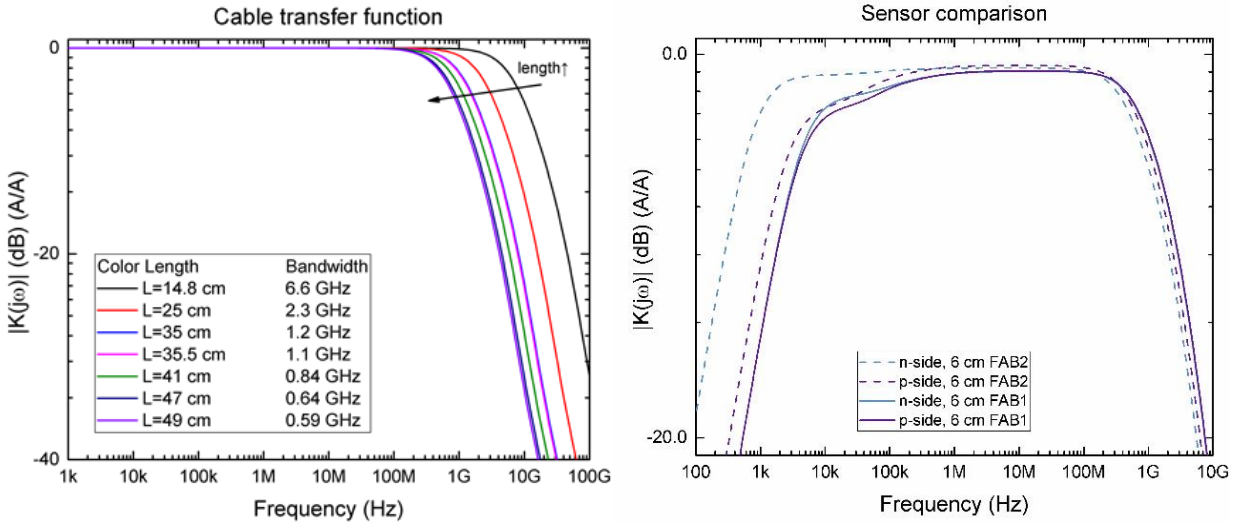


Figure 25 Transfer function comparison: a) cables of different lengths; b) sensors from two manufacturers, equal lengths.

1.5.4. Leakage current issues

A common problem in detector readout systems is leakage current originating from various system elements, that can cause parameters degradation, performance deterioration or even instability. Among the most severe issues caused by leakage current are for example a baseline shift at charge sensitive amplifier stage, system saturation or increased noise. Addressing these problems is particularly important in HEP experiments, where high energies of incoming charges can lead to a dramatical increase in the overall leakage value.

Leakage current in detection systems is unavoidable and has many sources, like for example sensor itself or external components, such as long cables [56], PCB fan-out and package (if applied) or ESD protection circuits (integrated into the readout circuit or external), that can dominate in certain conditions [63]. ESD protection circuit is commonly employed for the protection of the sensitive electronics against static discharge during the assembly process and for systems working with gaseous (GEM) sensors to improve immunity to sparks (however, in this case, additional, external protection is usually necessary [64]).

The sensors fabricated for the Silicon Tracking System in the CBM experiment by two different vendors (see previous section, 1.5.3) were characterized for the leakage current as well. The sensors used in the experiment are 290-330 μm thick, double-sided, AC-coupled with lengths of 2, 4, 6, or 12 cms, each contains 1024 microstrips. The total capacitance of the sensor connected by application-specific micro-cable ranges from 15 pF to 50 pF [65]–[67]. For example, at 400 V biasing voltage, total measured leakage of the newly fabricated sensors at 20 °C is around 1.3 nA/cm (8 nA/strip for the sensor of 6 cm length) [68]. This value is, however, dependent on the junction geometry, sensor architecture (vendor) and related to temperature (doubles approximately at every 8 °C increase [33]). In the STS detection station, the sensors will operate at a temperature around -5°C [69], [70]. After irradiation, the leakage can rise due to the radiation-induced silicon bulk damages [71]. For the CBM experiment, the limit value for all sensors independent on their length and distance from the beam is set to 400 nA/strip and after exceeding this value, a device is declared as dead (thermal runaway) [13]–[15], [72]. The sensor leakage current flow into the readout electronics is usually blocked by an integrated AC-coupling capacitor (low leakage, below 0.1 nA [73], however, it can be a source of additional leakage if the dielectric got damaged e.g. due to the pinholes appearing after irradiation (leakage growth up to 100 nA [74]).

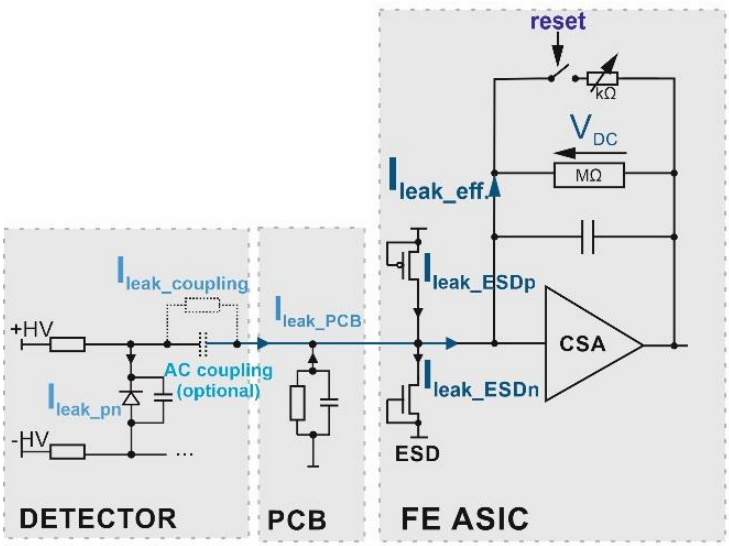


Figure 26 Simplified schematic of the considered front-end input stage with leakage current sources.

The presence of leakage current becomes a serious problem in the charge processing chains (Figure 26), that includes a CSA equipped with resistive feedback (also known as continuous reset, see Chapter 1.4), which is a large resistance (in the range of tens to hundreds of MΩ) for CSA stability and low noise contribution. However, the larger the CSA feedback time constant, the lower the input hit rate that can be achieved and the higher the risk of pulses pile-up. This effect leads to a significant operating point shift or even to saturation of the CSA core amplifier [33]. A solution to prevent from pile-up and provide faster baseline recovery and input pulses processing speed is a digitally-assisted pulsed reset of the CSA, which can be realized by a MOS switch. The principle is a bypass to the high-resistance continuous discharge of the CSA feedback capacitor by a small resistance to recover the baseline right after full processing of the input charge, to keep a low noise performance and good processing stage linearity.

A large resistance in the charge amplifier in conjunction with even a small leakage current flowing in the feedback path causes a DC level shift between CSA input and output (for example for leakage of 1 nA and feedback resistance equal to 20 MΩ, the DC level shift is equal to $\Delta V = I_{leak} \cdot R_{fb}$ = 20 mV). If the feedback resistor is realized using a MOS transistor working in the linear region, a DC level shift affects its gate-source voltage and therefore changes the effective resistance. As long as the change is not significant and has a negligible effect on the CSA transfer function, both phenomena are not visible in the whole system output, because the first stage of the charge processing chain is usually followed by an AC-coupled semi-Gaussian or similar shaping amplifiers. The problems may appear if the readout chain employs a fast reset, which in conjunction with leakage and a large resistance in the slow discharge path, may cause malfunction of the whole system. This phenomenon is depicted in Figure 27 by example waveforms of a channel working normally and two cases of channel performance in the presence of positive and negative leakage. As can be seen, the baseline shift can be different for the same amount of current but different polarities and varies during two phases of charge processing. In this example, for a feedback resistance set to around 13 MΩ, 2 nA of negative leakage results in 24 mV baseline shift and -52 mV for

positive, that can be seen as an equivalent of 2.4 fC and 5.2 fC input charge. A much smaller resistance of the reset switch (usually hundreds of kΩ) cancels the baseline shift and makes the CSA output potential equal to the input. The output voltage drifts back to the previous altered baseline slowly until the capacitor completely discharges.

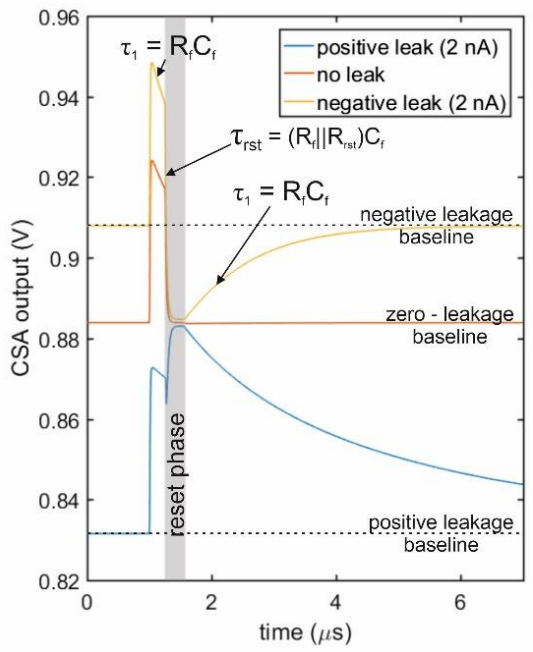


Figure 27 Simulated results showing the behaviour at the CSA output with the pulsed reset active.

The described problem was observed in measurements of a prototype ASIC incorporating a CSA with resistive feedback (slow discharge path) and a digitally-assisted fast reset. The measurement results are plotted in Figure 28. During a ~300 ns long reset phase, the CSA output voltage level is brought to the original baseline (equal to the level without presence of the leakage). The reset switch resistance is approximately in the range of 100 kΩ, so the effective baseline shift is around several mV and can be neglected. The fast edge visible at the beginning of the reset phase does not cause any problems in case of no leakage in the feedback path. The severity of problems caused by the leakage current depends not only on the direction and quantity of the baseline alteration (referenced to the original one) but also on the charge being processed by the readout channel. The effect on the CSA output waveform is shown in Figure 28 a) and on the shaper can be seen in Figure 28 b). Depending on the fast edge polarity at the application of fast reset, the pulse seen at the shaper output may be of the same polarity as the pulses caused by the incoming charges (and being processed by the channel). As a result, fake hits are registered by the readout electronics or, what worse, if the fast reset is triggered by the logic basing on the slow shaper output signal, a multiple afterpulse generation is likely to occur. After the reset phase, the first stage amplifier is still not back at the shifted baseline (through a long time constant), introducing an undesired baseline shift at the CSA output (accumulated). It can be concluded, that charge processing manner can be severely affected by the presence of leakage current flowing in the first stage feedback path.

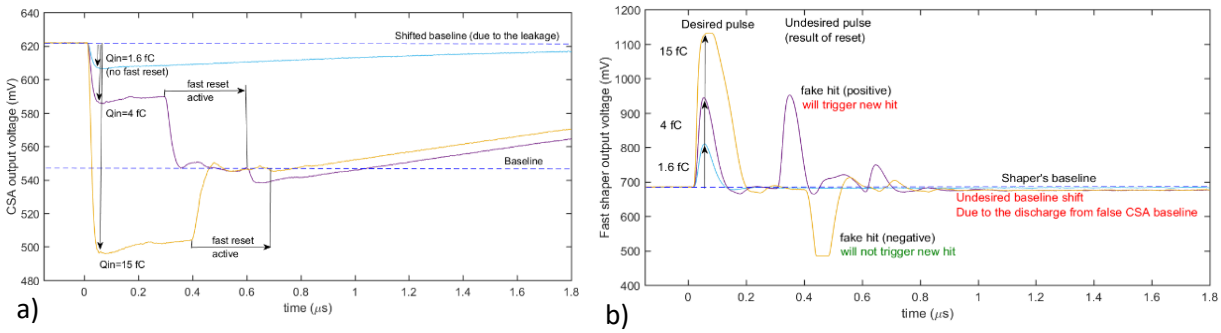


Figure 28 Measurements of the effect in the prototype ASIC: a) charge sensitive amplifier output, b) fast shaper output [75].

1.5.5. Noise in the readout system

A detector readout system suffers from the noise stemming from various system components. The noise level of such system should be optimized to allow energy measurements with required precision and resolution as the signals from radiation sensors are very often weak and cannot be properly registered in a noisy environment (low signal-to-noise ratio, SNR). The noise analysis of the whole system with all noise contributions is necessary for the readout electronics optimization – each noise type should be identified and represented as an equivalent current or voltage noise source connected to a charge sensitive amplifier (CSA) input, as shown in Figure 29. For the noise calculations, it is important to include also the total input capacitance (detector, CSA input transistor and some parasitic capacitances).

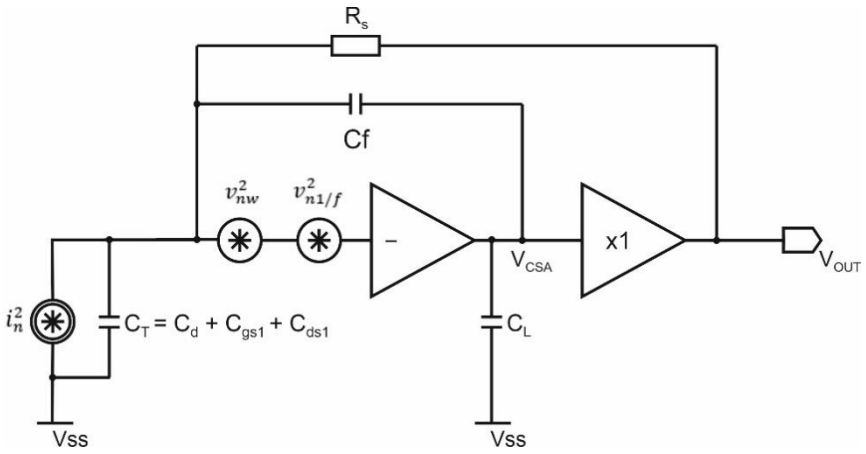


Figure 29 The input stage with current and voltage noise sources and total input capacitance [33]

The noise contributions can be divided into internal - intrinsic to the readout circuitry, especially its first stage, and external ones - stemming from a sensor, sensor biasing network, interconnect, or printed circuit board. In each group three types of noise can be distinguished: parallel current noise, voltage series noise (white) and flicker (also known as 1/f) noise (pink). The main contributions in each of these groups for an exemplary detector readout system are presented in Figure 30 and shortly explained below.

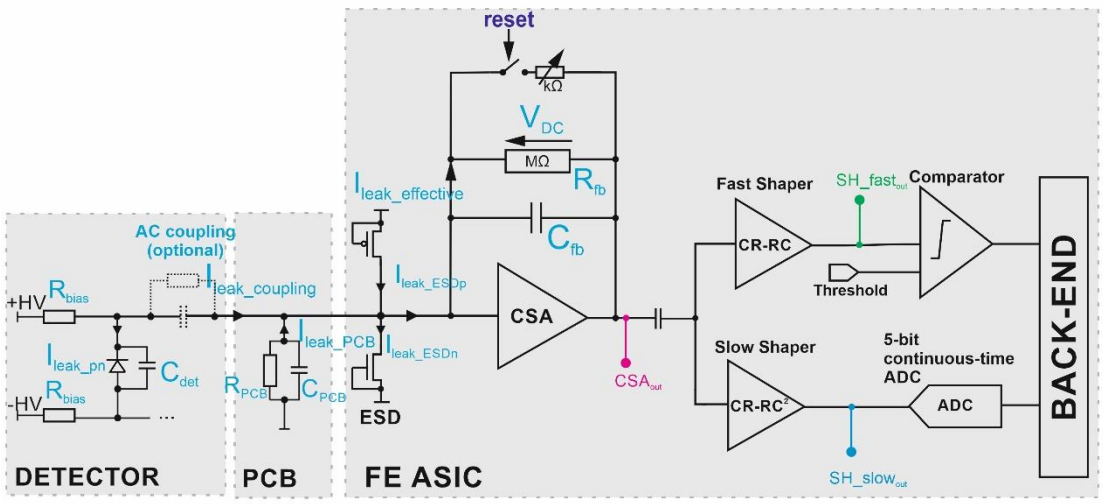


Figure 30 Exemplary detection system architecture – intrinsic and extrinsic noise sources.

The main system components contributing to:

1. parallel current noise:

- detector leakage current shot noise (I_L) - external,
- resistor bias shunt resistance R_{bias} - external,
- leakage current flowing through transistors in the Electrostatic Discharge (ESD) protection circuit - internal,
- current thermal noise from feedback resistance – internal,

2. series white noise:

- input transistor thermal noise - internal,
- input transistor gate resistance thermal noise – internal,
- interconnect on-chip resistance thermal noise – internal,
- various series resistors (sensor's metal strip, cable) thermal noise - external,

3. series 1/f (or flicker) noise:

- CSA input transistor flicker (1/f) noise.

In the first group, the main contribution is detector leakage current (I_{det}, shot noise) and its spectral density can be expressed as:

$$i_n^2 = 2qI_{det} \tag{5}$$

The same equation (5) is used to describe the contribution from the leakage current of the transistors in an Electrostatic Discharge (ESD) Protection circuit (I_{ESDn}, I_{ESDp}), applied very often to protect the channel from the ESD events (especially in applications with gaseous detectors [64]). Other sources of parallel current noise include feedback resistance current thermal noise (related to the CSA input), current flowing

in the feedback path [25], [33], sensor bias shunt resistance [20], leakage current from the damaged coupling capacitor (in AC-coupled detection systems, due to pinholes [74]) and thermal current noise of PCB traces resistance – see Equation (6).

$$i_n^2 = \frac{4k_BT}{R_{bias}} + \frac{4k_BT}{R_{fb}} + \frac{4k_BT}{R_{PCB}} + 2qI_{det} + 2qI_{ESDn} + 2qI_{ESDp} \quad (6)$$

The voltage noise sources main contribution is CSA input transistor thermal noise (current noise produced by the transistor resistive channel seen at the amplifier input as a series voltage source) expressed by the Equation (7) :

$$v_{nw}^2 = 4k_BT\alpha_w\gamma\frac{1}{g_m} \quad (7)$$

The gate of the input transistor has some resistance (denoted as R_G) which produces thermal noise seen as voltage noise source at the CSA, with a spectral density equal to:

$$v_{nw}^2 = 4k_BTR_G \quad (8)$$

The Eq. (8) expresses also noise spectral density of internal interconnect resistance (R_{inter}, metal paths from pad to the channel input) and various off-chip resistances like metal strip resistance within the sensor (R_{Al}, for AC-coupled detectors), the cable resistance (approximated with $R_w/3$, where R_w is total cable resistance) – Equation (9):

$$v_{nw}^2 = 4k_BTR_{Al} + \frac{4}{3}k_BTR_{cable} + 4k_BTR_{inter} + 4k_BTR_G + 4k_BT\alpha_w\gamma\frac{1}{g_m} \quad (9)$$

Where gm is the transconductance and γ is the inversion coefficient (ranges from 1/2 in the weak inversion to 2/3 in the strong inversion) of the input transistor:

$$g_m = \frac{I_{DS}}{n\varphi_T}f(i_f), f(i_f) = \frac{1}{\sqrt{i_f+0.5\sqrt{i_f}+1}}, \gamma = \frac{1}{2} + \frac{1}{6}\frac{i_f}{i_f+1} \quad (10)$$

, φ_T – thermal voltage, i_f - normalized forward current dependent on the drain current, device aspect ratio, mobility, subthreshold slope voltage and the thermal voltage [76].

The series flicker noise (1/f noise) is introduced by the CSA input transistor and usually contributes significantly to the total noise level (limiting for example performance of high-resolution detection systems). The presence of this kind of noise is explained by two mechanisms: mobility fluctuation (Hoodge model) or charge number fluctuation (McWorther model) [33]. The flicker noise spectral density can be expressed in simplified form:

$$v_{nf}^2 = \frac{k_f}{C_{ox}WLf} \quad (11)$$

The series flicker noise (1/f noise) is introduced by the CSA input transistor and usually contributes significantly to the total noise level (limiting for example performance of high-resolution detection systems). The presence of this kind of noise is explained by two mechanisms: mobility fluctuation (Hoodge

model) or charge number fluctuation (McWorther model) [33]. The flicker noise spectral density can be expressed in simplified form:

$$ENC^2 = ENC_i^2 + ENC_w^2 + ENC_{\frac{1}{f}}^2 \quad (12)$$

$$ENC^2 = \frac{1}{\tau_p} \cdot v_n^2 \cdot A_w \cdot C_T^2 + A_f \cdot v_{nf}^2 \cdot C_T^2 + \tau_p \cdot A_i \cdot i_n^2 \quad (13)$$

$$ENC^2 = A_w \frac{1}{\tau_p} C_T^2 4k_B T\left(\frac{\gamma}{g_m} + R_{Al} + \frac{1}{3}R_{cable} + R_{inter} + R_G\right) + A_f K_f C_T^2 + A_i \tau_p \left[2q\left(I_{det} + I_{fb}\right) + \frac{4k_B T}{R_{bias}} + \frac{4k_B T}{R_{fb}}\right] \quad (14)$$

From the above equation ((13) and (14)) it can be concluded that the white series noise contribution to the total ENC is proportional to the total input capacitance and inversely proportional to the square root of the shaper peaking time. The parallel noise contribution does not depend on the input capacitance and is directly proportional to the square-root of the filter peaking time. The flicker noise component in the total ENC is proportional to the total input capacitance and independent of the peaking time.

The divagations concerning noise contributions of the readout electronics presented above were focused on the CSA input transistor. This is a simplified approach because all transistors of the CSA core amplifier introduce noise (Figure 31). Those having the most significant impact on the total output noise level will be shortly described below.

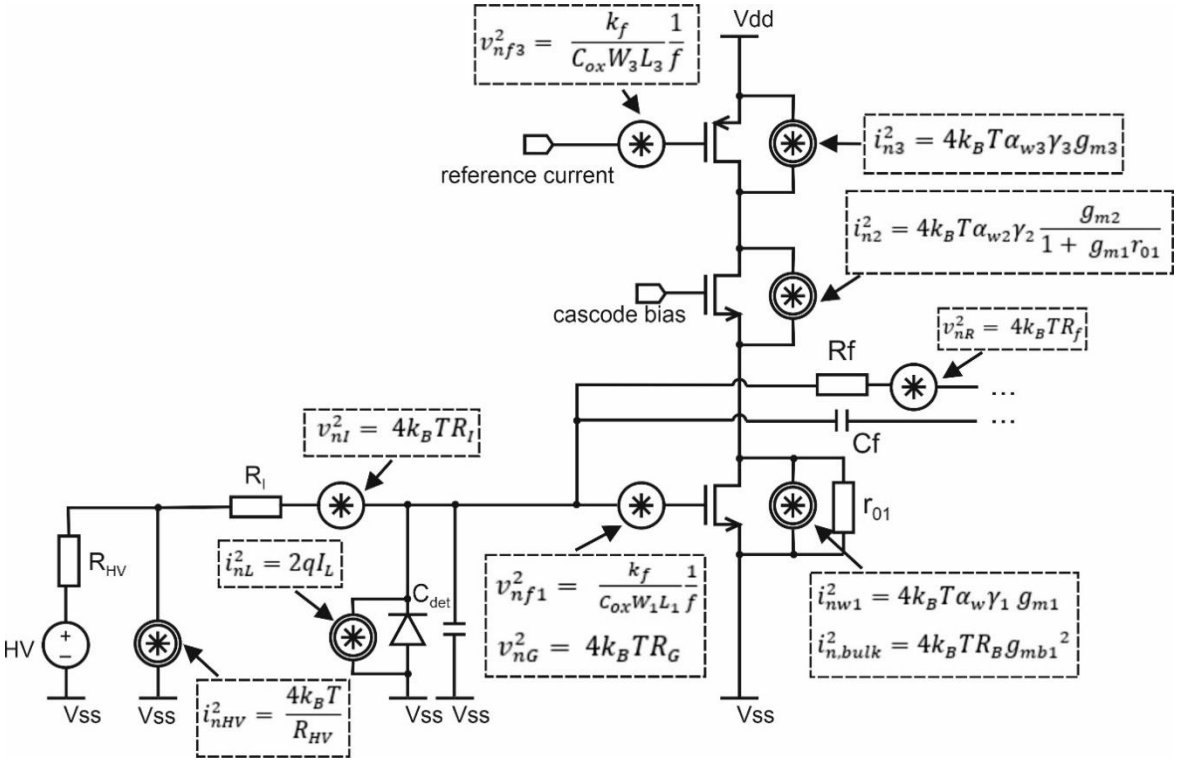


Figure 31 Detailed schematic of the input stage amplifier noise sources.

Thermal fluctuations in the bulk potential coupling to the channel through the bulk transconductance g_{mb1} introduce a drain current noise with spectral density $i^2_{n,\,bulk}$, that is visible at the CSA input as a voltage noise source with the value given by the following equation:

$$i_{n,bulk}^2 = 4k_BTR_B{g_{mb1}}^2 => v_{n,bulk}^2 = 4k_BTR_B\left(\frac{g_{mb1}}{g_{m1}}\right)^2 \quad (15)$$

The bulk transconductance is usually around 0.2-0.3 the gate transconductance, so this noise contribution is usually much smaller than the one induced by the channel and can be neglected [33], [77].

Quite significant noise is usually contributed by the reference current source. In older technologies (channel length L > 100 nm) it may be even impossible to lower this contribution below 10% of the total ENC [77]. This transistor (M_3) introduces current channel thermal noise (i^2_{n3}) and voltage flicker noise (v^2_{nf3}). To refer these noise sources to the CSA input, the first one needs to be divided by the input transistor transconductance g_{m1} squared, whereas the second one should be first changed into a current source by multiplying it by the source transistor transconductance squared and then divided by the g^2_{m1}.

$$i_{n3}^2 = 4k_BT\alpha_{w3}\gamma_3 g_{m3} => v_{n3}^2 = 4k_BT\alpha_{w3}\gamma_3\frac{g_{m3}}{{g_{m1}}^2} \quad (16)$$

$$v_{nf3}^2 = \frac{k_f}{C_{ox}W_3L_3}\frac{1}{f} => v_{nf3,in}^2 = \frac{k_f}{C_{ox}W_3L_3}\frac{1}{f}\left(\frac{g_{m3}}{g_{m1}}\right)^2 \quad (17)$$

The noise contribution from the cascode transistor M_2 is thermal current noise (i^2_{n2}). The cascode transistor can be treated as a source degenerated single-stage topology and its equivalent transconductance is inserted into the current noise spectral density calculation:

$$i_{n2}^2 = 4k_BT\alpha_{w2}\gamma_2\frac{g_{m2}}{1+g_{m1}r_{01}} \quad (18)$$

The equivalent transconductance can be approximated by $1/r_{01}$, where r_{01} is the M_1 output resistance and is much smaller than the input transistor g_{m1}. Its impact on the total noise level can be therefore neglected [33].

To optimize the CSA noise performance, transistors size and biasing currents should be carefully selected to limit all other noise contributions mainly to the large input transistor flicker and thermal noise [33], [78]. The feedback resistor value should be chosen large enough not only for stability reasons but also to keep its contribution smaller than the one of the sensor leakage current [33]. This approach is a front-end designer's point of view which assumes designing a charge sensitive amplifier, that contributes less to the overall system noise, than the external components. This, however, is not a solution to obtain good noise performance at the system-level. During the prototype development phase, both internal and external noise sources should be taken into considerations and included in the simulations towards optimum filter design.

Having all noise sources represented at the CSA input as voltage and current noise sources, a total noise level at the output can be calculated. For the calculations, the amplifier transfer function should be evaluated, taking into consideration feedback resistance and capacitance, total input capacitance, load capacitance and resistance and the input transistor transconductance. The amplifier transfer function is usually second-order (with two poles which should be real and distantly spaced) [33].

- τ_{fb} – CSA feedback capacitor discharge time constant (falling time),
- τ_r - rising time, related to the CSA bandwidth (for example ~40 ns for the CSA GBW ~9 GHz).

As the CSA feedback resistance value is usually big to ensure stable operation and low noise contribution, it can be assumed that the rising time constant is much smaller than the feedback time constant, and therefore that the CSA bandwidth has no strong impact on the ENC. However, checking if the relation between τ_r and τ_{fb} holds, should be taken into account during the design phase as well. To calculate the total noise at the CSA output, the impact of every element should be calculated including amplifier transfer function (the main equations are summarized in Table 3) and then, the total ENC is a square root of the sum of all ENC^2 values.

Table 3 Equivalent Noise Charge referred to the CSA output.

Source	ENC² @ CSA output
R_{bias}	$\frac{k_B T R_{bias} \tau_{fb}}{q^2}$
I_{det}	$\frac{I_L \tau_{fb}}{2q}$
I_{ESDn},I_{ESDp}	$\frac{I_{ESDn}\tau_{fb}}{2q}, \frac{I_{ESDp}\tau_{fb}}{2q}$
I_{FB}	$\frac{I_{FB}\tau_{fb}}{2q}$
R_{FB}	$\frac{k_B T R_{fb}}{q^2}$
R_{Al}	$k_B T R_{Al} \frac{g_{m1} C_T}{C_{fb} C_L}$
R_{cable}	$k_B T R_{cable} \frac{g_{m1} C_T}{C_{fb} C_L}$
$R_{inter.}$	$k_B T R_{inter.} \frac{g_{m1} C_T}{C_{fb} C_L}$
$M_{CSA_{in},th}$	$k_B T \frac{C_T}{C_{fb} C_L}$
$M_{CSA_{in},1/f}$	$\frac{C_T}{q} \frac{K_F}{C_{ox} W_1 L_1} \ln(\tau_{fb} \frac{g_{m1} C_{fb}}{C_T C_L})$

1.5.6. Power supply interference

Complex tracking detection stations comprise often a large number (up to tens of thousands) of multichannel integrated circuits working simultaneously. Uniformity of the parameters of all charge processing channels is very important in such systems and it can be ensured by providing a stable, uniform power delivery network (PDN) for whole detector station. Ensuring low noise operation of the readout ASICs require not only careful optimization of the noise level on the schematic and post-layout levels in terms of CSA core design, matching of the sensor capacitance and adjusting the feedback resistance to the expected sensor leakage shot noise. The performance of low-noise chip measured in the laboratory environment can be severely deteriorated in the whole system due to complicated biasing conditions and interferences coupling, as well as noisy power supply delivering devices (Low Drop-Out Regulators,

LDOs). The study on the PDN require system-level co-design between ASIC development and other system components, taking into account the specific operating conditions, power density on modules (number of chips supplied from a single source), cooling capabilities (power dissipation limitations and power efficiency), construction, distance from the beam etc. to make sure that the targeted detection system performance meets the tight requirements to enable achieving the experiment aim.

The power supply induced interference is particularly harmful to single-ended charge processing channels, that are the most common architecture in the detector readout systems due to the tight area and electronics intrinsic noise requirements. These structures are also very sensitive to internal cross-talk – switching noise coupling through the bulk of the transistors connected to the ground potential. The well-optimized low-noise performance of the system can be compromised by high-frequency noise from DC-DC converters used in the PDN. A standard approach to mitigate these effects is to separate ground and supply rails to provide multiple power domains, each of them supplied with an individual low-noise source.

Another approach is to filter out the power supply network noise using LC or RC filters for decoupling. The first method is, not applicable in tracking detectors, where ferrite-based inductors cannot be employed due to high magnetic field flux [56]. Application of large resistances for filtering is also limited in such applications because of the wide, distributed PDN and a varying amount of load current depending on the ASIC configuration resulting in variable I·R drop that, due to multiple load points, cannot be properly compensated. As a consequence, noise should be minimized at the LDO level by employing a low-noise device with good PSRR [56].

The LDO regulators used in high-energy physics experiments detectors readout are very often exposed to high total irradiation doses (TID) – up to several MRad (Si) in the system lifecycle [56]. For the CBM experiment, some off-the-shelf solutions for the PDN construction were tested on the beam in terms of TID and single-event effects (SEE) immunity, but none of them survived irradiation with GeV range protons [79]. Taking into account these results, as well as high output current and low area requirements, the linear regulators for such experiments should be custom-designed, with particular attention paid to low-noise performance and high PSRR. Meeting all of these requirements is not always possible and sometimes more emphasis is placed on radiation-immunity and good power efficiency than on the noise lowering capabilities, which challenges the development of the readout electronics.

1.5.7. The complexity of the system – long experiments lifetime

Detection stations in the, for example, HEP experiments, are very often massive, complex systems, comprising a large number of readout channels working simultaneously. In the CBM experiment, an STS detector will comprise more than 14 000 ASICs, each of them containing 128 channels, which yields almost 1.8 mln channels. The chips will be placed on 1752 front-end boards (FEB), readout by 600 readout boards (ROB) and the data from the event-driven electronics will be processed by almost 80 Data Processing Boards (DPB) [80]. Every component of such a compound system needs to meet tight Quality Assurance

(QA) requirements and should be thoroughly tested not only in the laboratory before the system assembly. The wafer-level, chip-on-board, and inter-assembly tests should be performed, as well as inter-assembly characterization and monitoring of the performance during the experiment lifetime. The entire detector station will be exposed to total irradiation doses of several MRad (2-3 MRad (Si)) for this particular experiment) during the lifetime [5]. Due to common effects induced by radiation in the sensors, readout electronics and other system components (like for example parts of the PDN), that are likely to occur (see Section 1.5.1), the whole system performance should be monitored and faults need to be detected. In the ICs channels calibration, it is possible to discover faults and indicate malfunctioning channels, however, this does not provide information about the root cause of the performance degradation. Another possibility is measuring the biasing voltages and power supply level inside each chip of the entire system and finding out any drift in the chip configuration due to radiation effects. In such a large system disassembly and measurements of every ASIC step-by-step is a very time-consuming approach, not possible to be applied in the real experiment. Routing all of these internal potentials outside the chip is also not possible and it would require a huge number of pads and the IC area would increase significantly. The power supply circuits located close to the readout ASICs on the FEB should also be monitored during the system operation [56] for effective diagnostics of the detection station performance.

1.5.8. Data transmission requirements

In the self-triggered readout systems for HEP experiments, all particle hits are being recorded. The selection of the important events is done by main data acquisition systems and this causes a huge amount of data generated during the experiment like signal amplitude (particle energy), timestamp, readout electronics diagnostic data. This data should be sent to the DAQ system in a very short time posing demanding requirements on the data transceiver. In the HEP experiments, readout electronics is very often placed in the close vicinity of the beam so its mass is required to be low which means a limited number of transmission channels (and the number of copper wires). Due to this fact, the data transmission rate over a single link should be increased and the channels need to be multiplexed. It is also important to minimize the size of the readout electronics and integration of the transceiver and serializer inside the chip, to reduce the number of the readout module components. As a result of these requirements, the exploration of newer sub micrometer technology nodes (below 90 nm) is promising. Employing these technologies enables speeding up the circuits operation and data transmission, minimization of the integrated circuits area and, therefore, a higher density of transistors placement in the selected area. Another advantage is thinning of the transistors gate oxide, that makes them more immune to radiation damages related to the dose accumulation (TID effects) and eliminates the necessity of using large transistors in the ELT geometry. More modern technologies allow for operation with lower nominal power supply, and it is, therefore, possible to significantly reduce the power dissipation, which is a very important aspect in large readout systems, that include a huge number of devices working simultaneously in a single detection station and require advanced cooling infrastructure [81].

Data transmission circuits (CML transceivers, LVDS standard) with all necessary circuitry like frequency synthesis circuits (Delay Locked Loop, DLL and Phase-Locked Loop, PLL) applied in the High-Energy Physics Experiments have been commonly designed using older, stable and verified in terms of radiation immunity technologies (like for example 0.35 μm, 0.18 μm and 0.13 μm) [82], [83]. Nowadays, many authors have been working on employing newer technologies for the application within radiation fields and evaluation of their behaviour after irradiation [84], [85] but mostly focused on technologies like 130 nm FD-SOI, 90nm or 65 nm bulk, only very initial research has been made towards the performance evaluation of the 28 nm bulk technology [42]. The works have been focused on speeding up the transceivers operation and data transmission, devices minimization, higher integration level, reduction of the transmission lines (particularly important in complex systems comprising a large number of readout ASICs). Additionally, it is important to maintain immunity to radiation effects of both analog and digital circuitry. Data transmission is particularly susceptible to Single Event Effects affecting the operation of digital circuits. In the serializer, when the operation speed of the circuits is high, especially if the Phase Locked Loop is employed, the appearance of the SEE on any of the circuit sensitive nodes leads to error propagation, losing sync in the communication and long-term consequences for the data integrity. Also, the control path of the read-out system should be protected from radiation-induced errors and implementation of diagnostic features is very important. Many Radiation-Hardening-by-Design techniques can be applied, including redundancy (for example Triple Modular Redundancy, TMR for the control path), errors detection and correction techniques (for example parity check in the data path), isolation of the critical nodes to prevent from change of for example memory cell. Many of the recent works were focused on the evaluation of the radiation effects in the PLL circuits as well as on the techniques improving their radiation immunity and the comprehensive overview is presented in [6].

1.6. Radiation immune digital interfaces

1.6.1. Phase-Locked Loop - architecture and radiation-related issues

Frequency synthesizers, such as a Phase-Locked Loop (PLL) shown schematically in Figure 32, are very important parts of data transceiver (transmitter/receiver) circuits. They are used to provide clocks both in the transmitter and the receiver circuitry [86]. The general principle of a frequency synthesizer operation is to generate an output frequency signal or signals (often multi-phase) from a stable input reference clock source. The PLL circuits employed in the transceivers for radiation measurements and imaging should be immune to radiation-related effects and keep their performance on an acceptable level during the whole system lifetime. Among the parameters that should be met by a frequency synthesizer for a particular application, the most important are: phase-noise performance, discrete spurious noise performance (preferably no parasitic frequency components in the output spectrum), operation/switching speed, frequency bandwidth and tuning range, maximum power consumption, area and possibility to integrate with the target transceiver in the read-out chip [86].

A PLL circuit is a negative feedback loop comprising a Voltage Controlled Oscillator (VCO), a Phase Detector (PD), or, more commonly, a Phase/Frequency Detector (PFD), a Charge Pump (CP), a loop filter (LF) and a divider (DIV, Figure 32). The operation principle is that the VCO output signal is divided by DIV and its phase is compared to a reference clock by the PFD (or PD). In case of any discrepancies in the frequency or phase, the VCO frequency is adjusted to match the phase of the reference clock and decrease the phase difference to zero [6]. The control signals are filtered by the loop filter to guarantee the stability, expected frequency behaviour and appropriate attenuation of the phase noise components. Phase lock between the feedback and reference clocks implies that the frequencies are also locked.

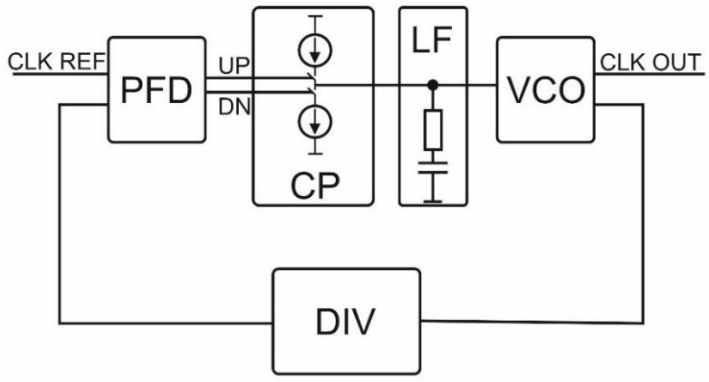


Figure 32 Phase-locked loop.

Phase-locked loops are versatile circuits that can be applied in multiple systems and devices for frequency synthesis, modulation and demodulation as well as in clock recovery and skew reduction (for example in data transceivers). The PLLs dedicated for operation in the harsh radiation environment are prone to radiation effects that cause parameters deterioration or even functional failure. Some of the relevant effects are discussed below. In the industrial applications, a common practice is a triplication of the whole PLL and voter, that decides, which output should be selected (is not affected by the radiation). This is, however, bulky, power and area greedy solution – other possibilities to compensate the radiation-induced effects are also shortly presented below.

Phase/Frequency Detector operation can be considered as a 4-state Finite State Machine (FSM), which output is a periodic signal, whose average value gives information about a frequency error if the frequencies are unequal (FD) or phase error (PD) for equal frequencies [87]. The occurrence of Single-Event Upset in the PFD might result in an incorrect switch of the FSM state and thus, a cycle slip in the PLL [6]. A self-correcting TMR method works well to mitigate this effect [88]. As it requires triplication of the PFD circuit and application of a majority voter, that makes the circuitry more complex thus introducing additional delays. This, however, does not degrade the speed performance in this case, as the PFD typically works at low frequencies (up to few hundreds of MHz). Employing a cross-coupled reset in the PFD allows for automatic state correction and recovery of the PLL operation without cycle slips [6].

The TMR technique can be also combined with some layout-level RHDB techniques as proper spacing of each of the three PFD cells [6].

Works of various authors indicate that the parts of a PLL that are most sensitive to the radiation damage, especially SEEs, are the charge pump, the voltage-controlled oscillator and the frequency divider [89], [90], [91].

The charge-pump circuit that is used to source or sink current depending on its input, in the simplest form is a set of two current sources and two switches, controlled by the UP and DOWN signals generated by the PFD. The charge-pump current value influences the loop dynamics, i.e. its bandwidth and damping factor. The proper up and down currents' balance minimizes the reference spurs and the static-phase offset [87]. The charge-pump is sensitive to both TID and SEE [92]. TID-related effects change the threshold voltage and current conduction of the current sources in the circuit, thus affecting the dynamics of the loop. The most important phenomena that are caused by the total dose are related to degraded matching of the charge-pump currents, increased overdrive voltage of the transistors (that enter the triode region sooner) and reduced output voltage swing [6]. These effects can be minimized by proper selection of the size of the transistors (large W and L) and providing a proper design margin. However, the more difficult part of the CP design is related to the switches (controlled by the up and down signals) due to conflicting requirements concerning small voltage drop, TID- immunity (large devices) and minimization of the charge injection (small devices). In this case usage of the ELT devices is necessary [6]. The charge-pump is the most susceptible to SEE part of the PLL and any variations on its output node connected directly to LF have a direct effect on the VCO control voltage [93]. SEE induced errors concern mainly the biasing circuit that generates bias voltage for the NMOS and PMOS current sources in the charge-pump. Depending on the architecture of the biasing circuit and which bias voltage was affected by the SEE, the loop gain can be affected temporarily leading to temporal degradation of the loop stability or one of the currents can change increasing the mismatch. This effect can be mitigated by the decoupling of the bias nodes [6]. Another issue is charge injection to the charge-pump output node connected to the loop filter capacitor caused by the SEE. The voltage shift caused by this phenomenon depends on the capacitance – the larger the capacitor value the less the voltage is shifted and thus, the less significant is the phase deviation [6]. This, however, leads to higher area occupied by the design.

An SEU in the divider-by-N logic can affect any of the bits and cause the phase deviation that depends on which bit was upset and on the current counter state [6]. The simplest approach to protect the logic in the DIV is the application of redundancy in the circuit, for example, TMR. Making all cells in the counter radiation-hardened has several drawbacks, like for example 3 to 4 times increased power consumption and area occupancy (triplicated cells and additionally, a voter employed), and slowed down design and reduction of the maximum frequency of the PLL. One possible solution may be an implementation of a prescaler, that means making the first flip-flop cell in the counter not radiation-

hardened, as the upset on this bit is not that severe and the speed of operation plays the significant role. The TID-related issues can become significant when the PLL runs at very high frequencies and the design uses small devices (for example in the standard library cells). To minimize this effect, ELT-based standard cells can be employed (if the timing restrictions are not very tight), but at the cost of increased power consumption and area due to geometric rules and the ELT devices minimum size [6].

The effects of the radiation on the VCO depend on the oscillator architecture: the LC-tank oscillators are generally more radiation-immune than the ring oscillators as the oscillation frequency depends on the inductor geometry and the oxide capacitance, the parameters, that do not change with the total accumulated dose (only a change in the loop gain may be observed, due to the transistors transconductance decrease) [6]. In the ring oscillators, the oscillation frequency is related to the biasing current which may vary due to the accumulated dose. In some cases, ELT devices should be employed, which limits the maximum oscillation frequency that can be achieved because of their larger size and therefore increased capacitive load. The SEE can affect three parts of the VCO: biasing circuits, tuning circuit and the core of the oscillator. If the biasing current circuit is affected, the frequency of the oscillator changes – this effect can be minimized by proper decoupling. SEE on the tuning circuit, which is usually based on a current mirror, causes an instantaneous frequency shift. In this case mitigation by using capacitive decoupling is more difficult so that the bandwidth and the phase margin of the PLL are not affected. The SEE in the oscillator core results in phase steps (instead of frequency jumps as it is in the two remaining components). To minimize this phenomenon, larger node capacitance and more oscillator power can be considered but always at the cost of reduced maximum VCO frequency. Some radiation-hardened VCO examples include an embedded VCO in voltage-mode feedback to mitigate the SET strike at the control voltage node [94], employing a “Maneatis” load providing more symmetrical resistance around the switching point [95]. SEE sensitivity of the VCO can be increased by using more stages in the ring-oscillator for a constant power consumption [6].

1.6.2.Phase-Locked Loop – circuits for HEP/Space applications overview

In recent years there has been growing interest in the development of fast digital interfaces for data transfer dedicated for radiation-imaging and physics experiments, as well as space applications. In these applications, usually older, mature and stable technologies (with transistor length larger than 100 nm) have been widely used. Radiation-hardened by process technologies develop slower than the commercial ones and thus the designers cannot fully exploit the benefits and disadvantages of the technology scaling [19]. However, there are some new rad-hard by Process technologies being developed, for example, 90 nm SkyWater high-reliability process [96]. Recent works have been focused on the investigation into a possibility to employ more modern technologies in the high-energy physics (HEP), to benefit from less power, smaller circuits area and higher speed while maintaining the circuits radiation-immunity for example for the Large Hadron Collider (LHC) at CERN [42], [97]. Generally, newer technology nodes, thanks to thinner transistors oxide and less charge trapping, are believed to be more immune to TID effects. Smaller

transistors dimensions and no need to employ ELT devices allow reducing the circuits area, which is especially important for better data transmission circuits integration with the sensors read-out electronics. Smaller transistors enable achieving faster operation, faster data transfer over a single link, higher data throughput and a possibility to reduce the number of links. Since the application of some RHBD techniques (for example TMR) in older technologies results in significant degradation of the circuit speed, it is promising to employ faster technology nodes to provide the same or higher operation speed, while ensuring the proper handling of the SEEs.

Table 4 summarizes some of the recent works presenting various approaches to radiation-hardening-by-design a PLL circuit. A number of studies found that the most vulnerable part of a PLL circuit is the charge-pump [6], [93]. Some techniques to partially mitigate the effect of SET currents in the CP were proposed in [93], that employ charge sharing between up and down switches (current compensation technique combined with a differential charge cancellation layout method). Authors in [91], [93] suggested a radiation-hardened current-based CP (C-CP) architecture in 130 nm technology node, to overcome some limitations of the voltage-based CP (V-CP), that is generally believed to provide better SET-immunity [98] at the cost of increased reference spurs and phase noise. The VCO architecture in [93] bases on the differential cascade-voltage switch logic (DCVSL) delay cell, that provides higher SET immunity thanks to data storage on two different nodes instead of one in conventional static logic gates. The architecture of every single flip-flop in the frequency divider is based on a true single-phase clock (TSPC), which is a type of a dynamic (edge-triggered) D flip-flop, and is combined with dual-rail logic and dual interlocked storage cell (DICE) architecture. Additionally, Muller C-elements are implemented at each flip-flop output for the perseverance of the data [93]. The measurements results presented in [93] and in more details in [91] show very good immunity to both TID and SEE induced issues - the TID-related jitter degradation was improved by almost 15 times (reduced to around 2% at 100 krad for the presented design comparing to for example a self-biased PLL), whereas the maximum SEE-related RMS jitter degradation was reduced by 2 orders of magnitude comparing to an unhardened PLL. Also the number of lock losses caused by a SEE was eliminated completely, whereas the average value for an unhardened design was around 30 during the test period [93].

The authors in [99] propose an RHBD phase-locked loop designed in 65 nm to reach higher output frequencies (up to 3.2 GHz). In this work, a comparison between an LC and a low-noise ring-oscillator in terms of sensitivity to TID and SEU was performed. The radiation-immunity of other structures in this design was also improved. For example, the divider is split into two parts: a prescaler providing division by 4 implemented in Current Mode Logic (CML) and a divide-by-16 circuit based on a standard logic with TMR. In terms of TID-immunity, the LC oscillator designed in this work maintained its performance up to 600 Mrad with only 5% oscillation frequency variation, whereas the ring oscillator output frequency was significantly affected – up to 30% change at 300 Mrad dose. Tests for the SEU showed a larger cross-section for the LC-oscillator than for the ring oscillator [99].

The work by S. Capra et. al. [100] presents a new approach to the design of a PLL for HEP experiment's purpose using the 28 nm technology node. The PLL is based on a digitally controlled oscillator (DCO) to benefit more from the chosen technology. The designed ring-oscillator provides an output frequency ranging from 2 to 3.2 GHz and is fully digitally controlled. Post-layout simulations showed that the designed DCO meets the requirements of the higher level FPGA-based system. As far as the author is concerned, no measurements of the presented solution have been published yet, so the verification of the 28 nm utility in the data transmission systems for HEP experiments and other radiation environments needs to be performed.

Another interesting example of a design of a Phase-Locked Loop circuit for physics experiments is presented in [101]. This circuit was implemented in 65 nm technology and is based on an LC voltage-controlled oscillator that achieves output frequencies between 4.8 and 6 GHz. The most interesting thing in the presented design is its moderate power consumption (18 mW) and compact area (0.124 mm^2), which does not compromise the period jitter performance (< 4 ps rms). This makes it a competitive solution to PLLs based on a ring-oscillator for integration in the read-out ASICs – see Table 4. Similarly, as in [99], the divider-by-32 is split into a CML prescaler (divide-by-4) and D-flip-flop (DFF)-based CMOS divide-by-8 circuit implementing the TMR correction (using three DFFs and three majority voters). This approach was proven to provide good SEU protection of the critical blocks [82]. The circuit was characterized against TID effects using 10 keV X-rays to accumulate a dose of 2.5 MGy and shown only a moderate degradation in jitter performance without any functional degradation.

The design presented in [89] includes an alternative approach to radiation-hardening of the frequency divider, that occupies less area and consumes less power than the standard TMR technique. Another advantage of the proposed solution is its improved immunity to SEU on both combinational and sequential logic circuits. The PLL circuit proposed in [89] contains also a radiation-hardened: VCO, CP and a lock-detector (RH-LD). The role of the RH-LD is the detection of the phase displacement that results from a SEE on any sensitive PLL node. The reduction of the recovering time after a radiation-related issue, the authors designed the loop to have relatively high bandwidth. Additionally, the most important loop parameters (for example charge pump current or the division ratio) are made programmable. To provide low susceptibility to the SEEs, the VCO gain is kept relatively low (1 GHz/V). The measurement results proved a good immunity to both TID and SEE issues of the designed PLL circuit. The presented design can withstand over 300 krad(Si) total ionizing dose with the jitter degradation of only 7.42% and also shows an immunity to single-event effects up to 83.7 $MeV \cdot cm^2/mg$ (which is more than two times better comparing to an unhardened PLL design, that can survive less than 37.6 $MeV \cdot cm^2/mg$).

Table 4 Comparison of RHBD PLLs design.

	2016 [91]**,** [93]	**2017** [99]	**2018** [100]	**2018** [101]	**2020** [89]
Technology node	130nm PD-SOI	65 nm	28 nm	65 nm	130 nm PD-SOI
Supply voltage	1.2 V	1.2 V	1.0 V	1.2 V	1.2 V
Radiation hardening - SEE	SEE lock threshold 37.6 MeV·cm2/mg	significantly higher sensitivity to SEUs on the LC oscillator compared to the ring oscillator PLL (heavy ions with LETs between 3.2 and 69.2 MeV.cm2/mg)	N/A	TMR correction on the divider to provide some level of upset protection in the most critical block	immune to single-event effect (SEE) up to 83.7 MeV·cm2/mg
Radiation hardening - TID	jitter degradation after a total dose of 300 krad(Si) **7.55%**	from 300 Mrad of 5% to 10%, nearly 30% of the variation is observed after 600 Mrad /up to 600 Mrad - no variation in the free-running oscillation frequency of more than 5%.	N/A	fully functional after a total dose of **2.5 MGy**, with a moderate jitter increase.	can provide greater than 300 krad(Si) total ionizing dose assurance (jitter degradation **7.42%**), design fully functional after a total dose up to 2.5 MGy (moderate jitter increase)
Oscillator	VCO (RO)	RO/LC	DCO (RO)	LC	VCO (RO)
Output/target frequency	450~650 MHz	2.2 - 3.2 GHz	2 - 3.2 GHz	4.8 - 6 GHz	450~900 MHz
Power dissipation	8.6mW@ 500MHz	6 mW (oscillators only)	less than 10 mW	18 mW	14.3mW@ 900MHz
Phase noise	−107 dBc/Hz at 100 kHz	-91 dBc/Hz / -106 dBc/Hz @ 100 kHz	N/A	N/A	-107.80 dBc/Hz @ 100 kHz / -106.61 dBc/Hz @ 1 MHz
Jitter	Cycle-to-cycle: 7.3ps@ 500MHz	5.6 ps / 325 fs (rms jitter)	N/A	<4 ps rms (period jitter)	Cycle-to-cycle: 3.2ps@ 900MHz
Area	0.113 mm^2	N/A	0.00144 mm^2	0.124 mm^2	242 μm × 186 μm / 0.045 mm^2
Reference spur	−54 dB	N/A	N/A	N/A	-47.67 dB

1.7. Dissertation theses

1. Differential charge processing can be efficient in low-noise systems with the tight area and specific environmental constraints. Differential charge processing in the read-out electronics for detectors is rarely used due to higher power dissipation, larger area occupancy and intrinsically higher noise. However, this assumption is true only if the clean supply voltage can be provided. There are applications where the use of differential or pseudo-differential charge processing architectures may become beneficial. These applications include tracking detection stations where the power supply induced interference coupling is not negligible, cannot be externally filtered due to magnetic field and influences the electronics performance significantly. – The expected radiation dose and high magnetic field prevents the use of the commercial off-the-shelf low noise DC-DC converters/linear voltage regulators and ferrite-based inductors.
2. It is possible to improve the noise performance in the harsh and variable environment with varying and complex dominant noise sources contribution by in-depth analysis and simulation of the longitudinal and transverse architecture of the detector and connection to the read-out electronics and by employing configurability in the read-out electronics, especially in the shaping filters to adapt and a better match to the external conditions.
3. Stable operation of the Charge Sensitive Amplifier (CSA) with high feedback resistance while providing fast input charges processing in the presence of extensive leakage current of the unknown and variable amount and flowing direction, can be obtained by the combination of digitally-assisted fast reset with the leakage current compensation techniques.
4. Using newer technologies in the design of data transmitting circuitry is beneficial in terms of speeding up the operation and data transmission which is required in the complex read-out systems generating a huge amount of data but also can decrease the sensitivity of the circuit to the radiation-related effects (Total Irradiation Dose) and enable employing acceptably effective Single Event Effects mitigation techniques without compromising the available area and possible operating speed.

Chapter 2 Analog circuits for the silicon strip detectors

2.1. Charge sensitive amplifier – noise optimization

The front-end electronics should be carefully designed and optimized particularly in terms of CSA input transistor noise, which is the main contributor. Although all devices forming the core amplifier and its feedback network contribute to the overall noise their impact is usually smaller compared to the large input transistor [33]. As can be concluded from equations (4) – (8) (Section 1.5.5), the channel thermal noise (seen at the CSA input as a voltage noise source) can be minimized by maximizing the input transistor transconductance (g_{m1}), whereas the flicker noise is lowered by making this transistor big enough (large W and L). The input transistor transconductance can be increased by a high aspect ratio (W/L) and large biasing current. However, large input transistor contributes to the total input capacitance (C_T) and therefore increases the total noise level. Finding an optimum size of the input transistor depending on its operation region (strong, weak or moderate inversion [76]) is crucial in the noise optimization process of the readout electronics and is usually performed for a particular sensor capacitance. If the channel thermal noise is dominant, and the flicker noise can be neglected, the optimum width of the input transistor working in the strong inversion can be calculated using the formula [76] :

$$W = \frac{C_{det}+C_{fb}}{2C_{ox}L_{min}+6C_{ov}} \tag{19}$$

Where C_{det} – sensor capacitance, C_{fb} – feedback capacitance, C_{ox} – gate oxide capacitance, C_{ov} – overlap gate-diffusion capacitance per channel width.

If the input transistor works in the strong inversion, the gate capacitance versus detector capacitance is related by a common formula: $C_g = \frac{1}{3} C_d$ minimizing the thermal noise contribution. Taking into account the flicker noise, that can be even higher than the thermal one, the gate capacitance can be increased up to the value of the sensor ($C_g = C_d$) [33].

It was observed in the simulation results, that a minimum in the ENC curve is more visible for older technologies (like for example 0.35 μm) and for smaller sensor capacitance, whereas it is flatter around the minimum value for newer technologies and larger capacitances. That effect can be attributed to the lower current density (Ids/W) and operation in the moderate inversion region of the input transistor [76]. The equation (20) assumes that the optimum width of the CSA input transistor does not depend on its biasing current but this assumption is true only in the strong inversion. If the transistor works in the weak or moderate inversion, increasing its width leads mostly to higher noise because the transconductance is not increased anymore, while the input capacitance is large. The formula for the optimized W is different for the transistors operating in moderate inversion [76]:

$$W_{opt} = W_{SI} \frac{1}{1+A\cdot\left(\frac{W_{SI}}{i_{f,W}}\right)^{m}} \quad (20)$$

In the above equation, W_{SI} is the optimum width in the strong inversion, $i_{f,W}$ is inversion current times the transistor width, A and m are constants characteristic for particular technology [76].

The input transistor biasing current source related noise can be minimized by ensuring that its transconductance is smaller than the input transistor's one (see Eq. (13) in Section 1.5.5).

To minimize the contribution of the gate resistance (R_G) thermal noise, wide input CSA transistor can be split into more identical devices (fingers) connected in parallel by short-circuiting their both end-points with a metal strip (Figure 33). The noise generated by the bulk resistance (R_B) can be reduced by using enough substrate contacts [33].

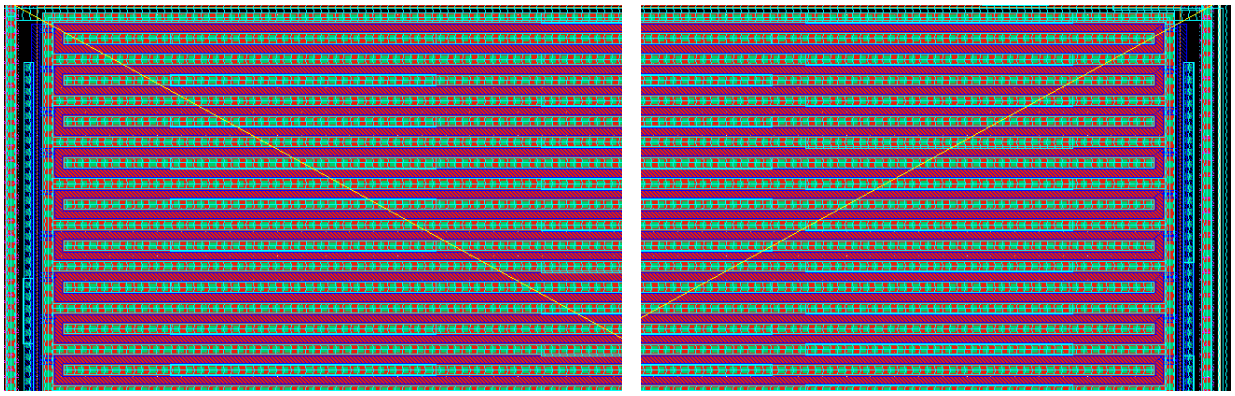


Figure 33 CSA input transistor layout with gate polysilicon connected on two sides to reduce the gate resistance.

The noise contribution of the readout electronics should be kept on such level so that it does not dominate the other, external noise sources. The feedback resistance (R_f) should be chosen large to introduce less noise than the sensor leakage current according to the equation [33]:

$$\frac{4k_BT}{R_f} = 2qI_L \rightarrow R_f = \frac{2k_BT}{qI_L} \approx \frac{50\ mV}{I_L} \quad (21)$$

In many applications, the leakage varies during the sensor lifetime, so the feedback resistance is usually configurable to compensate for these changes.

The examples of noise contributors with their typical values (e.g. for the CBM experiment) are summarized in Table 5.

Table 5 Noise contributors and typical values.

Source	Comment	Source	Comment
R_{bias}	typ. 500 kΩ - 1.7 MΩ	R_{Al}	typ. 10.5 Ω/cm
I_{det}	typ. 2 - 8 nA/cm	R_{cable}	typ. 0.635 Ω/cm
I_{ESDn},I_{ESDp}	typ. 1 - 10 nA	$R_{inter.}$	typ. 15 Ω
I_{FB}	typ. 2 - 5 nA	$M_{CSA_{in},th}$	γ between 1/2 and 2/3
R_{FB}	typ. 5 - 30 MΩ	$M_{CSA_{in},1/f}$	technology-dependent

Using the values from Table 5 to calculate the equivalent noise charge and dividing by the total value for current and voltage noise sources separately, the percentage of contributions can be calculated. It allows for identification of the dominating noise source for each of these groups (Figure 34) and system-level-oriented noise performance optimization.

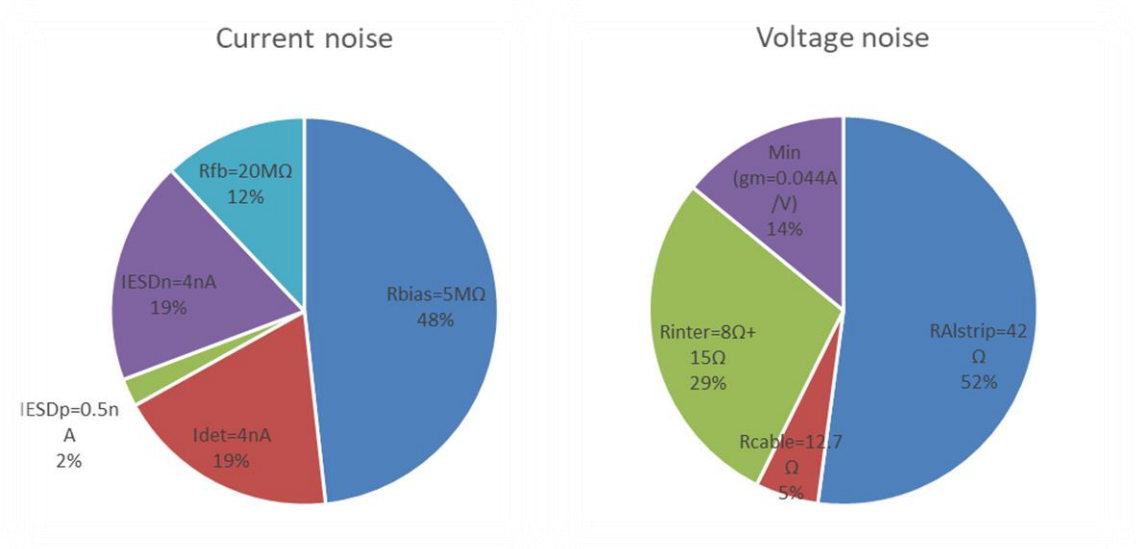


Figure 34 Pie charts for current and voltage noise contributors

As can be concluded from the pie charts presented above, in the exemplary readout system, the noise contribution from the electronics itself is low compared to other system elements. Although the front-end may be well optimized and provide very low ENC value in the simulations and measurements in the laboratory, the whole system noise can increase significantly due to extrinsic components, that should be taken into account from the very first phase of the design. The possible decisions for the noise optimization at the system-level both for the readout electronics and the sensor and its biasing network are summarized in Table 6.

Table 6 Noise optimization possibilities.

Readout electronics	**Sensor & biasing network**
Maximize **transconductance** and **area** of the input transistor (large W/L)	Minimize sensor capacitance (not always applicable) + cable (length)
Minimize **input transistor capacitance** (minimize capacitance at input) – should be optimized and matched with detector capacitance	Minimize detector leakage current (irradiation!)
Maximize **feedback resistance** of the CSA	Minimize Al strip resistance
Minimize R_{inter} (~50%)	Maximize R_{bias} (>5 MΩ)
Optimum **peaking time** (depending on various noise components contribution and FE maximum rate capability)	
Shaping amplifier (filter) **architecture and order**	
Input transistor reference **decoupling** or/and **filtration**	

2.2. CSA feedback and leakage current compensation

In the readout systems, a known problem is leakage current originating from various system components. The exact value of the leakage determination is difficult and it can be unexpectedly high (exceeding the simulated values resulting from models provided by the foundry). In this work, it was found out that for the technology used, the simulated leakage values are underestimated compared to the measured ones. The value and polarity of the leakage may tend to change during the readout circuit operation. The leakage can stem also from an additional, external or on-chip ESD protection used in, for example, readout systems for the gaseous (GEM) detectors to protect from sparks.

The leakage current, especially when a fast reset of the Charge Sensitive Amplifier is used, can severely deteriorate the overall parameters or may even lead to incorrect performance (Chapter 1.5.4). If the operating conditions like voltage and temperature are constant and known, the sizes of the MOS transistors, used as diodes, in the ESD protection circuit can be selected so that the current from the upper diode is sunk and fully compensated by the lower one. In some experiments, like for example the CBM experiment, one chip is dedicated for operation in two different detection stations and the difference between temperatures in these two systems is large (e.g. -20ºC and +85ºC), limiting the possibility to ensure balanced MOS-based diodes leakage. Additionally, the radiation damage during the chip lifetime may change the originally balanced circuit and increase the resulting current. The more universal solution is providing a way to compensate for the leakage current of both polarities while ensuring high CSA feedback resistance and the possibility to apply a pulsed reset.

As a first step, to get some insight into the leakage quantities relevant for selected technology (180 nm), an ESD protection test structure (Figure 35) was implemented in a prototype integrated circuit for measurements and comparison with simulated parameters. The circuit comprises regular threshold voltage PMOS and NMOS transistors with aspect W/L = 264 μm/0.28 μm and W/L = 216 μm/0.28 μm respectively, which widths are approximately 30% smaller than typical ESD protection circuit according to the technology vendor recommendations to minimize the capacitance. The circuit is supplied with 1.2 V power supply, lower than nominal 1.8 V for this technology. 1.2V node is normally shared with the supply of the CSA input MOS transistor branch and is separated from other nodes to reduce interference coupling. The internal node of this structure is connected to a pad for connection of external, precise source-measure unit (SMU). In this work, a Keithley 2400 SMU was used to provide the bias voltage and measure the current (see Figure 35), which in the real application would flow into (or from, depending on the polarity) an input stage of the front-end.

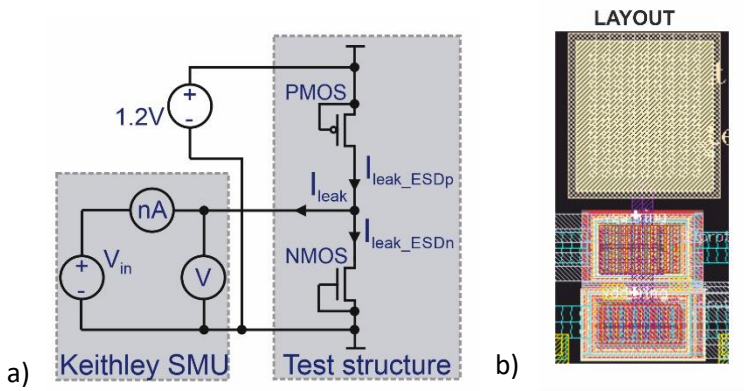


Figure 35 Measurement of the test structure leakage current: a) test setup schematic and b) layout of the test structure.

Figure 36 a) shows the leakage current versus temperature acquired in simulations for two power supply voltages (1.2 V and 1.8 V). The leakage current exceeds 1 nA for temperatures above around 55 °C. Even this amount of current will affect the performance of the circuit (especially the fast reset feature), but as measurements showed (Figure 36 b)), this value is underestimated.

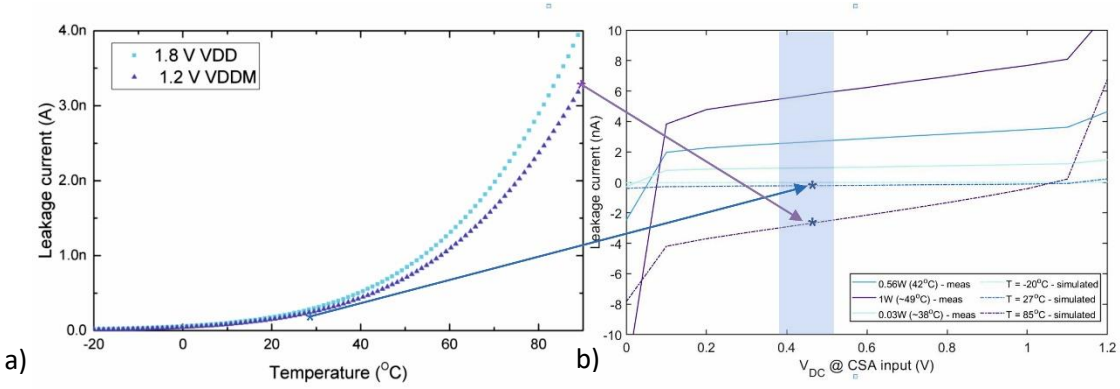


Figure 36 Leakage current of the ESD protection circuit; a) simulated versus temperature; b) measured and simulated versus applied voltage and power dissipation/temperature.

The comparison between measured and simulated leakage values and for several temperatures and across various potentials at the input node, presented in Figure 36 a) and b) respectively, shows that the discrepancies between model and real-world devices are significant and suggests that the models used for the simulations may not be accurate. In the target application (in the readout ASIC [30]), the input node is kept on around 0.4 V (the application range marked with a blue field in Figure 36). At this potential, the measured leakage current achieves a value of 6 nA at ~50°C, which for this kind of readout circuit is not a negligible amount. As can be concluded from the plot above, the polarity of the leakage is also variable and difficult to predict. According to the previous study on the UMC 180 nm process, the leakage from the ESD protection diodes may increase by even a factor of 100 after irradiation to 2.5 MRad (TID) [71], which may result in complete degradation of the front-end electronics fast performance.

A solution, usually employed in the pixel detectors readout [107], [108], is a compensation circuit forming a low-frequency feedback loop in the CSA stage, which was originally proposed by F. Krummenacher [109]. Its operation principle is an assumption, that for a selected polarity, the current

can flow into a current source (transistor M_{3_n} of the Krumm_p part in Figure 37) instead of the CSA large feedback resistor, and does not cause the voltage drop between amplifier input and output. The slow feedback path, formed by transistor M_2, M_{3_n} and a capacitor C_{Krumm} (in the Krumm_p part, see Figure 37) equivalent model is a high value inductance (defined as $2 \cdot C_{Krumm}/(g_{m1} \cdot g_{m3})$), that compensates the voltage offset by sinking the leakage current. The Krummenacher-type feedback works as an equivalent resistance with a value defined by $R_{fb} = 2/g_{m,in}$ (if $g_{m1} = g_{m2} = g_{m,in}$) [110]. The value of the effective feedback resistor in this case is controllable by the circuit biasing current (I_{Krumm}) – the lower the current, the higher the effective resistance value.

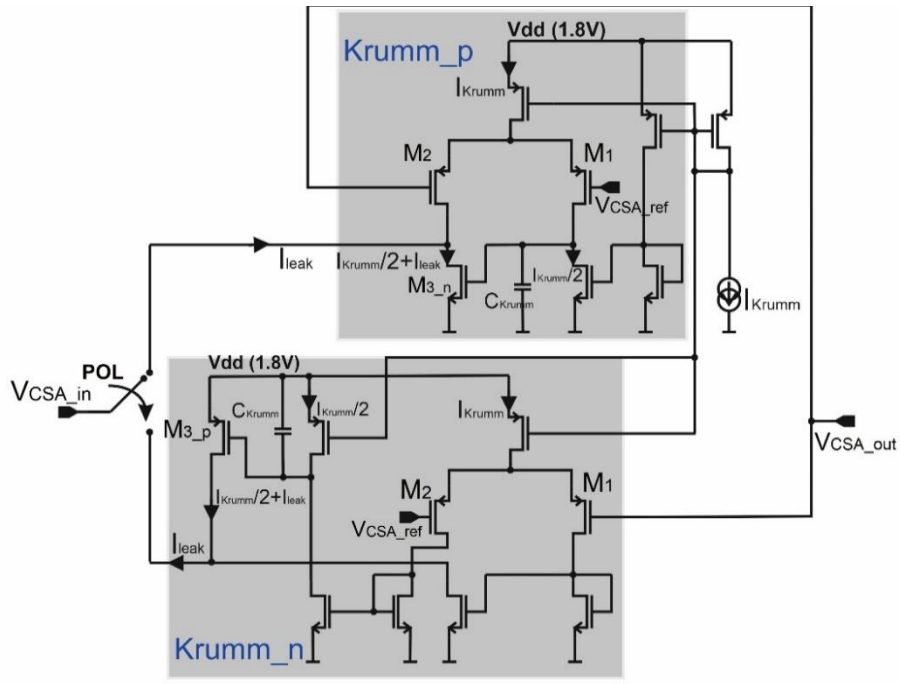


Figure 37 The Krummenacher feedback for both leakage current polarities schematic [111].

In applications, that ensure known and determined leakage current polarity, typically PMOS differential pair and NMOS current source for currents flowing into the CSA input node are employed, and a complementary configuration for the opposite current direction. The range of current that can be compensated by a topology selected for particular polarity is much larger than the anticipated value of the leakage (according to the measurements ±40 nA leakage leads to the resistance change around 15% and the DC voltage shift is only ± 3mV). The compensation abilities of the opposite current are equal to half of the reference current ($I_{Krumm}/2$), as shown in Figure 38. If the leakage of opposite polarity exceeds the half of the circuit bias current, the sinking transistor (M_{3_n} or M_{3_p}) are eventually cut off to ensure equal currents in the transistors of the input pair, causing an offset at the CSA output growing with the leakage (ΔV) [33]. As a remedy, increasing the bias current helps to compensate relatively large currents of both polarities, but as a trade-off, results in higher input pair transconductance and therefore, lower effective feedback resistance.

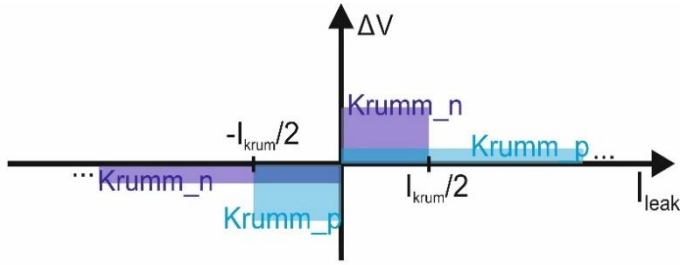


Figure 38 The amount of current of both polarities compensated by the Krummenacher feedback.

High effective feedback resistance value independent on the amount and polarity of the leakage current present in the system can be achieved employing a double, switchable, Krummenacher feedback circuit (Figure 37), that allows for stable operation and compensation of even large currents varying due to temperature change or radiation-induced effects [111]. This solution comprises of two complementary feedback paths operating independently for particular selected leakage current polarity. The Krumm_p part of the circuitry is dedicated to compensating current flowing into the CSA input node by employing an NMOS current source (M_{3_n}) and the Krumm_n part is suited for current sunk from the input by a PMOS current source (M_{3_p}). Both complementary circuits use PMOS transistors as the input differential pair as in the target application the DC level at the CSA input is low.

Figure 39 shows CSA output waveforms for two cases: with and without a fast reset and for two types of feedback: standard MOS-based and double Krummenacher-type circuit. No DC level shift and therefore, no transient at the CSA output is visible after releasing the fast reset for the case with leakage current compensation, whereas when using a MOS transistor, this effect is quite significant. Moreover, from the waveforms, it can be concluded that long discharge time constant and also sufficiently large effective feedback resistance can be achieved for both types of feedback. The operation of the implemented feedback is stable for input charges from 2 fC to approximately 10 fC, for larger charges an overshoot is visible. This effect is growing with the increase of the pulse amplitude.

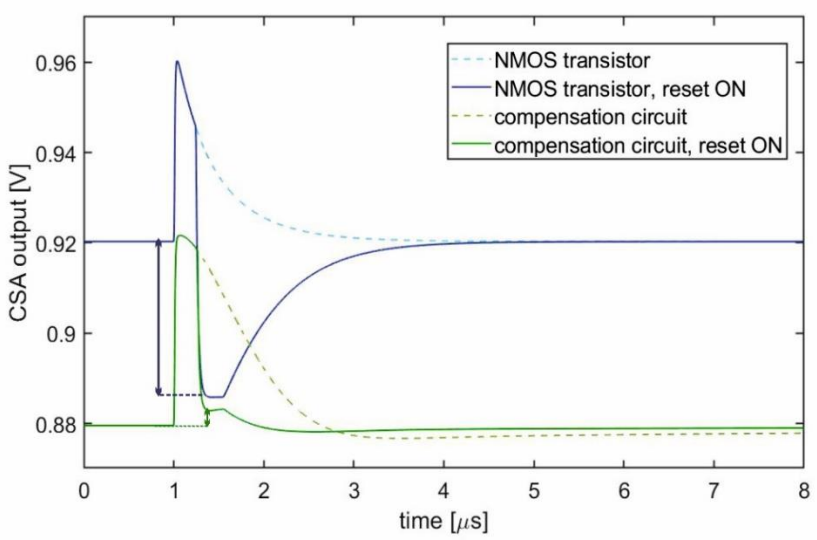


Figure 39 Comparison of CSA output waveforms for MOS transistor as a feedback resistor and Krummenacher feedback (bias current, IKrumm=12 nA) with and without fast reset enabled @ Ileak = 5 nA.

The effective feedback resistance for the Krummenacher circuit does not vary in the presence of the leakage current, whereas the discrepancies in the MOS feedback resistance are significant, as shown in Table 7.

Table 7 Relative effective resistance change for various feedback types.

Leakage polarity	**A relative effective resistance change**		
	Krummenacher feedback	**PMOS transistor (1 µ/10 µ)**	**PMOS transistor (4 µ/10 µ)**
Negative	0.28 %/nA (R_{nom} = 13.3 MΩ)	-9.71 %/nA (R_{nom} = 13.5 MΩ)	-10.16 %/nA (R_{nom} = 13.0 MΩ)
Positive	-0.21 %/nA (R_{nom} = 13.0 MΩ)	54.76 %/nA (R_{nom} = 13.7 MΩ)	50.97 %/nA (R_{nom} = 13.2 MΩ)

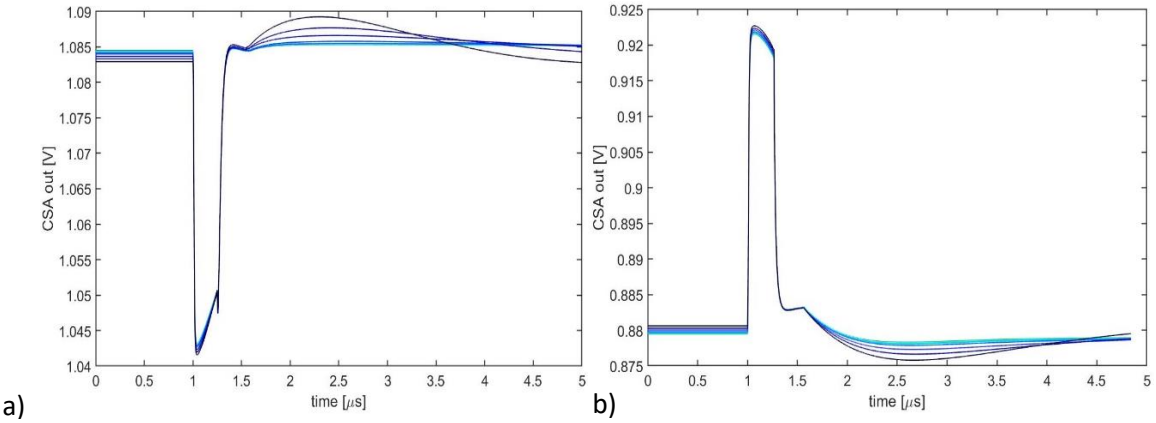


Figure 40 Simulated CSA output waveforms for leakage currents ranging from 1nA to 200nA, (@ Ikrum = 20 nA), a) for holes, b) for electrons

Figure 40 shows simulated CSA output waveforms employing a double Krummenacher-type feedback for two polarities of the input charge and a fast reset, for various leakage current values. An undershoot or overshoot, that are visible in the picture above for higher leakage currents is related to the shift of the feedback lowest frequency pole given by relation (22) [110]:

$$p_1 \approx -\frac{g_{m3}}{C_{Krum}} \quad (22)$$

Where g_{m3} is the transconductance of the current source (M_{3_n} or M_{3_p} depending on the selected signal polarity).

A negligible overshoot can be obtained by ensuring that the phase margin of the circuit is higher than 60°. The sizes of the PMOS and NMOS sources (M_3) were optimized to minimize the overshoot or undershoot, with respect to maximum leakage current present in the system and the area limit for the circuit layout. According to simulations results, the implemented feedback operates properly if the positive leakage does not exceed 80 nA, for negative polarity, the operation is stable up to 120 nA. The circuit performance deterioration was observed for leakage current reaching around 200 nA, which causes phase margin reduction to 52° and 55° for positive and negative input charge respectively and sets a limit for compensation abilities.

To evaluate the rate capability of the CSA with combined Krummenacher-type and fast-reset feedback, a double-pulse resolution simulations were performed. Estimation of the speed was based on a criterion that an error in the amplitude measurement does not exceed 1 LSB of the ADC used in exemplary readout front end (~0.5 fC [112]). Using only the Krummenacher feedback circuit, a channel occupancy up to ~870 kHit/s/ch was achieved, whereas adding a fast reset increases the speed up to 1.2 MHit/s/ch. Simulation results obtained for a standard MOS transistor as the feedback resistor showed a maximum channel occupancy up to 1 MHit/s/ch if the fast reset is applied without any leakage current flowing in the CSA feedback loop. If the leakage increases to even 1 nA, the input rate falls down to around 375 kHit/s/ch and is further reduced to ~150 kHit/s/ch for 5 nA of leakage as a result of feedback resistance shift.

A noise performance for an exemplary readout channel employing presented CSA feedback type was evaluated in simulations using a simple capacitor as a detector (which provides no additional sources of noise and parasitic components) from 10 pF to 30 pF. The peaking time of a CR-RC^2 semi-Gaussian shaper was used. Simulation results show, that the main noise contribution is related to the CSA input transistor (NMOS, W/L = 2.5 mm / 320 nm). Assuming no leakage current, the Krummenacher circuit bias current equal to 12 nA (resulting in effective feedback resistance of around 13 MΩ) and for maximum input capacitance, a simulated ENC value is equal to 480 e^- rms with slope ~8.6 e^- rms/pF and 483 e^- rms, slope ~9.5 e^- rms/pF for negative and positive input charge polarity respectively.

2.3. Slow shaping amplifier

Apart from careful design of the input stage and proper sizing the input transistor, given the sensor capacitance and making all remaining noise contributions negligible, filtering and signal shaping helps to improve the circuit SNR. A first step to design an efficient shaping amplifier is an evaluation of the noise

sources and indication of the dominant one and its type (current, voltage thermal or flicker). Depending on the level of these three noise types, the shaper order and peaking time value can be evaluated [25], [33].

Depending on the application (energy or time measurements of the incoming charge with required accuracy), an optimum filter can be employed to minimize the main noise contribution type, according to weighting coefficients shown in Table 8. For the mitigation of the white series (v_{nw}) and parallel (i_n) noise (assuming that the flicker noise can be neglected) a filter with an impulse response that is an indefinite cusp, gives the best results in the energy measurements. The decay time constant of its exponential slopes should be equal to a time constant related to the frequency at which these two noise types give identical contributions [33]. The ENC that can be obtained using this kind of filter can be expressed by the following equation [33]:

$$ENC = \sqrt{C_T v_{nw} i_n} \tag{23}$$

However, this kind of filters is not feasible to be applied in practical systems. They assume that the noise is white in the whole spectrum and that the filter impulse response is infinite. The most common real filter types with finite impulse response are triangular, unipolar and bi-polar filters containing real or complex conjugate poles in the transfer function [78]. The optimum filter architecture and its order depend on the dominating noise type to be minimized by proper weighting coefficients (Eq. (13) and (14) in Section 1.5.5). These coefficients, summarized in Table 8 for the most common filters, are calculated from the shapers transfer function and depend on the number of poles and zeros and their relation, however, are independent on their absolute *s*-plane location [33].

Table 8 Noise weighting coefficients for various shaper architectures.

Architecture	$\mathbf{A_w}$	$\mathbf{A_{1/f}}$	$\mathbf{A_i}$
CR-RC	0.92	3.69	0.92
CR-RC^2	0.85	3.41	0.64
CR-RC^3	0.93	3.32	0.52
CR-RC^4	1.02	3.27	0.45
CR^2-RC	1.03	4.70	1.00
CR^2-RC^2	1.16	4.89	0.72
Complex conjugate poles 3rd order	0.85	3.39	0.61
Complex conjugate poles 5th order	0.96	3.27	0.45

If the flicker and parallel current noise are to be minimized, the filters of higher-order provide lower weighting coefficients. The white thermal noise coefficient, however, can even increase for higher filter orders, as well as area occupancy and power consumption, especially for filters employing active stages. If the area and power are limited and have to be minimized, the complex conjugate poles transfer function can be employed for comparable or even better noise performance.

To find an optimum peaking time value, each of the noise types should be plotted against various peaking time values – the best peaking time value minimizes the series white and parallel noise

contributions (see Figure 41). These curves were plotted for various conditions, the total input capacitance equal to 13.9 pF (the sensor capacitance C_{det} = 10 pF) – the lightest ones are for the readout electronics limited to charge sensitive amplifier and feedback resistance (realized by a MOS transistor). The darker the curve, the more leakage sources were included in the calculations – for the current parallel noise sensor leakage currents (two values: 2 nA and 5 nA, separately), the leakage from the ESD protection circuit, parallel thermal noise from the sensor biasing resistance (in case of AC-coupled sensors). The series thermal noise was calculated for the channel noise alone, with the aluminium strip (R_{Al}), with micro-cable (R_{cable}), with interconnect resistance (R_{inter}) additionally (the darkest curve – all sources). The input transistor flicker noise does not depend on the peaking time and for the exemplary readout system, the ENC stays on the level of 92 e^- rms.

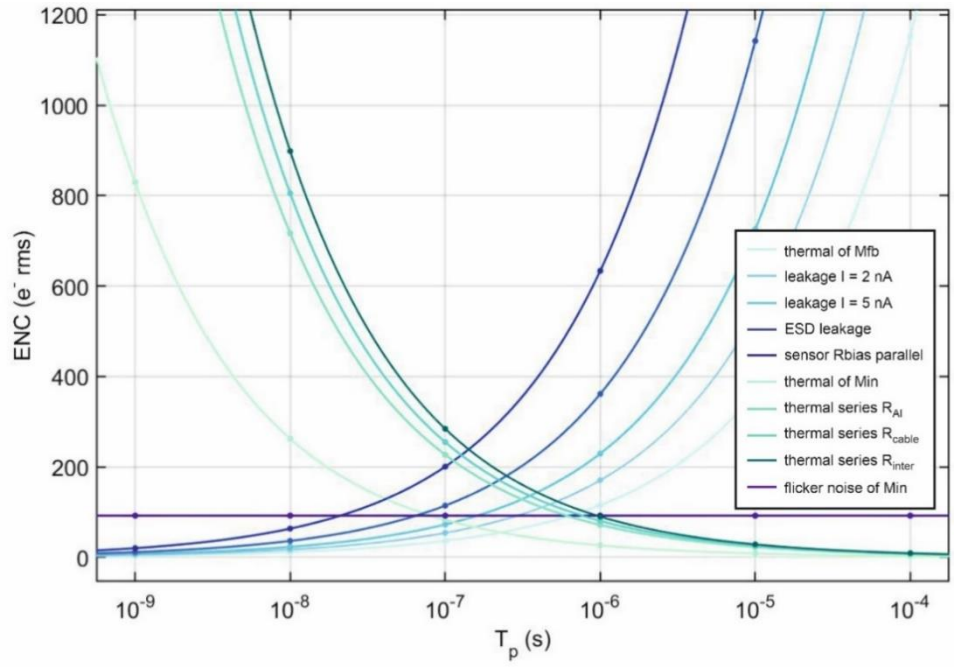


Figure 41 ENC for various conditions vs peaking time.

The optimum filter selection and multidimensional noise optimization require simulation of various filters architectures, given the acceptable peaking time range, with respect to timing requirements for the particular application. The performance of an exemplary charge processing chain for various semi-Gaussian shaping amplifiers orders and the influence of the presence of leakage current in the system on the optimization results is shown in Figure 42. It can be concluded that for this set of conditions and system parameters, the optimal peaking time is higher than assumed 90 ns, marked with a blue vertical line (a value required by this application). The presence of leakage current shifts this value towards shorter shaping times. It can be concluded that in this particular example the series voltage noise is considerably high.

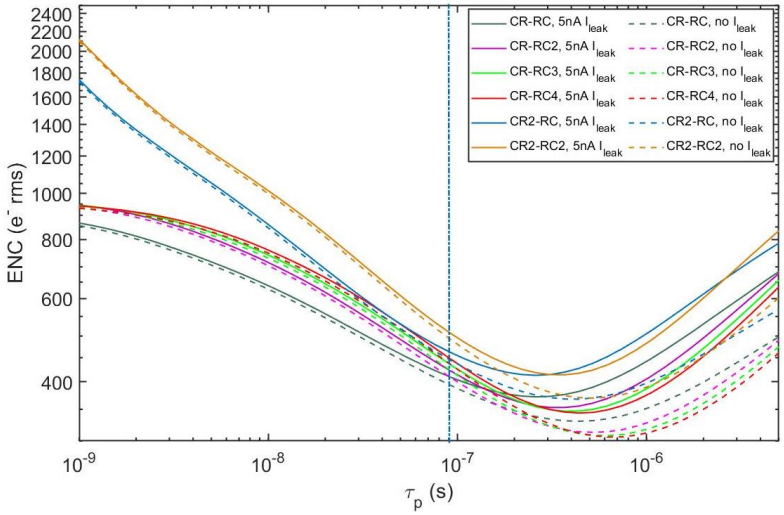


Figure 42 Simulated noise (ENC) for different shapers architectures - with and without leakage current. Pure capacitance connected to the CSA input (20 pF). Typical peaking time - 90 ns.

For the simulation of more realistic behaviour and noise, curves shape the models of application-specific cable and a double-sided sensor were prepared based on the parameters for the CBM experiment components. The distributed models used for the simulation for cable length equal to 49 cm and a sensor length of 4 cm are presented in Section 1.5.3. The simulations prove useful for estimation of the dominant noise type. In the final application, however, the second-order effects may play a significant role, contributing significantly to the noise level. System-level oriented evaluation of all external components like power supply noise coupling and going beyond the basic phenomena simulations is important to achieving very low-noise performance. Figure 43 shows the simulated ENC versus peaking time for the investigated system, with models of sensor and application-specific cables connected and, additionally, with a model of a custom noisy low drop-out (LDO) regulator used for all supply domains.

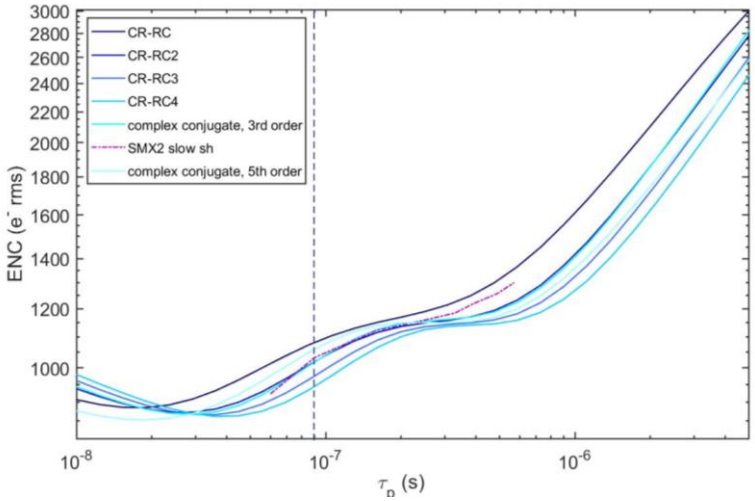


Figure 43 Simulated total output noise (ENC) for an LDO noise model (a custom LDO for CBM experiment), detector and cable models connected.

As can be concluded from the simulation results, shown in Figure 43, for this application the best noise performance, and lowest area and power consumption at the same time, can be achieved by employing a semi-Gaussian CR-RC^2 or 3rd order complex conjugate poles shaping amplifier architectures.

To design a CR-RC^2 shown in Figure 44 the values of passive components can be calculated as shown in the following equations (24) – (28). It can be assumed that the time constant of all stages is equal (30) for simplicity to achieve peaking time of 90 ns, and the total gain of the charge processing chain is known and determined. The value of the gain of the first stage (CR) was set to 10 mV/fC, resulting in a peak amplitude equal to 2.74 mV for a charge of 1 fC. To obtain a total gain of 35 mV/fC, the two RC stages should provide a total multiplication by 1.277, which is equally distributed among (1.13 V/V each).

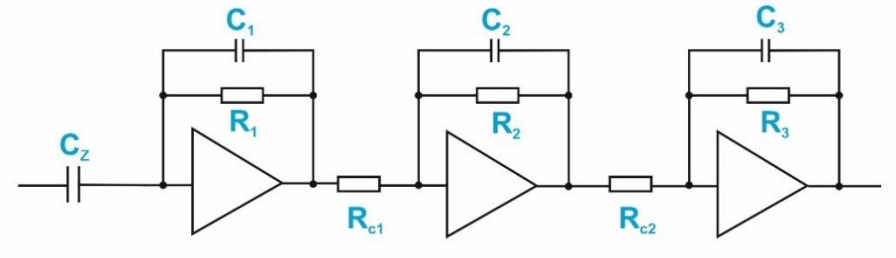


Figure 44 Semi-Gaussian CR-RC^2 shaping amplifier.

$$V_{out,max} = \frac{Q_{in}}{C_f} \cdot G \cdot \frac{n^n}{n!}\, e^{-n} \tag{24}$$

$$V_{out}(s) = \frac{I_{in}(s)}{C_f} \cdot C_z \cdot \frac{R_1 \cdot R_2 \cdot R_3}{R_{C1} \cdot R_{C2}} \cdot \frac{1}{(1+s\tau)^3} \tag{25}$$

$$V_{out}(t) = \frac{Q_{in}}{C_f} \cdot C_z \cdot \frac{R_1 \cdot R_2 \cdot R_3}{R_{C1} \cdot R_{C2}} \cdot \frac{1}{2!} \cdot \frac{1}{\tau} \cdot \left(\frac{t}{\tau}\right)^2 \cdot e^{-\frac{t}{\tau}} \tag{26}$$

$$\tau = R_1 C_1 = R_2 C_2 = R_3 C_3 \tag{27}$$

$$V_{out}(t) = \frac{Q_{in}}{C_f} \cdot \frac{C_z}{C_1} \cdot \frac{R_2 \cdot R_3}{R_{C1} \cdot R_{C2}} \cdot \frac{1}{2!} \cdot \left(\frac{t}{\tau}\right)^2 \cdot e^{-\frac{t}{\tau}} \tag{28}$$

The semi-Gaussian (CR-RC^n) shapers provide better noise performance, the more symmetrical is the impulse response. To achieve this, the shaper order should be increased, which imposes significant growth in the occupied area. For the best approximation of a true Gaussian filter shape, an infinite number of RC stages (n) is necessary, which is not applicable. To improve the symmetry of the impulse response, complex conjugate poles can be introduced in the transfer function. Figure 45 presents one possible implementation of such filter (a complex conjugate poles 3rd order shaping amplifier). This architecture was studied by Ohkawa et al. [113] and the idea is to obtain an impulse response that is the best approximation to a Gaussian function and can be realized using physical components [33].

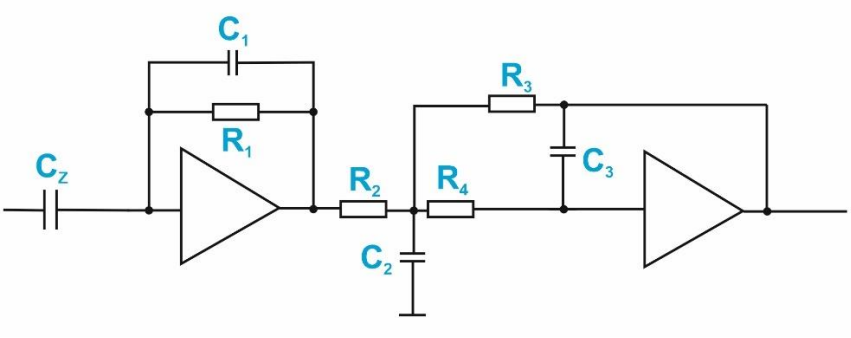


Figure 45 Complex conjugate poles 3rd order shaping amplifier.

In the following considerations, a transfer function of a second-order system will be used :

$$T(s) = \frac{{\omega_0}^2}{s^2+\frac{\omega_0}{Q}+{\omega_0}^2} \tag{29}$$

Where Q – quality factor (Q = 0.606 for CCP 3rd order shaper), ω_0 – angular frequency related to the poles.

The transfer function for the 3rd order shaper shown in Figure 45, is given in the Laplace domain by the Eq. (30), where C_f is the CSA feedback capacitance and I_{in} the input current signal (from the sensor).

$$T(s) = \frac{I_{in}}{C_f} \cdot \frac{C_z R_1}{(1+sC_zR_1)} \cdot \left(-\frac{R_3}{R_2}\right) \cdot \frac{1}{1+C_3R_3s+C_2R_4C_3R_3s^2} \tag{30}$$

For the complex conjugate poles shaper of 3rd order (the total number of poles n=3), the relation between angular frequency and peaking time is given by the following formulas:

$$\omega_0 T_p = 1.793,\ \omega_1 T_p = 1.976 \tag{31}$$

The angular frequencies ω_0, ω_1, the quality factor Q and the passive filter components are related by equations (32) – (34). The gain of each stage (A_{v0}, A_{v1}) is calculated using expressions in Eq. (35).

$$\frac{1}{\omega_0} = R_1C_1 \tag{32}$$

$${\omega_1}^2 = \frac{1}{R_3R_4C_2C_3} \tag{33}$$

$$\frac{1}{Q} = \sqrt{\frac{C_3}{C_2}} \cdot \left(\frac{\sqrt{R_3R_4}}{R_1} + \sqrt{\frac{R_3}{R_4}} + \sqrt{\frac{R_4}{R_3}}\right) \tag{34}$$

$$A_{v0} = \frac{C_z}{C_1}, A_{v1} = \frac{R_3}{R_2} \tag{35}$$

The passive elements of the shaper can be calculated explicitly using the above expressions and the following equations:

$$R_2 = \frac{1}{2A_{v1}\omega_1 Q C_3} \tag{36}$$

$$R_3 = \frac{1}{2\omega_1 Q C_3} \tag{37}$$

$$R_4 = \frac{1}{2\omega_1 Q C_3 (1+A_{v1})} \tag{38}$$

$$C_2 = 4Q^2(1 + A_{v1})C_3 \tag{39}$$

A comparison of the impulse response of the two shapers selected for this particular application and discussed above is shown in Figure 46. The shapers passive elements were selected so to make it possible switching between these two architectures, this is discussed in details in Chapter 3.

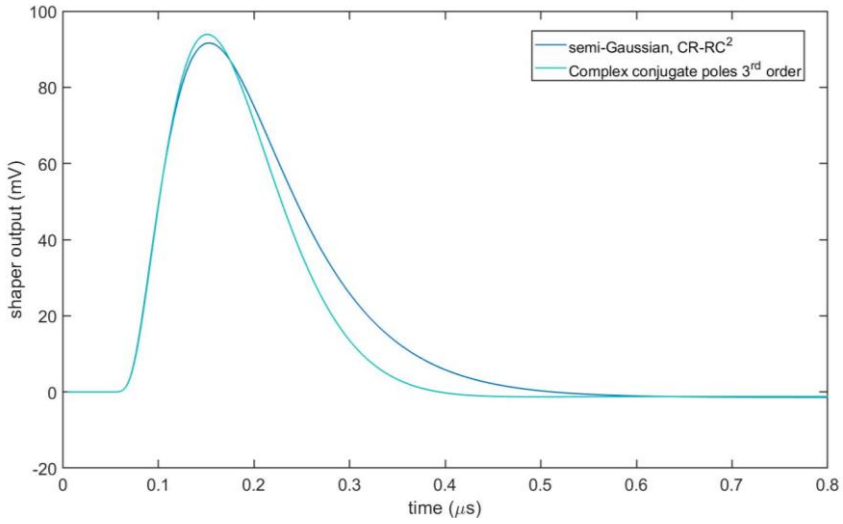


Figure 46 Comparison of shapers with real and complex conjugate poles in the transfer function, Q_{in} = 2 fC.

2.4. Fast shaping amplifier

For the timing applications, where timing resolution should be of ns range (or even less), a good noise-to-slope ratio of the signal is required. The optimum filter can be achieved by derivation of the indefinite cusp thus providing infinite slope for the jitter-free measurements. In practical applications, the slope is finite and much smaller than the one which results from the mathematical derivation, so the jitter is also higher [33]. Realization of a shaping amplifier for timing measurements requires achieving a fast rising edge and high gain, whereas the falling edge can be slower. A good candidate for this type of filter is a semi-Gaussian CR-RC architecture, the simplest type of shaping amplifier (Figure 47).

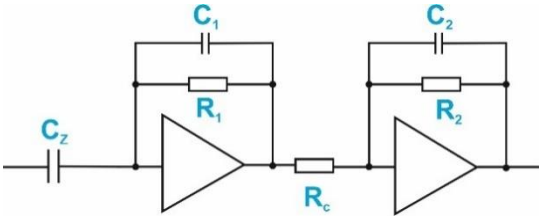


Figure 47 Semi-Gaussian CR-RC shaper.

The transfer function of this shaper in the Laplace domain can be written as [33]:

$$V_{out}(s) = \frac{Q_{in}}{C_f} \cdot \frac{\tau_{deriv}}{(1+s\tau_{deriv})\cdot(1+s\tau_{integ})} \tag{40}$$

In the time domain, the above equation is represented by:

$$V_{out}(t) = \frac{Q_{in}}{C_f} \cdot \frac{\tau_{deriv}}{\tau_{deriv} - \tau_{integ}} \cdot \left(e^{-\frac{t}{\tau_{deriv}}} - e^{-\frac{t}{\tau_{integ}}} \right) \tag{41}$$

In the above equations, τ_{deriv} and τ_{integ} are the derivation and integration time constants respectively, which can be made equal for simplicity and will be replaced by a τ, reducing Eq. (40) and (41) to the following forms, respectively:

$$V_{out}(s) = \frac{Q_{in}}{C_f} \cdot \frac{\tau}{(1+s\tau)^2} \tag{42}$$

$$V_{out}(t) = \frac{Q_{in}}{C_f} \cdot \frac{\tau}{t} \cdot e^{-\frac{\tau}{t}} \tag{43}$$

Using the passive components designators of the shaper network (Figure 47), the equation (43) can be represented in the form given below (Eq. (44)).

$$V_{out}(t) = \frac{Q_{in}}{C_f} \cdot \frac{C_z}{C_1} \cdot \frac{R_2}{R_c} \cdot \frac{\tau}{t} \cdot e^{-\frac{\tau}{t}} \tag{44}$$

The waveforms for exemplary shaping amplifiers of 1st and 3rd order are shown in Figure 48. Both shapers were designed for the peaking time T_p = 40 ns and the total gain of 115 mV/fC (assuming CSA gain around 13 mV/fC obtained in the simulation using a simple CSA model).

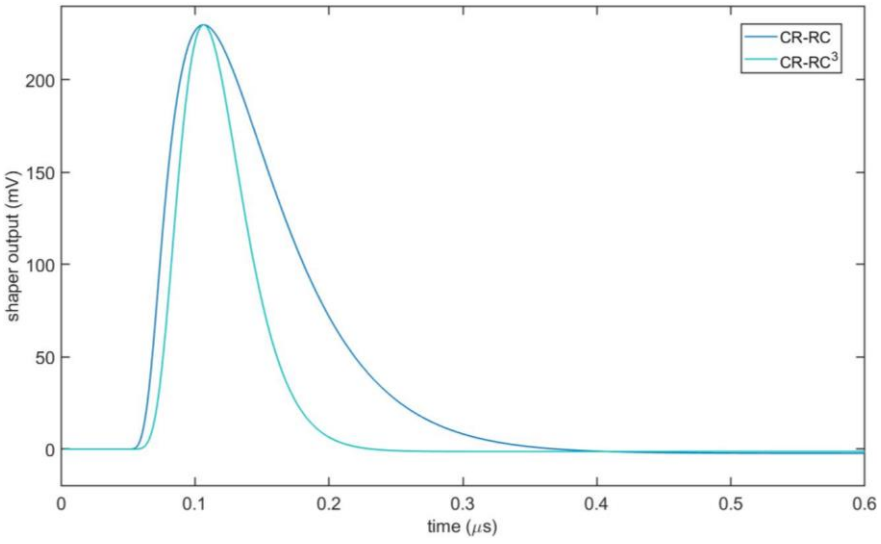


Figure 48 Impulse response of the CR-RC and CR-RC³ shapers, Q_{in} = 2 fC.

The comparison of the impulse response for these two shapers leads to the conclusion, that the fast leading edge of the CR-RC shaper makes it the best choice for timing applications than for more symmetrical CR-RC^3 type filter.

2.5. Design of the internal bias-potentials monitoring circuit

Measurement of the power supply voltage by the ASICs helps in effective fault-diagnostics in the readout system. The internal monitoring circuit is a solution enabling easy measurements of selected important potentials inside the chip. To meet reliability requirements it should be radiation-hardened by design and carefully characterized after fabrication with particular respect to long-term stability and TID-related effects. The circuit should maintain operability across the wide range of supply voltages and enable measurements of voltages close to supply rails.

The internal potentials monitoring circuit was designed and implemented using 180 nm CMOS technology and fabricated in Q3 2018 (MPW run July 2018) as an integral part of the SMX 2.1 ASIC. This circuitry occupies an area of 660 × 208 μm^2 and is fully controlled by accessing the register cells available within the chip address space [30]. The general architecture is shown schematically in Figure 49.

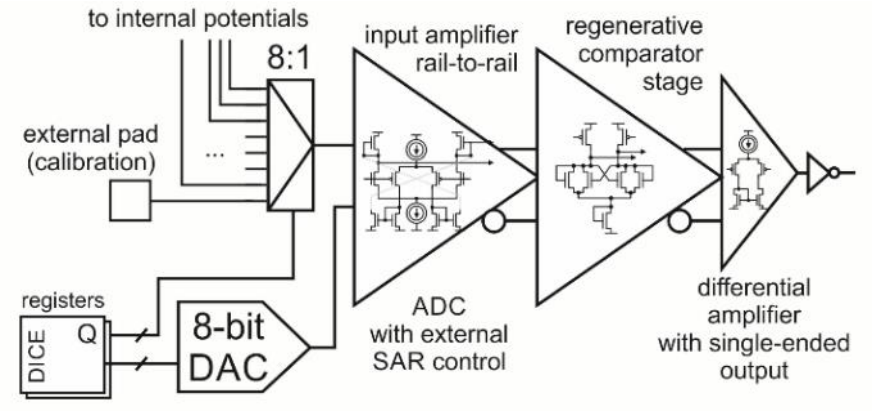


Figure 49 Monitoring circuit overview [102]

The biasing potentials monitoring circuit is realized as a 1-bit successive approximation register (SAR) analog-to-digital converter (ADC) which reference digital-to-analog converter (DAC) is controlled from the higher-level circuit in the DAQ system. The circuitry incorporates an 8:1 multiplexer enabling selection of particular voltage to be measured, an 8-bit DAC for setting a reference voltage and a 3-stage comparator with rail-to-rail input. The process of voltages scanning includes control of the input MUX, threshold potentials and reading-out the conversion result. This can be done at a maximum rate of 45 kHz, as a result of 8 successive approximation steps via regular register access through a dedicated protocol called STS-HCTSP (22 μs in total) [81]. The design of the circuit ensures that it can withstand an extended range of power supply voltage variation and a wide range of operating temperature (-20−85 ºC) without significant change in the performance. The radiation immunity of the circuit is improved by using enclosed-layout transistors (ELT) for NMOS devices [50], [103].

The diagnostic circuit was laid out (Figure 50) with radiation immunity assurance by using all NMOS transistors in Enclosed-Layout Geometry and equipping all transistors with individual guard rings. These layout techniques were tested and their radiation tolerance was positively verified during irradiation tests

[104]. For the improved matching, the first and second comparator stages use symmetric layout geometry. To reduce the switching noise the PCAP-type decoupling capacitors were placed as close as possible to the stages that generate fast edges. The digital-to-analog (DAC) converters using current mirrors are implemented as a symmetric matrix and connected using common-centroid topology. Additionally, for further improvement of matching a dummy transistor ring was placed around the matrix. All 8-bit memory cells used for control of the circuit were designed basing on dual-interlocked cells, which is a proven technique to prevent from single-event upsets (SEUs) [48].

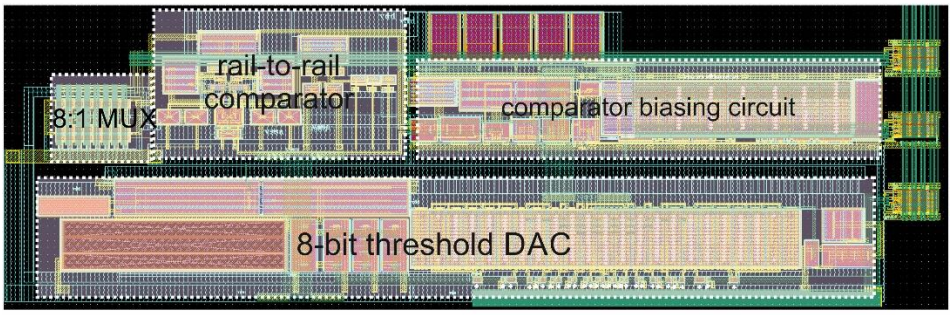


Figure 50 Layout of the diagnostic circuit.

The three-stage general-purpose comparator with a rail-to-rail input stage is presented in Figure 51 [105]. For the generation of comparator biasing currents, a bandgap reference source and a digital-to-analog converter are used. The currents can be selected in a range from 25 µA to 88 µA with 1 µA steps.

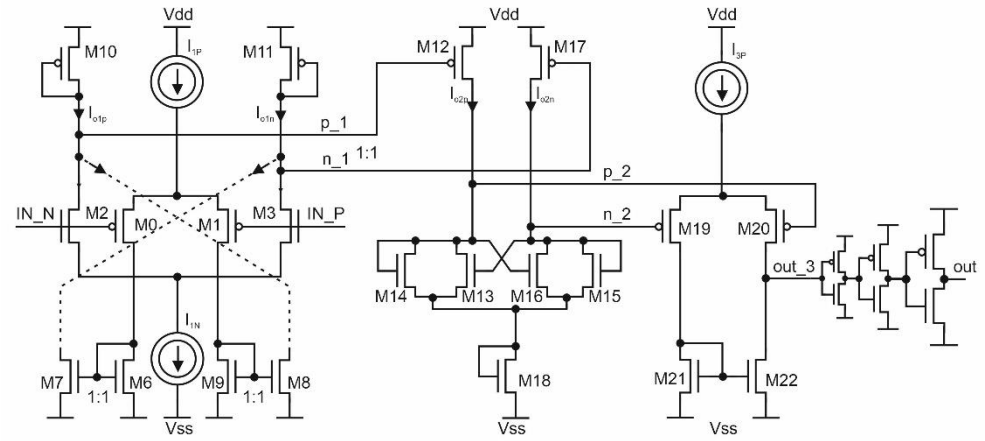


Figure 51 Three-stage comparator schematic.

The first stage is realized as a differential amplifier with PMOS and NMOS input transistor pairs to provide rail-to-rail operation. This is necessary to guarantee a constant Signal-to-Noise (SNR) ratio for various supply voltages and the highest possible input signals' swing [106]. As depicted in Figure 51 both input transistor pairs are biased with nominal 40 µA current, that is summed up in transistors M_{10} and M_{11} and mirrored by M_{12} and M_{17}. The differential output currents range therefore from approximately 0 to 80 µA.

The total gain of the comparator first stage and individual transistors transconductance (g_m) versus input common-mode voltage sweep are plotted in Figure 52. It can be concluded that up to a certain level, the total gain of this topology can be approximated by the algebraic sum of transconductances of the PMOS and NMOS transistors from the complementary input pairs.

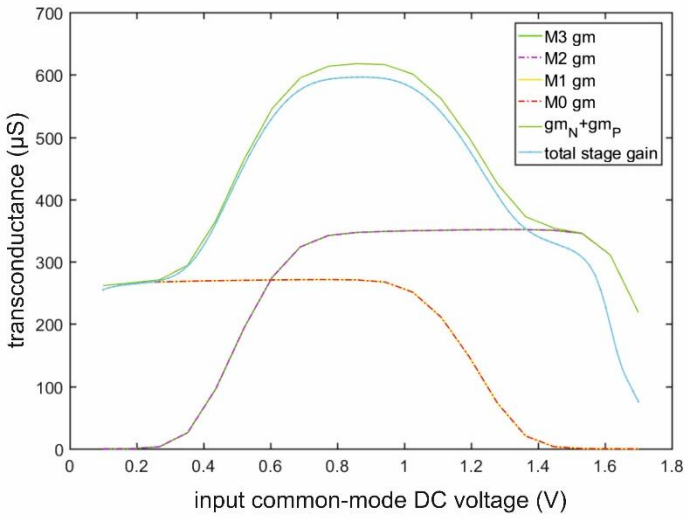


Figure 52 Transconductances of the individual transistors and the total gain of the comparator's first stage.

The rail-to-rail input stage is followed by a current-input regenerative comparator stage (see Figure 51). The pair of cross-coupled load transistors is employed to provide higher gain and to introduce hysteresis. The second stage outputs are determined by the following equations, where β_A is a characteristic value for a particular transistor equal to $\mu C_{ox}(W/L)$ [105]:

$$v_{op} = \sqrt{\frac{2 \cdot i_{op}}{\beta_A}} + v_{thn} \tag{45}$$

$$v_{on} = \sqrt{\frac{2 \cdot i_{on}}{\beta_A}} + v_{thn} \tag{46}$$

The diode-connected transistor M_{18} serves as the output voltage level shifter to adjust it to the common-mode range of the following stage [105]. The transistors sizes are chosen for non-zero hysteresis value with the loop width proportional to the relation (18) [105]. The aspect ratios are equal to $(W/L)_{14,15}$ = 20/0.5 µm and $(W/L)_{13,16}$ = 22/0.5 µm. The simulated hysteresis width equals around 4.43 mV.

$$v_h \sim \frac{\frac{W_{14,15}}{L_{14,15}} - \frac{W_{13,16}}{L_{13,16}}}{\frac{W_{14,15}}{L_{14,15}} + \frac{W_{13,16}}{L_{13,16}}} \tag{47}$$

The last stage is a buffer to convert the differential signals to the single-ended one with higher gain and fast rising edge. This stage is a PMOS-input pair differential amplifier with an active load and provides a gain (calculated as $g_{m19,20} \cdot (r_{o20} \| r_{o22})$) equal to 23.73 V/V.

The threshold voltage for the comparator is provided by an 8-bit DAC with binary scaled current sources architecture (Figure 53). For a generation of the DAC reference current external 1.2 V reference is

used. This can be provided by a band-gap reference source used in the chip incorporating presented biasing potentials monitoring circuit. A temperature-compensated set of resistors connected in series converts the DAC output current to voltage. The resistor types and values were carefully chosen basing on a study of temperature and voltage induced resistance variations among all resistor types available in the selected technology node (UMC 180 nm).

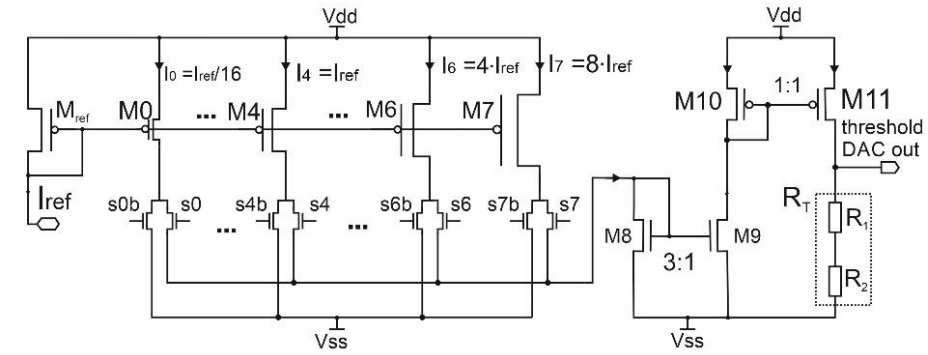


Figure 53 Threshold voltages generating DAC - schematic.

Various combinations of resistor pairs with opposite first-order temperature coefficient (TC) were considered to build resistance with a ratio matched to the TCs. To calculate the relative change of total resistance for two corner temperatures, the equations (48) and (49) and the data supplied by the IC manufacturer were used. The radar plot in Figure 54 presents the resulting relative changes for all considered resistor pairs – the closer to the plot center, the smaller is the change. The best two sets of resistors were selected for further considerations: "non-salicide P+ poly & N+ poly RF" and "non-salicide P+ poly & P+ salicide". While the first pair provides the smallest relative change of the total resistance, it was not chosen to be implemented in the circuit because of its availability limitations (only in the RF process). The second set is more universal and available in the standard process, so it was employed in the ADC output stage. The size ratio of the resistors was chosen to be R_1:R_2 = 1:11 to build a total resistance equal to 18 kΩ. The nominal value of the current flowing through this resistor is around 90 µA, which provides 0-1.6 V voltage range and an LSB equal to 6.27 mV.

$$R_1 = \frac{R_{opt.}\cdot\left[tc_{1,p}\cdot(T-T_n)+tc_{2,p}\cdot(T-T_n)^2\right]}{tc_{1,p}\cdot(T-T_n)+tc_{2,p}\cdot(T-T_n)^2 - tc_{1,n}\cdot(T-T_n)-tc_{2,p}\cdot(T-T_n)^2} \quad (48)$$

$$R_2 = R_{opt.} - R_1 \quad (49)$$

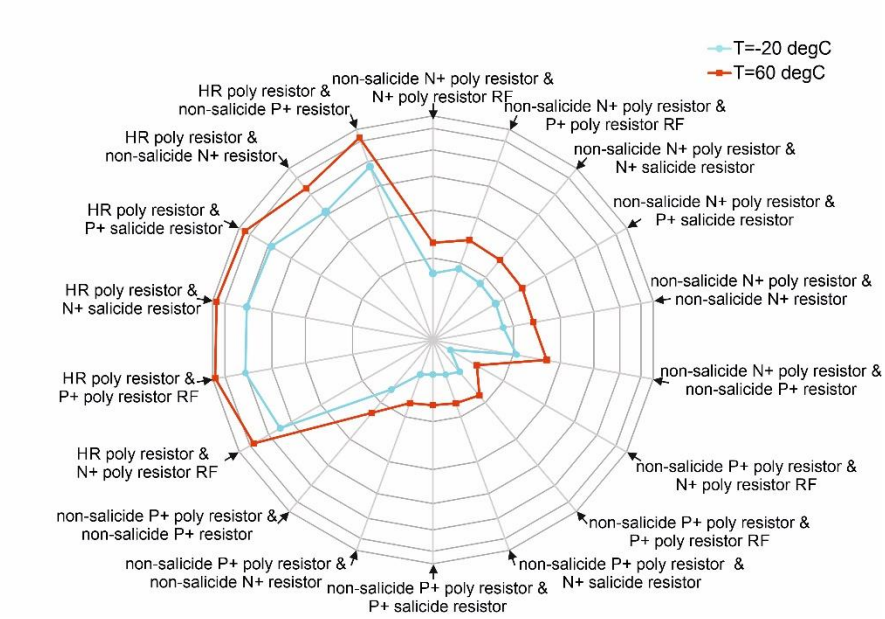


Figure 54 Relative changes of the total series resistance of the resistor doublets for corner temperatures.

A simple 8:1 analog multiplexer, presented in Figure 55, including also a decoder function, is used for the selection of voltage to be measured. It is built of transmission gates connected in series and controlled by three control lines. This architecture is easily scalable towards a larger number of input channels, if necessary.

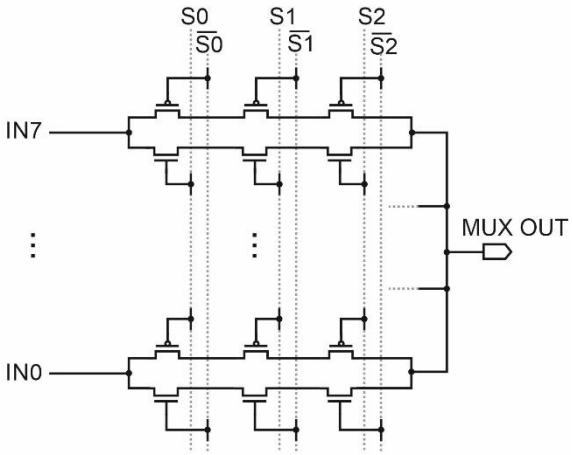


Figure 55 Schematic of the analog multiplexer

2.6. Characterization of the internal bias-potentials monitoring circuit

The circuit performance was thoroughly verified on the simulation level at nominal conditions and all possible variations (PVT, mismatch). The nominal performance was studied at input common-mode voltage set to half of the nominal power supply voltage (1.8 V) and temperature equal to 27°C. The summary of nominal performance, corner analysis and Monte Carlo simulations is presented in Table 9.

Table 9 Input stage simulated parameters.

Param.	Nominal conditions (DC=0.9 V, T=27 °C, V_{dd}=1.8 V)			
	Nominal value	**Monte Carlo mismatch**	**Monte Carlo process**	**Corners**
Gain (µA/V)	595.70	µ=592.96 σ=4.37	µ=590.45 σ=13.91	µ=592.55 σ=13.57
BW (MHz)	12.85	12.82	11.90	12.80

The gain experiences both power supply and temperature fluctuations. However, no significant degradation of the input stage performance (in terms of gain and bandwidth) is observed in corner and MC simulations. The gain versus power supply dependence has a slope equal to 572 µA/V within 1.3 V to 1.8 V range, and it is degraded to 270 µA/V at 1.2 V. The drift of the gain with the temperature exhibits a proportionality coefficient of 1 µA/V·K.

The differential output voltage of the second stage, plotted in Figure 56, were obtained for a sawtooth input signal for various supply voltages. The performance of this comparator stage is correct for the supply values from the nominal 1.8 V down to 1.1 V.

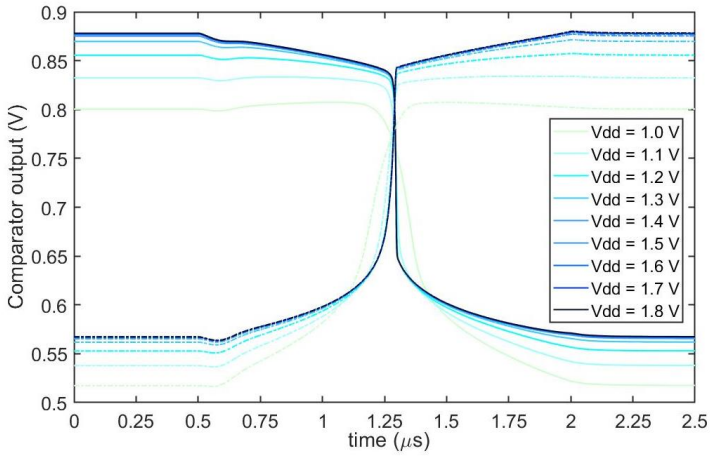


Figure 56 Comparator stage output waveforms for different supply voltages.

The comparator third stage simulated parameters for nominal conditions, mismatch, process variations and various corners are summarized in Table 10. The gain of this stage can be calculated as $g_{m19,20}\cdot(r_{o20}||r_{o22})$) and the nominal theoretical value equals 23.73 V/V. The simulated nominal gain is consistent with the calculated value. It can be concluded, that no major parameters change is introduced by mismatch and process variations.

Table 10 Output stage parameters

Param.	Output amplifier			
	Nominal value	**Monte Carlo mismatch**	**Monte Carlo process**	**Corners**
Gain (V/V)	23.55	µ=22.94 σ=0.89	µ=23.29 σ=1.36	µ=23.90 σ= 1.38
BW (MHz)	16.64	16.67	16.68	16.14

The comparator performance as a whole was also simulated for Monte Carlo mismatch and process variations and verified for various power supply voltage and temperature corners and the results are presented in Table 11.

Table 11 Comparator full-stage parameters

Param.	Nominal conditions (DC=0.9 V, T=27 °C, V_{dd}=1.8V)			
	Nominal value	**Monte-Carlo mismatch**	**Monte-Carlo process**	**Corners**
Hysteresis	4.43 mV	μ=3.46 mV σ=3.07 mV	μ=4.07 mV σ=1.02 mV	μ=4.29 mV σ=1.01 mV
Offset	42.08 fV	μ = 43.31 uV σ=3.85 mV	μ = 50nV σ = 364.58nV	μ = 25uV σ = 70.71uV
Delay	36.5 ns	μ=35.30 ns σ=10.28 ns	μ=36.12 ns σ=3.09 ns	μ=37.01 ns σ=3.20 ns

The impact of the power supply voltage fluctuations on the comparator performance is shown in Figure 57. The power supply can go down to 1.1 V without causing any severe performance degradation. The hysteresis loop width and the delay drops by approximately 2.34 mV/V and 30 ns/V respectively for the supply voltage drop from 1.8 V to 1.3 V. For this range, the comparator offset deviates from the nominal value by ±4.97 μV at maximum.

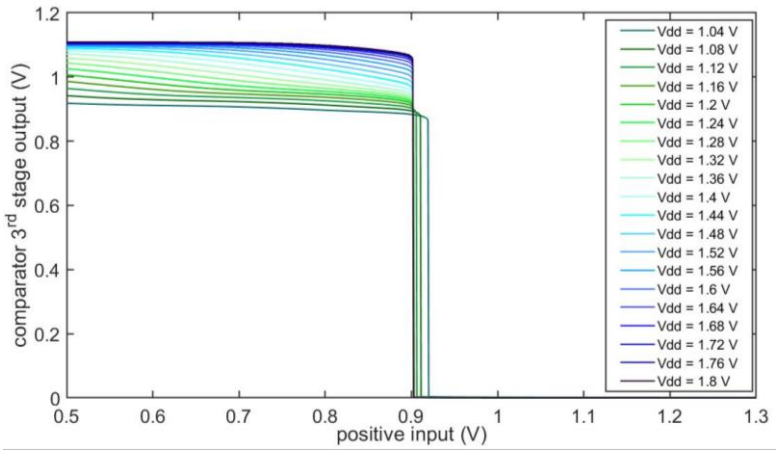


Figure 57 Comparator output for different supply voltages.

The simulated intrinsic comparator delay is equal to $t_d \approx 7.5$ ns. Figure 58 shows the comparator propagation delay for various overdrive voltages of the input signal. The rail-to-rail operation is correct and only slight signal degradation for threshold voltages very close to the supply rails was observed. The delay increases significantly (up to 10 ns) if the overdrive voltages are very low (below 100 mV). As the single conversion step for the whole circuit takes approximately 2.76 μs (defined by the register access), the delay almost three orders of magnitude lower does not affect the circuit performance.

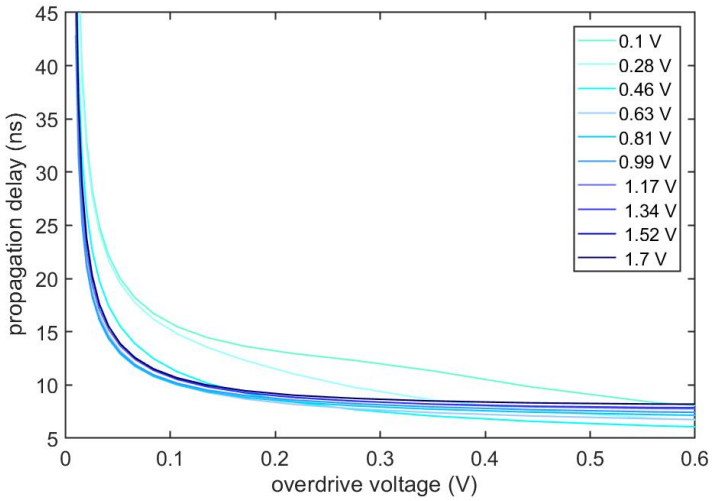


Figure 58 Propagation delay vs. overdrive voltage for different threshold voltages.

The hysteresis loop width was investigated across the whole input dynamic range. As can be seen in Figure 59, this value does not change significantly for input common-mode voltages up to 1.6 V. The comparator input-referred noise simulated value equals 82.66 μV_{RMS}.

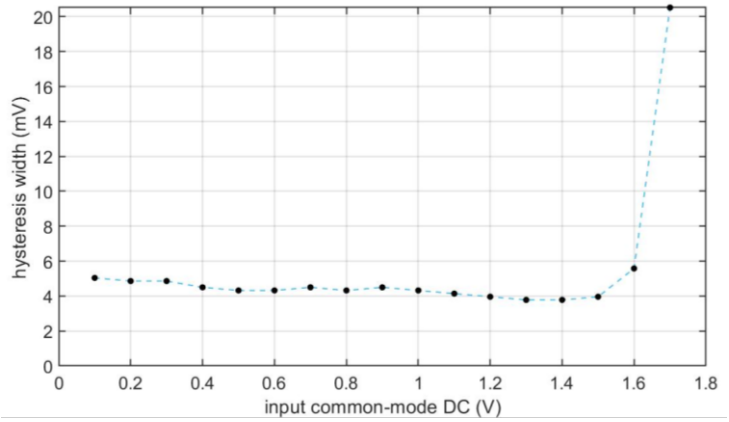


Figure 59 Hysteresis variations with comparator input DC level changes.

The robustness of the selected resistors pair to the temperature fluctuations was simulated and the results are shown in Figure 60. The behaviour of each element of the compensated resistor was studied and the maximum change within the selected temperature range was ≈250 µV and ≈2 mV for the non-salicide p+ poly and salicide p+ respectively. The maximum absolute change for the set of resistors did not exceed ≈8 µV. To keep the same output voltage for the nominal temperature (27 °C), the currents flowing through the resistors were normalized in the simulations.

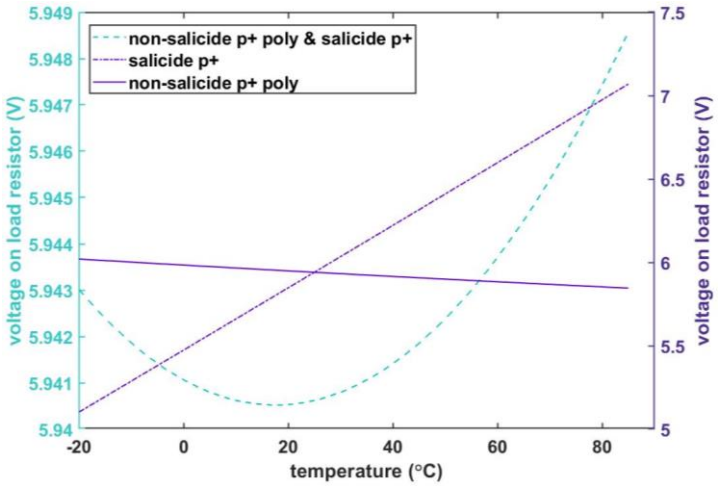


Figure 60 Temperature dependence of the full set and individual components of the selected doublet

Figure 61 shows transfer characteristics for the DAC loaded with the temperature compensated resistor for various values of the power supply. The first effect that can be observed is the bending of the curves for values close to the maximum DAC control code, which is caused by the designed DAC internal circuitry. The second issue is a significant gain loss for supply voltages below 1.4 V which is attributed to the band-gap reference circuit performance degradation.

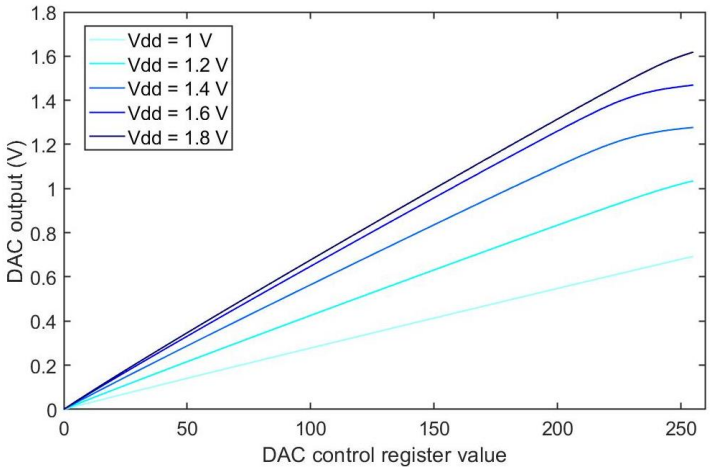


Figure 61 DAC output for different supply voltage levels

The differential and integral nonlinearity normalized to the LSB is presented in Figure 62 a) and b) respectively. The impact of the power supply variations is visible, nonetheless, the circuit keeps the monotonicity. In the nominal conditions, the INL value does not exceed 2% full scale. The performance degrades slowly as the band-gap reference circuit current drops for supply voltages below 1.4 V, which causes the reduction of the slope of the characteristics. The INL improvement was observed for even lower voltages, as the smaller steepness compensates other phenomena. The simulated noise contribution of the DAC in the whole circuit is 318.57 μV_{RMS} measured at the comparator output.

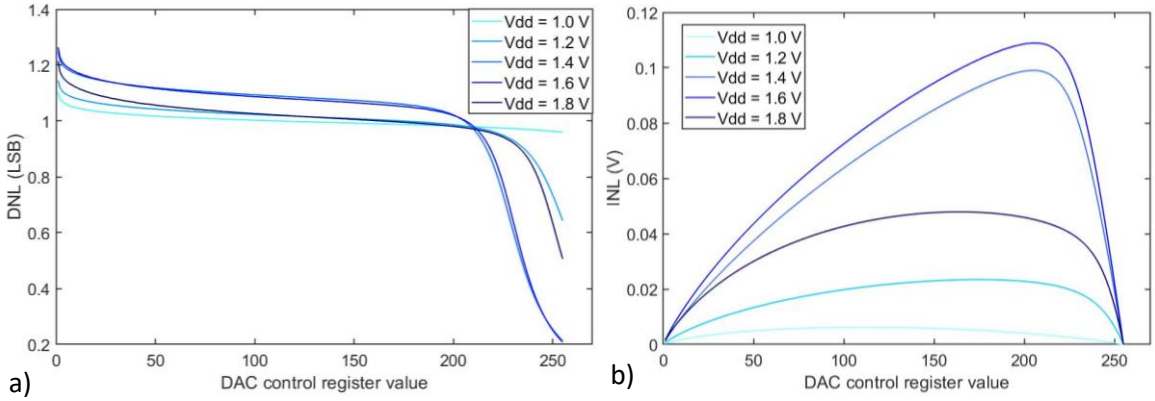


Figure 62 a) DNL changes with supply voltage variations, b) INL changes with supply voltage variations

The monitoring circuit propagation delay was simulated on schematic and post-layout levels. As shown in Figure 63 no significant degradation of the circuit operation speed was noticed. There are only slight differences between schematic and post-layout performance due to existing offset errors.

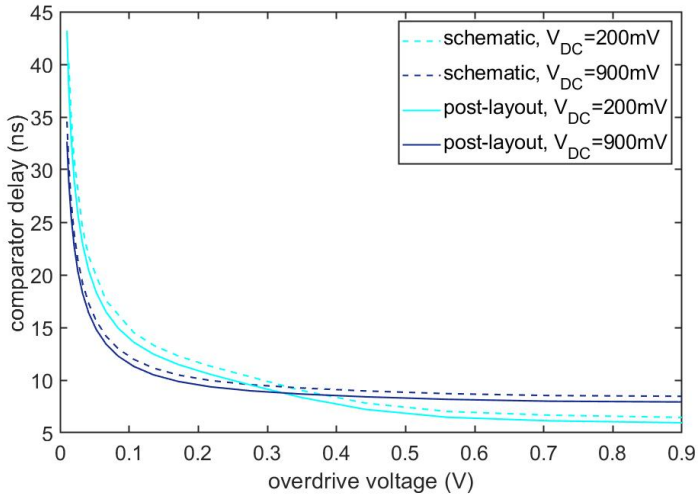


Figure 63 Comparator delay vs. overdrive voltage- schematic and post-layout simulation.

The presented diagnostic circuit simulated operation is proven to be robust to the power supply and temperature fluctuations. That enables usage of this component in the complex multichannel front-end readout for monitoring of the internal biasing potentials without additional pads for diagnostics as well as controlling the power supply voltage fluctuations during system operation, even in a radiation environment.

1.. Summary

A detector readout system is prone to noise stemming from various system components (internal and external) and all of them should be carefully examined for the readout electronics optimization. The intrinsic noise contribution (related to the readout electronics) should be kept on a much lower level than this from the external noise sources. The CSA noise optimization concerning the input transistor and some additional input amplifier transistors noise contribution is discussed. Apart from careful optimization of the input amplifier, given the sensor capacitance and all noise sources present in the system, an optimum filtering and signal shaping stages should be selected to improve the circuit SNR. A multidimensional noise

level optimization based on simulations of various filters architectures is required, taking into consideration the acceptable peaking time range, with respect to timing requirements for the particular application.

A known problem in detector readout systems is leakage current originating from various elements, leading to the parameters degradation or even instability (especially in HEP experiments, where high radiation intensity may lead to a great increase in the leakage of both the sensors as well as electronic devices). Some examples of issues related to the leakage current are the input amplifier's baseline shift, system saturation or increased noise. The exact value of the leakage determination is difficult and it can be higher than simulated values based on the foundry models. To mitigate the leakage-related effects, a switchable, double-polarity Krummenacher-circuit based architecture is proposed. The effective feedback resistance can be controlled within the MΩ range, not compromising the ability to the leakage compensation in the wide range. Combination of the switched-Krummenacher circuit with a fast reset of the CSA allows high input hits processing – up to 1.2 MHit/s/ch even in the presence of the leakage current.

Integrated circuits for radiation imaging and measurements applications should keep their parameters during the whole system lifetime in the harsh radiation environment and while being exposed to varying environmental conditions. The most common challenges for the development of the readout electronics include uniform and stable operation of all devices in the system during the whole lifetime, power-supply induced noise coupling, internal and external noise contributions, proper signal shaping and filtering, high input hits rate, leakage current compromising the electronics performance. In the tracking detectors, very often the number of multichannel integrated circuits is very high – up to tens of thousands. The radiation-induced effects affecting the performance of the sensors, readout electronics and other system components, put a requirement of constant system performance monitoring and faults detection. The parameters, that should be tracked for an insight into the electronics behavior, are biasing voltages and power supply levels of each ASIC. The aim of the design of the internal biasing potentials monitoring circuit was to enable remote measurement of important voltages inside the circuit during the read-out electronics for HEP experiments lifetime (for example 10 years) and eventual correction of the circuit's settings to restore the optimum performance in the harsh, irradiated environment and power supply fluctuation conditions. The circuit comprises an analog multiplexer, an 8-bit resolution threshold voltage generation digital-to-analog converter (DAC) and a comparator dedicated for slow, successive-approximation measurements. The total circuit area is equal to $660 \times 208\ \mu m^2$. The simulations of the presented diagnostic circuit operation prove that it is robust to the power supply and temperature fluctuations. It can be used in the complex multichannel front-end readout circuits for internal bias diagnostics without additional pads for each of them and controlling the power supply voltage fluctuations during system operation.

Chapter 3 SMX_mini ASIC, a prototype readout chip for silicon strip detectors

3.1. Overview of the chip architecture

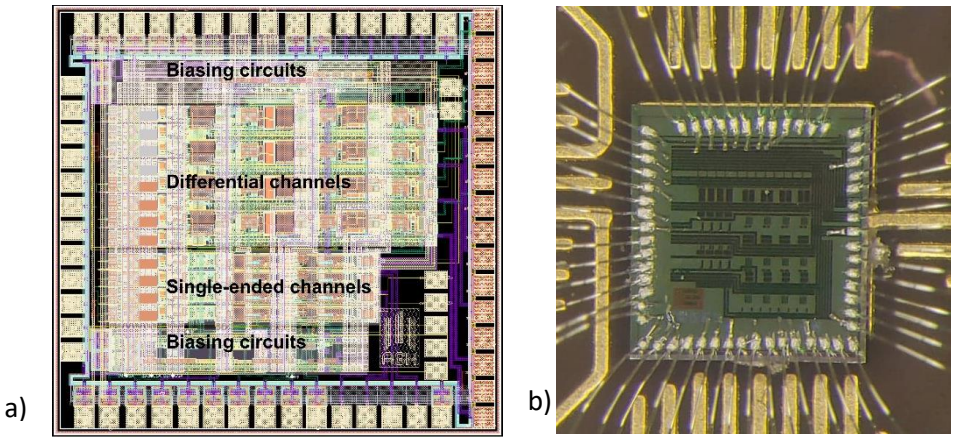


Figure 64 SMX_mini ASIC a) layout, b) photograph.

The SMX_mini ASIC (Figure 64) was designed and fabricated in Q4 2018 adopting 180nm CMOS technology and nominal 1.8 V power supply. It is a prototype 8-channel chip for readout of the silicon strip sensors designed based on the requirements for the CBM experiment (FAIR, Darmstadt, Germany) and dedicated for the double-side silicon strip sensors readout. Four of the charge processing channels are single-ended and four differential each of them dedicated for two input charge polarities (electrons and holes). The chip comprises biasing circuits shared among all channels. Single-ended channels can be configured to work in 16 operational modes. For the differential channels, there are four modes available. The ASIC features are summarized in Table 12. The IC area is 1.5 x 1.5 mm^2 and the power consumption is 88mW (single-ended: ~ 4.62mW/ch, differential: ~ 12.31mW/ch).

Table 12 Summary of the features and working modes of the SMX_mini.

Channel type		**Single-ended**		**Differential**	
Input charge		Electrons	Holes	Electrons	Holes
CSA feedback type	MOS resistor	✓		✓	
	Krummenacher	For negative leakage		×	
		For positive leakage			
Slow Shaper architecture	CR-RC^2	✓		✓	
	CCP 3rd order	✓		✓	
Polarity selection		Polarity Selection Circuit: **ON**	Polarity Selection Circuit: **OFF**	×	

3.2. Single-ended channels architecture

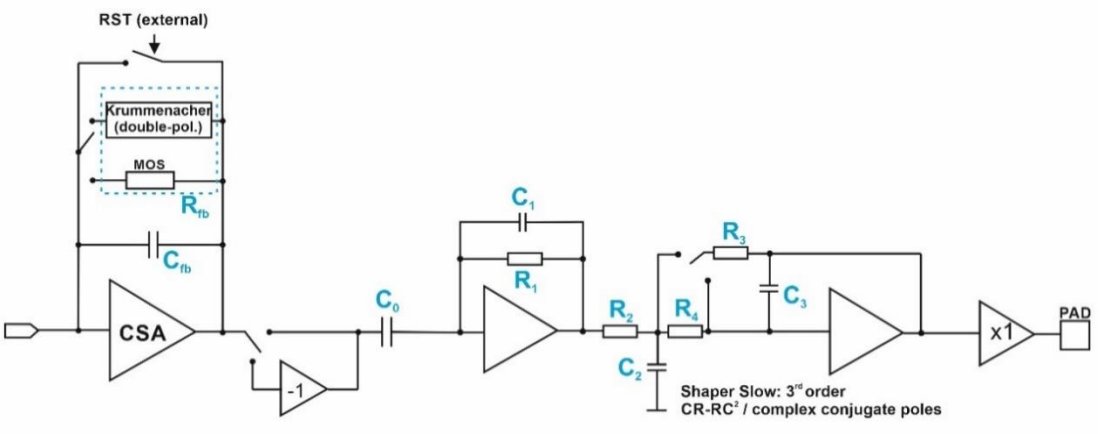


Figure 65 Single-ended channel schematic.

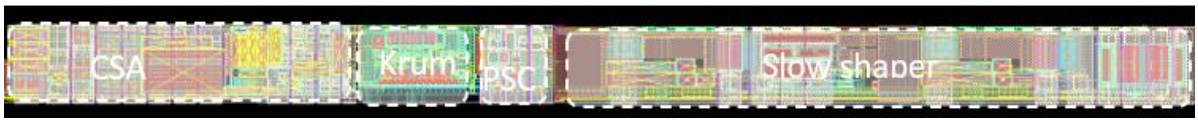


Figure 66 Layout of the single-ended channel.

The single-ended (SE) channel shown schematically in Figure 65 occupies an area of 950 µm x 60 µm and enables operation with two polarities of processed charge (electrons and holes), various feedback resistances and a pulsed reset circuit for fast baseline recovery. The charge processing chain comprises of Charge Sensitive Amplifier (CSA), Polarity Selection Circuit (PSC) [114] and 3rd order shaping amplifier (shaper) with selectable architecture (CR-RC^2 or complex conjugate poles, CCP – multiple feedback architecture) – see Figure 65 and Figure 66.

The CSA core is a circuit used in the SMX ASIC for the CBM experiment. Its architecture is a direct cascode voltage amplifier with split bias current and the input transistor is an NMOS with the length almost the double of the minimum length for this technology (180 nm) [114], [115]. The nominal current for the CSA operation is 2 mA and it is sourced by a current source connected to the lower than used for the whole design power supply (1.2 V) to reduce the power consumption [114]. The core amplifier for the nominal current setting has a gain equal to 4.8 kV/V and the gain-bandwidth product (GBW) of 8.1 GHz [114]. The CSA feedback is selectable between MOS transistor working in the linear region and double-polarity Krummenacher circuit for leakage compensation (see section 2.2).

The shaping amplifier core architecture is a folded cascode voltage amplifier with voltage gain equal to 2.5 kV/V and GBW of 1.3 GHz [114]. The polarity of processed charge is selected by the PSC – for the holes, the CSA output is directly connected to the shaping amplifier, whereas for the electrons the CSA output signal is reversed by a differential pair-based unity gain reverting amplifier [114]. Both shaping amplifier architectures, CR-RC^2 and CCP 3rd order set the shaping time value to around 90 ns. The slow

shaper architecture is depicted in Figure 65 and the values of the passive components are summarized in Table 13.

Table 13 Passive components values for the semi-Gaussian and complex conjugate poles filter configuration.

	CCP 3rd	**CR-RC²**
C_{in}	2p	2p
C1	400f	400f
R1	116k (116.4k)	116k
R2	40k (38.91k)	40k
C2	1.8p (1.9p)	1.8p
R4	27k (26.9k)	24k
R3	88k (87.16k)	166k
C3	400f	400f

The resulting values of peaking time and gain related to input charge for both types of filters are presented in Table 14. It can be seen that for both kinds of signal filtration the achieved charge processing parameters are very similar which make noise level comparison possible.

Table 14 Peaking time and input charge related gain for the single-ended channel (simulated values).

	CCP 3rd	**CR-RC²**
t_p [ns]	85.41	85.56
gain [mV/fC]	38.02	37.71

The front-end was simulated on the schematic and post-layout level for two input charge polarities and with an input capacitance of 10 pF. Exemplary waveforms for negative input charge of 2 fC at each test point: CSA output and shaper output, are shown in Figure 67 a) and b) respectively.

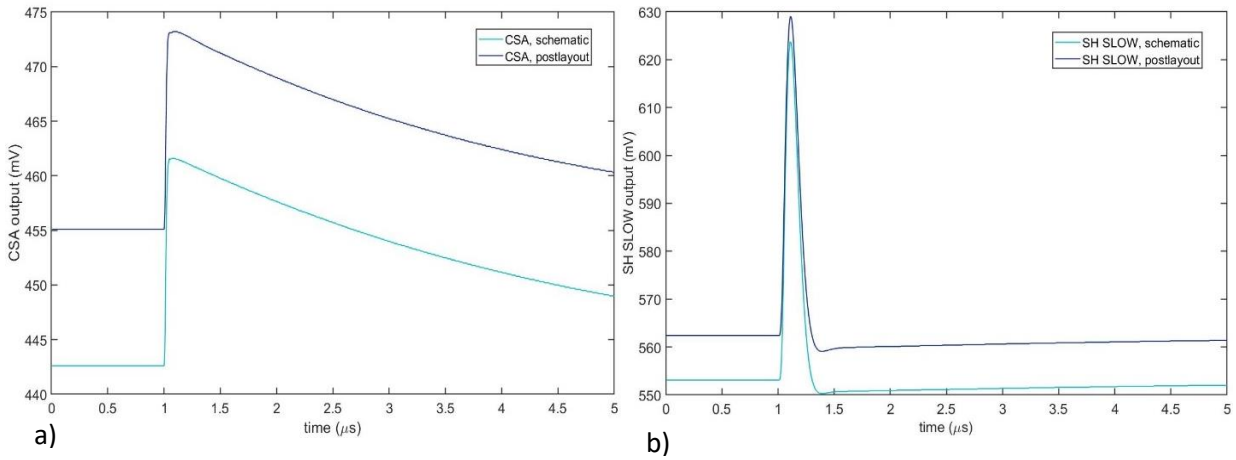


Figure 67 Single-ended channel output waveforms post-layout versus schematic for electrons, input charge 2 fC: a) CSA, b) slow shaping amplifier.

The charge processing channel schematic vs. post-layout performance comparison for the single-ended channel is summarized in Table 15 for both negative and positive input charge. Some differences are visible (gain loss and longer peaking time in case of shaping amplifier) but no significant performance degradation was observed.

Table 15 Simulated values of peaking/shaping time and gain for CSA and shaper for both polarities.

	Schematic (e^-)	Post-layout (e^-)	Schematic (e^+)	Post-layout (e^+)
CSA gain (mV/fC)	9.69	9.51	9.21	8.85
CSA tr (ns)	40.89	40.81	41.07	41.33
SH_slow gain (mV/fC)	36.54	35.42	33.9	32.29
SH_slow tp (ns)	96.61	97.68	92.97	94.61

3.3. Differential channels architecture

The differential channel schematically shown in Figure 68 occupies an area of 1150µm × 125µm. The channel architecture is pseudo-differential as it contains a single-ended CSA and its replica (Figure 69) [116] which is not scaled in terms of area and power for the best power supply interference rejection. The CSA core is identical as in the SE channels, the feedback is only MOS-based (and the Krummenacher circuit is not used here for simplicity and area limitations). This type of channel contains fully differential 3rd order shaping amplifier with switchable architecture (CR-RC^2 and CCP identical as in SE channel). The shaping amplifier inputs switching enables selection of the processed charge polarity.

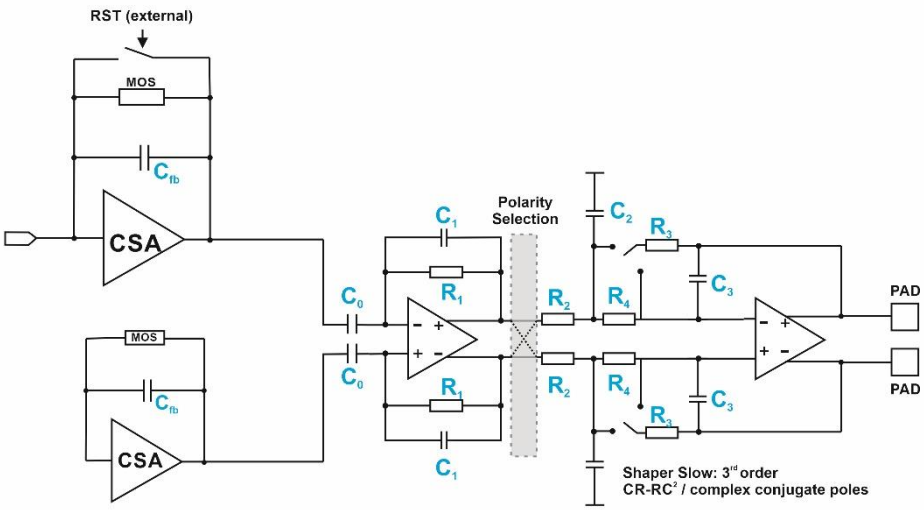


Figure 68 Differential channel schematic.

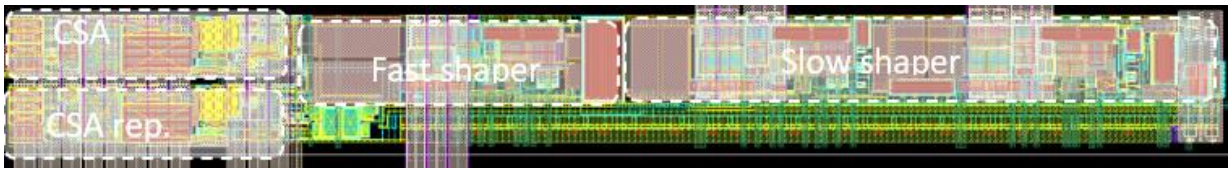


Figure 69 Layout of the differential channel.

A fully differential folded-cascode operational amplifier with common-mode feedback (CMFB) was used as the shapers' core [106], [117]. The transistors in the amplifier's input pair are PMOS (Figure 70). For the stable operation and keeping the output voltage on a constant level, a common-mode reference potential is set to 0.9 V (this potential is accessible from outside through a pad and provides tunability in

case of mismatch or process variations). The common-mode (CM)-sense network employs resistors and capacitors to take the average of the two outputs of the differential amplifier for comparison with the reference voltage to provide a balanced output [116]. Using resistors to detect the CM is the most straightforward way, however, the disadvantage of this approach is a pole in the common-mode feedback loop, introduced by the resistors and the input capacitance of the CM-sense (or error) amplifier. To reduce the effect of this pole in higher frequencies (leading to stability issues), capacitors were placed in parallel with the resistors in the sense network. Loading of the main operational amplifier outputs by the sensing resistors causes degradation of the open-loop voltage gain. To avoid it, these resistors should be much larger than the impedance of the differential amplifier output branches [117]. Placing such large resistors inside an integrated circuit is not feasible and increases the occupied area, so another approach was implemented. In this design, complementary voltage buffers are added to the inputs of the CM-sensing network. This approach ensures proper operation in the wide input voltage range and eliminates a voltage offset caused by the V_{GS} of the voltage buffers. The core simulated open-loop GBW is equal to 1.91 GHz and gain equals 800 V/V.

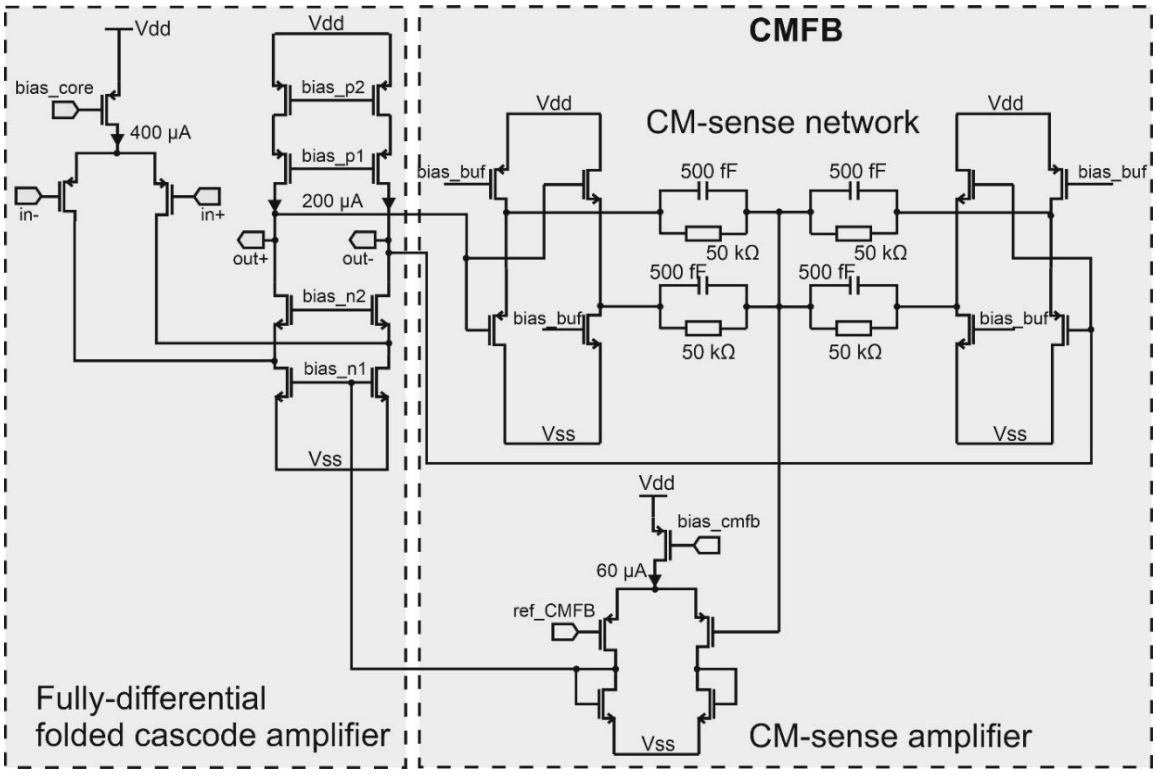


Figure 70 Slow shapers core - fully differential folded cascode amplifier with common-mode feedback.

The passive components values are selected to be identical (or scaled) for both types of channels and both shaping amplifier architectures. These components are built from identical smaller passive elements to reduce the mismatch and to make switching easy (changing the value by adding or subtracting one smaller element). These values are summarized in Table 16.

Table 16 Passive components values for the semi-Gaussian and complex conjugate poles filter configuration.

	CCP 3rd (DIFF)	CR-RC2 (DIFF)	CCP 3rd (SE)	CR-RC2 (SE)
Cin	2p	2p	2p	2p
C1	400f	400f	400f	400f
R1	116k	116k	116k	116k
R2	40k	40k	40k	40k
C2	1.8p	1.8p	1.8p	1.8p
R4	25k	20k	27k	24k
R3	88k	166k	90k	166k
C3	400f	400f	400f	400f

Table 17 shows the comparison of the essential parameters obtained for both architectures of the shaping filters in the single-ended and the pseudo-differential channels using the values of the passive components presented in the table above. The performance of the shapers does not show significant differences between two types of filter architectures and discrepancies between channel types are acceptable from the noise comparison point of view.

Table 17 Peaking time and input charge related gain for differential channel compared to the single-ended (simulated values).

	CCP 3rd (DIFF)	CR-RC2 (DIFF)	CCP 3rd (SE)	CR-RC2 (SE)
t_p (ns)	90.24	89.67	85.41	85.56
gain (mV/fC)	35.71	36.96	38.02	37.71

The front-end simulation results on the schematic and post-layout levels are presented in Figure 71 a) and b) for CSA and slow shaper respectively. These plots were obtained for positive input charge equal to 2 fC and with an input capacitance C_{det} = 10 pF. CSA baseline shift is observed of around 30 mV but it still allows for processing the charges in the targeted full range (up to at least 10 fC).

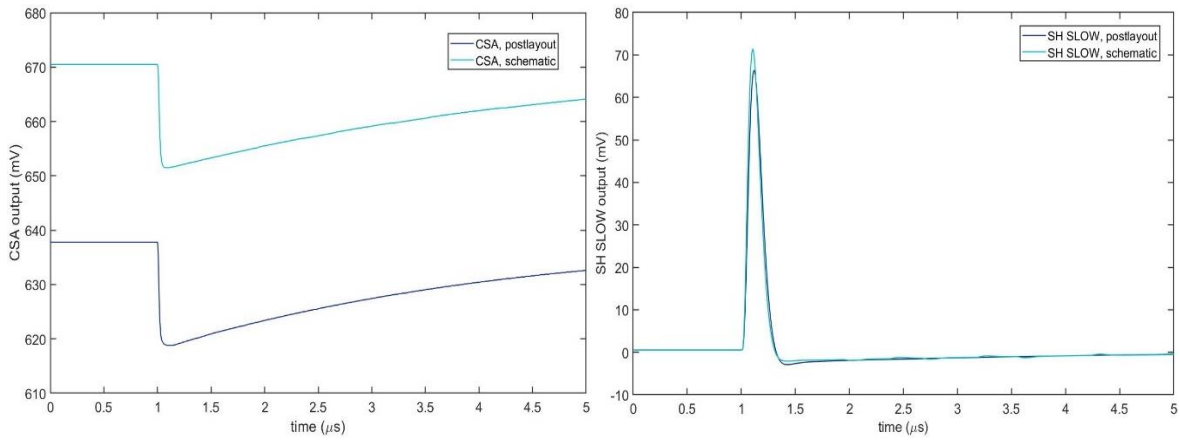


Figure 71 Pseudo-differential channel output waveforms post-layout versus schematic for holes, input charge 2 fC: a) CSA, b) slow shaping amplifier.

The performance comparison for pseudo-differential channel for schematic-post-layout simulations is presented in Table 18 for both charge polarities. As for the single-ended channels, there are some differences between schematic and post-layout performance (gain loss and longer peaking time).

Table 18 Simulated values of peaking/shaping time and gain for CSA and shaper (CCP) for different polarities.

	Schematic (e^-)	Extracted (e^-)	Schematic (e^+)	Extracted (e^+)
CSA gain (mV/fC)	9.46	9.26	9.53	9.23
CSA tr (ns)	53	64	48	58
SH_slow gain (mV/fC)	36.51	35.39	33.93	32.54
SH_slow tp (ns)	95.16	97.68	91.07	96.3

3.4. Test setup and software

The fabricated ICs were tested and characterized in all of their operating modes. The ICs were assembled on the dedicated test Printed Circuit Boards (PCBs, Figure 72) using a wire-bonding technique. Test PCB was designed for easier reuse in future designs just by changing the chip footprint and relevant pins to shorten the design time. It comprises passive components for generation and control of biasing potentials (resistors and trimmer potentiometers), decoupling capacitors as close to the ASIC as possible to keep the power integrity. The design comprises two power supply domains (1.8 V and 1.2 V) and it can be connected directly from laboratory power supply device or generated by DC-DC converters. To conduct noise measurements for various converters the PCB comprises two connectors to use with the custom-designed linear voltage regulator for the CBM experiment designed by Variable Energy Cyclotron Centre, Kolkata, India or to connect dedicated mezzanine boards with selected off-the-shelf devices. The PCB provides test points for important biasing/internal potentials to make debugging easier. All output signals are connected to SMA connectors, that can be also used for direct connection of active single-ended or differential probes.

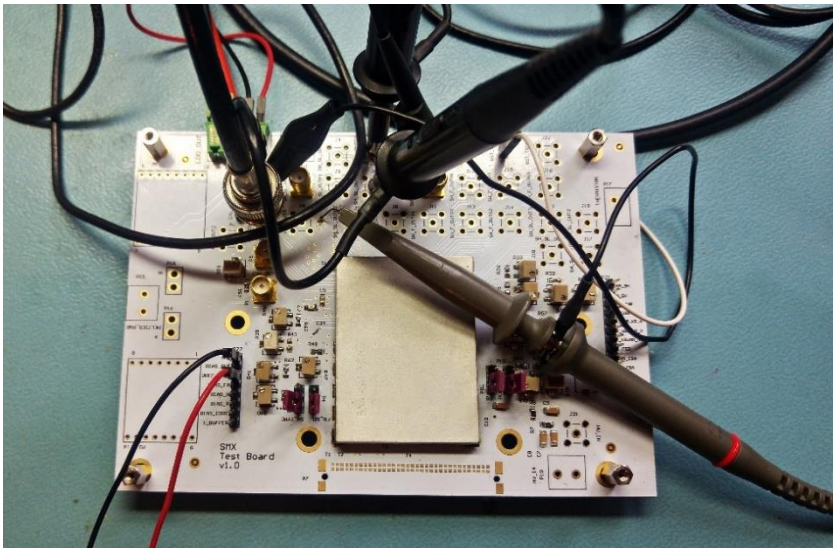


Figure 72 Test PCB with scope probes connected to test points.

The test setup presented in Figure 73 included a Keithley 2231A-30-3 triple channel laboratory DC power supply, a Tektronix AFG 3251C arbitrary waveform generator (τ_r = 2.5 ns) for the external calibration pulse generation and a Tektronix DPO 7354C 3.5 GHz bandwidth oscilloscope with differential

3.5 GHz active probes ($C_{in} \leq 0.8$ pF) for waveforms acquisition. The Keithley 6487 Picoammeter-Voltage Source was used for the leakage current effects and compensation verification.

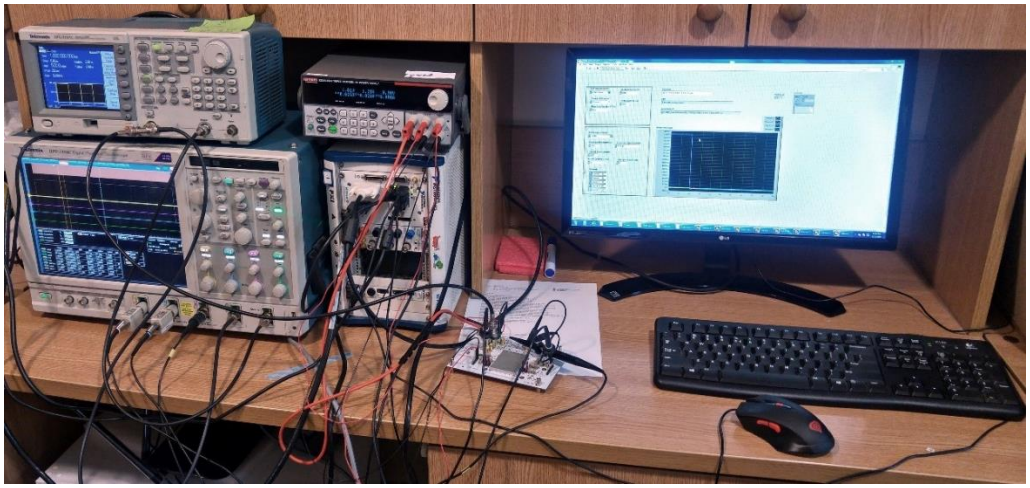


Figure 73 SMX_mini test setup.

A custom test software was prepared using the LabVIEW environment and National Instruments PXI platform. The application allows for communication with the measurements equipment to be able to conduct automatic or semi-automatic tests by a generation of calibration pulses and acquisition of the IC output waveforms. It automatically sets the calibration pulse amplitude to obtain gain characteristics and saves the waveforms acquired from the scope to files indicating test settings in the name.

3.5. Functional characterization of the ASIC

First, the functional characterization of the IC was performed to obtain gain characteristics for both stages of the charge processing chain. The measurements results are consistent with the simulations so the chip operates correctly. As can be seen from Figure 74, showing CSA transfer function obtained for negative input charge polarity (electrons), there are no significant differences between the CSA gain in single-ended and pseudo-differential channels. The average gain for both types of channels and all possible operation modes is equal to 9.08 ± 0.55mV/fC and the integral non-linearity (INL) between 0.34% and 1.59% full range (depending on the channel type and operation mode) for charges up to 10 fC [118].

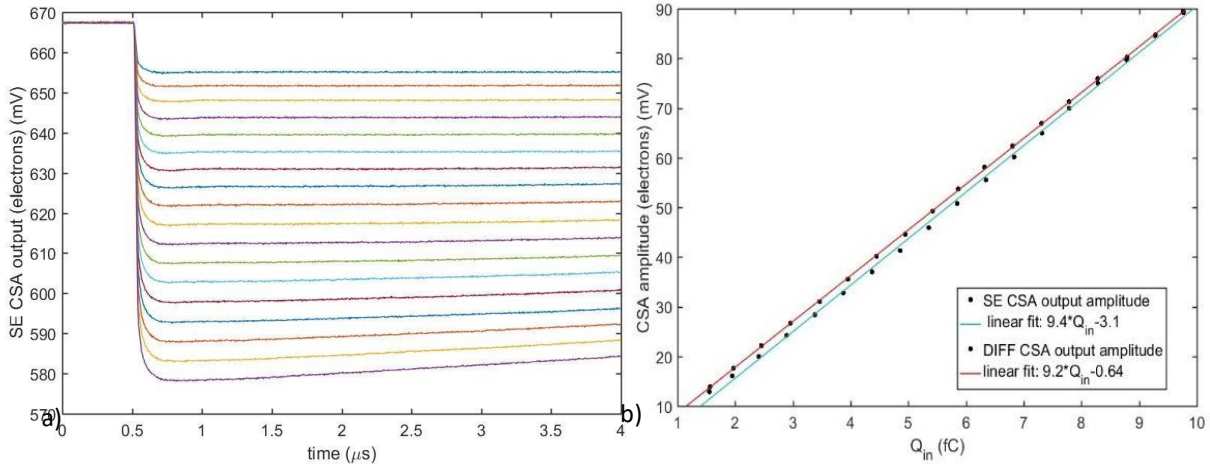


Figure 74 Measured CSA a) output waveforms and b) transfer function for input charges 0.5fC to 10fC.

Figure 75 shows the shaping amplifier gain characteristics evaluated for all configurations and channel types. The calculated average gain of all the operation modes is 33.67 ± 1.67 mV/fC. The integral non-linearity (INL) of the transfer functions varies between 0.44% and 2.48% full range for charges up to 9.5 fC depending on the channel type and configuration. The peaking time measured values are in the range from 94 to 98 ns, which is consistent with the simulated value around 90 ns.

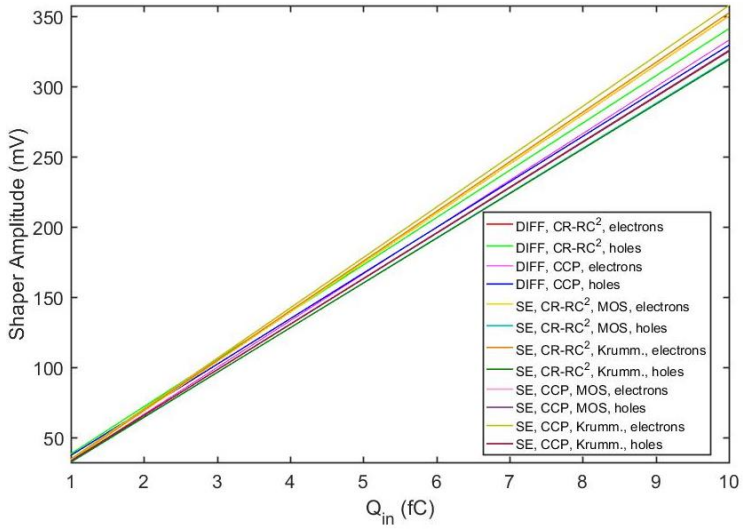


Figure 75 Measured shaper's characteristics — transfer function for charges 0.5–10fC.

The performance of the SMX_mini ASIC is summarized in Table 19. Mean values and standard deviations of all operation modes are compared for SE and DIFF channels. It can be concluded that there are no big differences between the performance of the ASIC considering charge processing type. This conclusion is useful from the noise performance comparison point of view.

Table 19 Summary of measured charge processing characteristics

Channel type	Single-ended (mean ± sigma)	Differential (mean ± sigma)
CSA gain (mV/fC)	8.813 ± 0.383	9.425 ± 0.263
CSA peaking time (ns)	55.5 ± 2.976	57 ± 5.291
Slow Shaper gain (mV/fC)	33.75 ± 1.909	33.81 ± 1.28

Slow Shaper peaking time (ns)	94.25 ± 3.284	93 ± 2.582

The comparison of two architectures of shaping amplifier was performed by observing the shaper output in both single-ended and pseudo-differential channels – the results are plotted in Figure 76 a) and b) respectively. If the transfer function of the filter contains complex conjugate poles, the pulse for the same peaking time is shorter and more symmetrical – the output returns to baseline around 13% faster (input charge 1.5 fC) and over 20% faster for larger input charge (e.g. 10 fC at the 0.8 fC threshold).

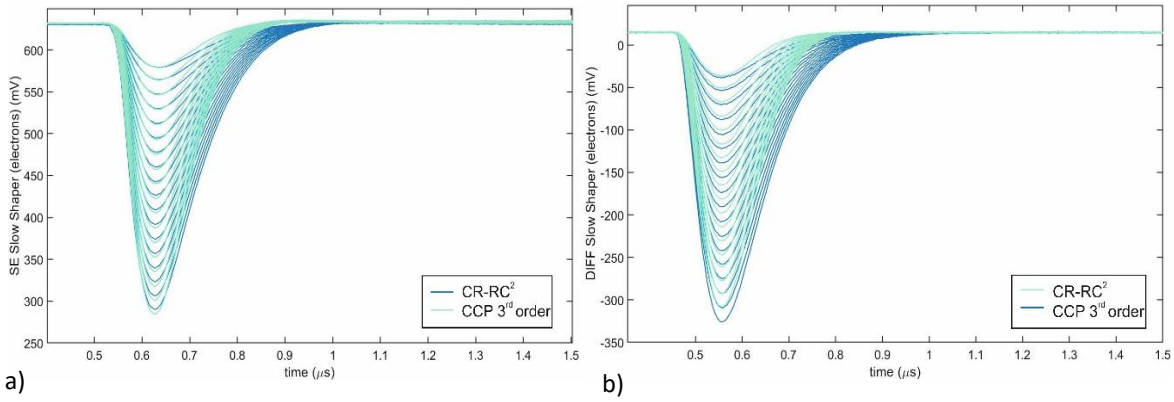


Figure 76 Measured output waveforms of the shapers with the switchable architectures for a) single-ended and b) differential channels.

The feedback resistance setting was investigated using MOS-based and Krummenacher circuit feedbacks. The effective resistance was estimated measuring the CSA discharge time constants (Figure 77 b) and Figure 78 b)) The MOS resistor value is configurable between 5 MΩ and 120 MΩ, as presented in Figure 77 a). The double-polarity leakage compensation circuit acts as an effective feedback resistance with values between 10 MΩ to 27 MΩ or 15 MΩ to 37 MΩ for positive and negative polarities of compensated current respectively (see Figure 78 a)). The measured value meets the requirements for correct operation in the charge-sensitive regime even if the sensor capacitances are large, leading to longer charge aggregation times.

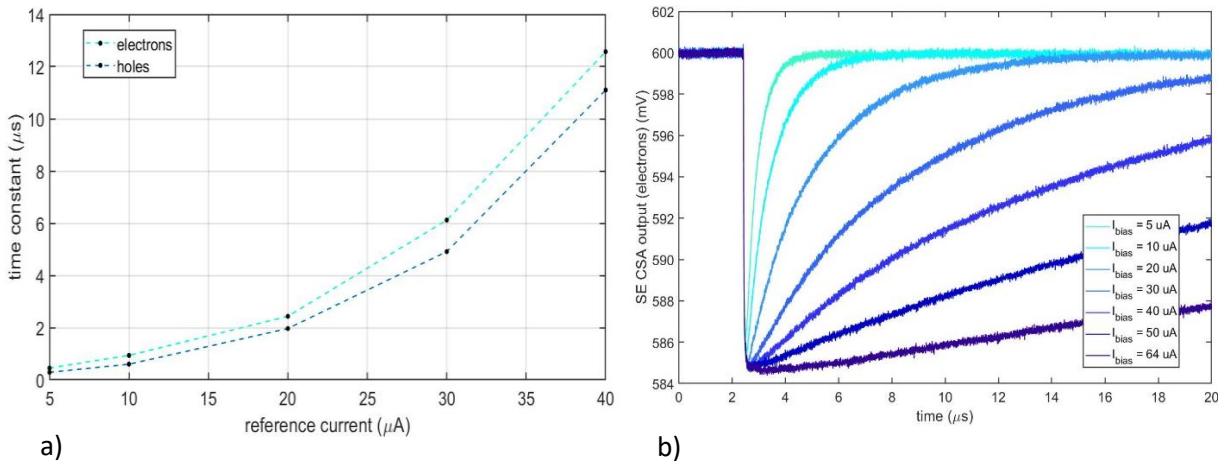


Figure 77 MOS transistor in the linear region as a feedback resistance; a) CSA discharge time constant; b) CSA output waveforms; different bias current setting.

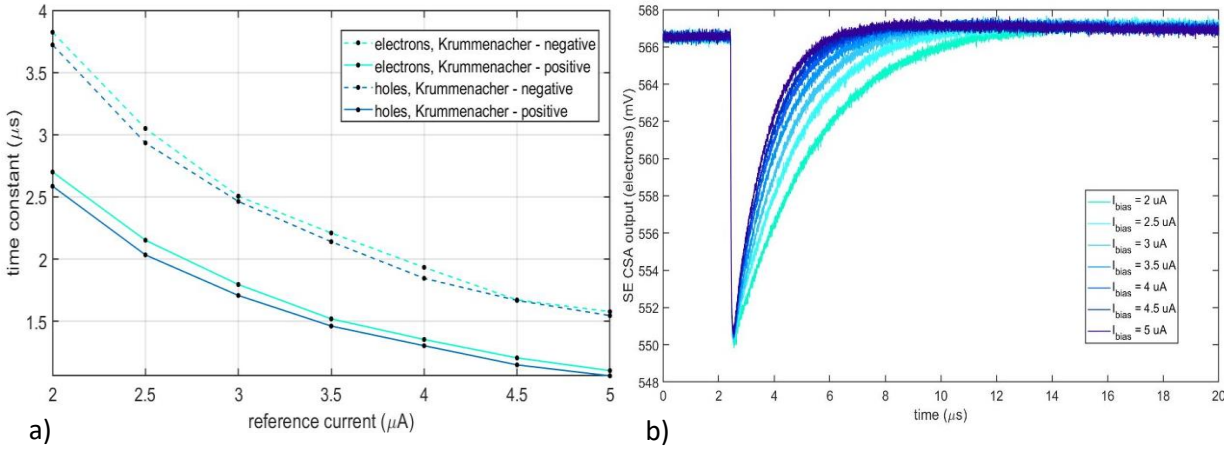


Figure 78 Double-polarity Krummenacher circuit as a feedback resistance; a) CSA discharge time constant, b) CSA output waveforms; depending on the bias current setting.

The shift of the CSA DC level and change of the effective feedback resistance due to leakage current flowing into/from the input node was investigated. The leakage current presence was injected or sourced to/from the channel input employing a Keithley 6487/E Picoammeter/ Voltage Source to be able to measure this current precisely. Both types of feedback were measured in the presence of currents of two polarities (Figure 79).

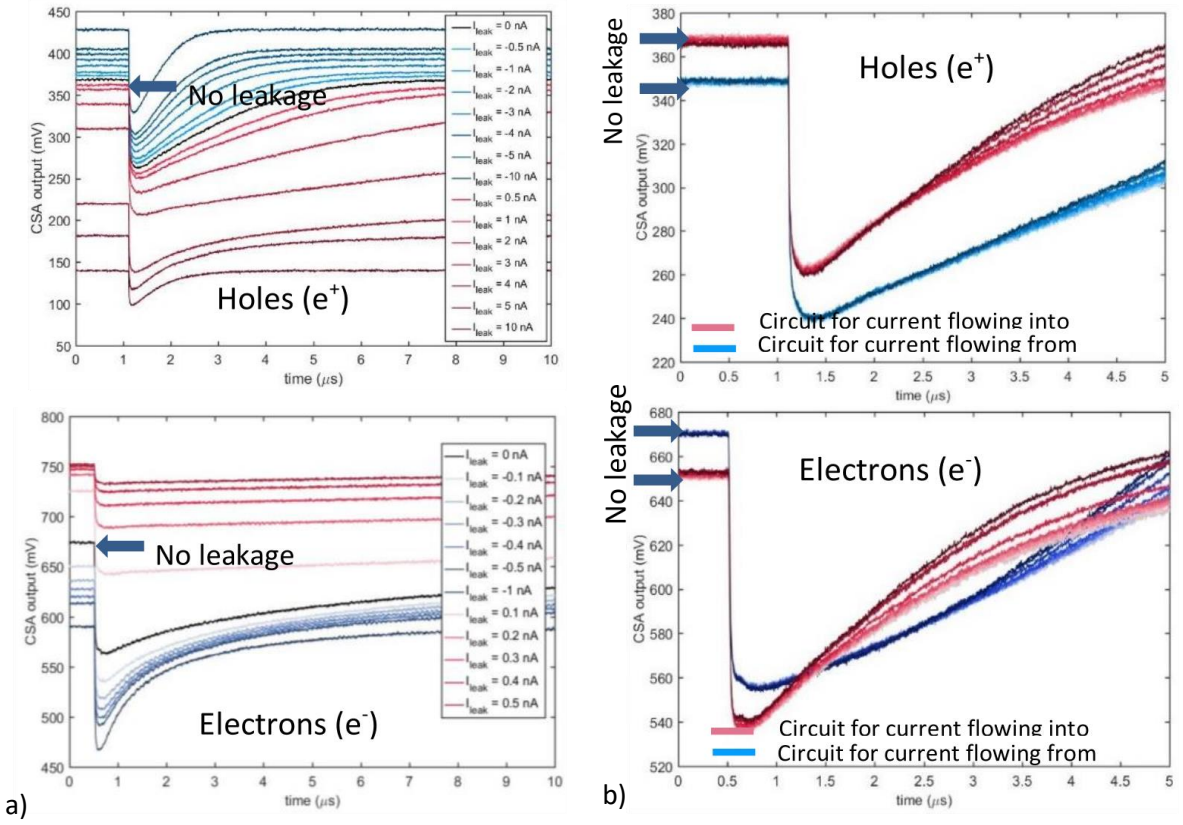


Figure 79 CSA output waveforms for a) MOS, b) Krummenacher feedback type with leakage up to 10nA (MOS) and −40 to 40nA (Krummenacher).

Figure 80 a) shows that the DC level shift in case of MOS transistor feedback is significant and varies from -50 mV up to 250 mV. For comparison, using a Krummenacher type feedback limits the shift to values

from -3 mV to 3 mV only (see Figure 80 b)). As a result, the leakage-current related relative feedback time constant change is low (1% - 5%) in case of Krummenacher-based circuit or very high (50% - 200%) in case of simple MOS transistor (Figure 81). Consequently, the effective feedback resistance follows the same behaviour. The Krummenacher type feedback can be particularly useful when the pulsed reset of the CSA feedback capacitor is employed for faster baseline restoration.

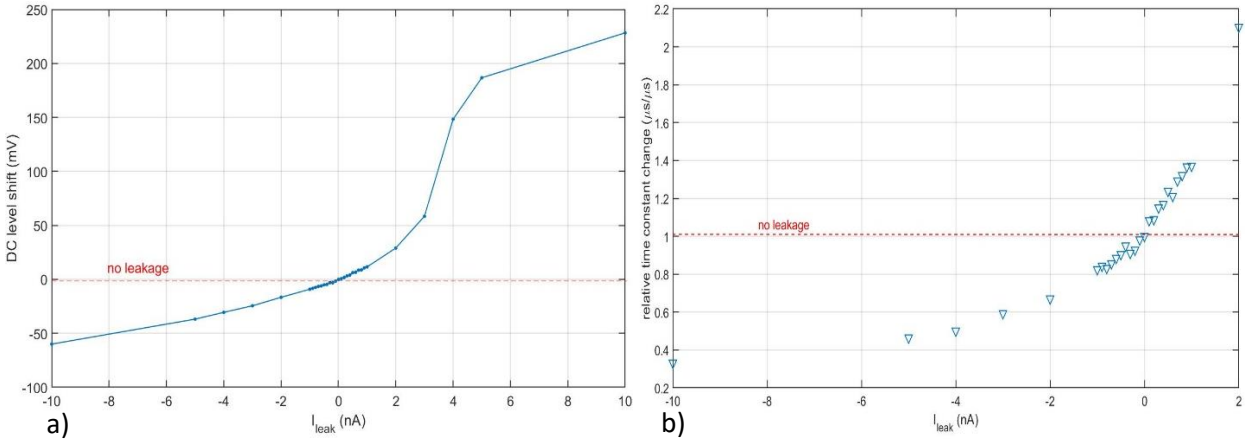


Figure 80 DC level shift using a) MOS feedback, b) double-polarity Krummenacher type feedback.

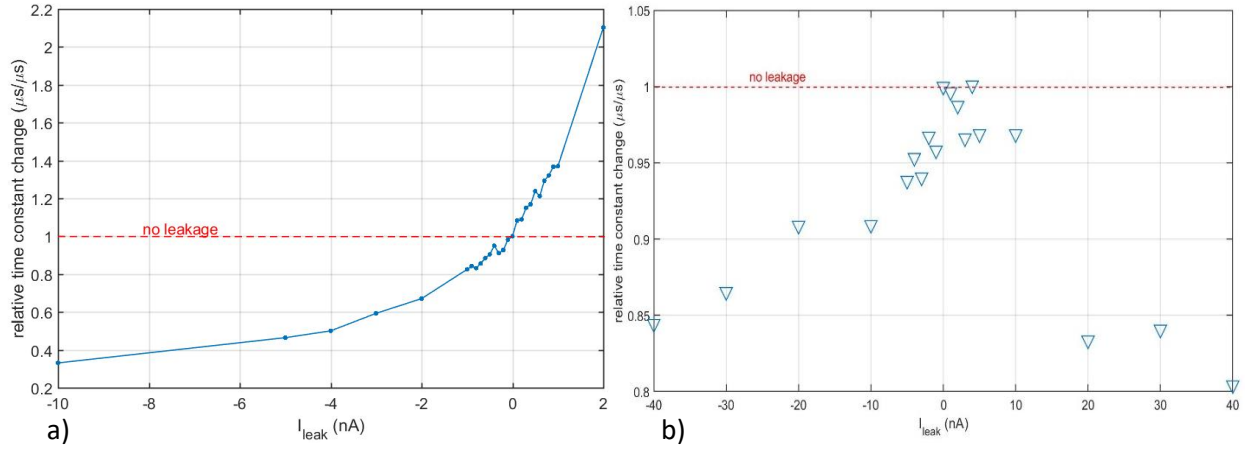


Figure 81 Relative time constant change for a) MOS feedback, b) double-polarity Krummenacher type feedback.

3.6. Noise measurements

Basic noise characterization was performed for all operation modes, without an input capacitance. Two scenarios were taken into account: using a clean power supply (Keithley 2231A-30-3 laboratory power supply device) and using a noisy DC-DC converter (Advanced Power Electronics APE1707M). The measured values of total input-referred noise, expressed in Equivalent Noise Charge (ENC), are shown in Figure 82. As can be seen, for clean power supply the noise performance is slightly better for the single-ended channels and the ENC values are around 300 e^- rms. If the power supply is noisy (high-frequency switching noise of the converter), the total output noise measured in the SE channels increases up to 1.6 times, whereas in the DIFF channels no significant change was observed. Differential charge processing proves useful in such applications, where the noise spectrum of the power supply and its interference are

not negligible, for example, if switching-based Low-Drop Out voltage regulators provide insufficient PSRR reduction and poor spectral purity of the supply voltage at the output. It is also a compact approach for applications, where the mitigation of interfering power supply noise is not possible on the system-level (for example by using ferrite-based filtering).

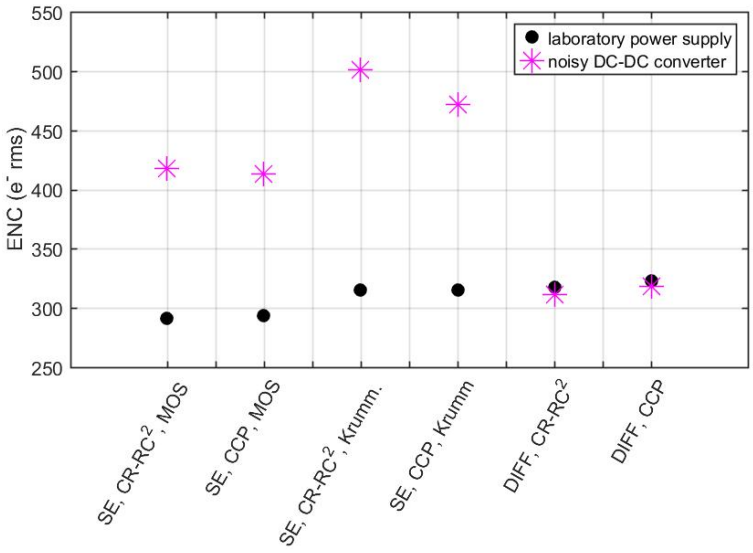


Figure 82 ENC for clean and noisy power supply for all operation modes and channel types.

The noise slopes were evaluated for both types of channels and all configurations using C0G dielectric type capacitances forming together with PCB traces a total input capacitance of values up to 14 fC mimicking the detector capacitance. The capacitors were used for simplicity to investigate the performance with a sensor without wire-bonding the device itself and without any additional effects caused for example by the detector leakage current (contributing to the overall output noise as well). The ENC values and noise slope for channels operated in the "holes" mode (for positive input charge) are higher, as visible in Figure 83 a). Average ENC slope values in the single-ended channels (for all operation modes) are equal to 15.2 e^- rms/pF and 16.36 e^- rms/pF for negative and positive polarity settings. For lower input capacitances, a better architecture of noise shaping seems to be semi-Gaussian CR-RC^2 one, whereas, with the increasing input capacitance, a filter with complex conjugate poles gives marginally lower ENC values (a detailed explanation of this effect is in chapter 4.9, confirmed by the measurements of another prototype IC). Measured noise slopes in the pseudo-differential channels are lower than in the single-ended and equal to 11.39 e^- rms/pF and 11.77 e^- rms/pF for electrons and holes respectively. No discrepancies between channels configured to process negative and positive charges were observed, so the difference noticed in the SE channels may be attributed to the PSC circuit.

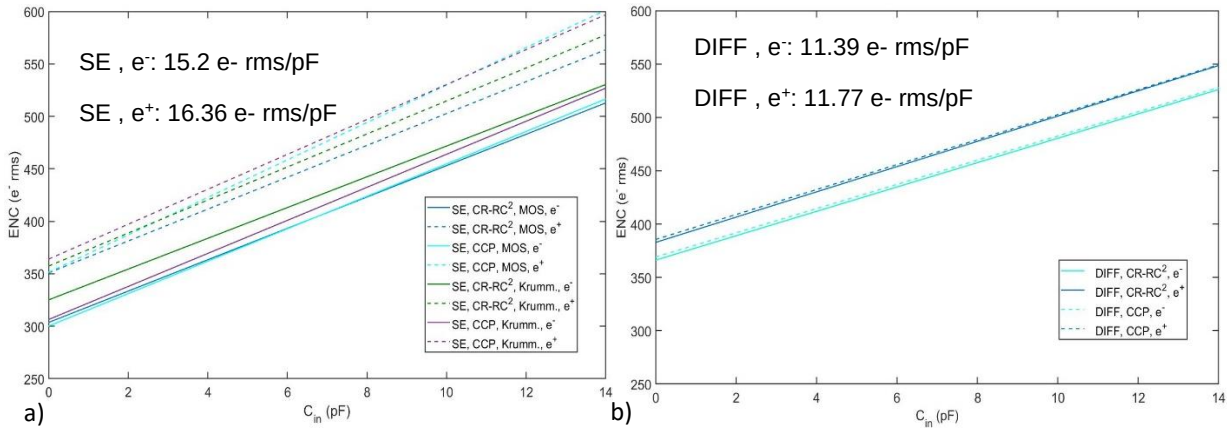


Figure 83 Noise slopes for various modes of operation - input capacitance up to 14 pF.

3.7. Summary

Presence of the leakage current in the detector readout systems may lead to several effects like DC level shift at the CSA output, the effective feedback resistance value change or, especially if the fast reset of the first stage is employed, fake hits and instability. The value and direction of this current flow in the input stage are unpredictable and dependent on the conditions (for example varying temperature), which makes the compensation a difficult task. The measurements of the SMX_mini ASIC prove that a double-polarity Krummenacher-type circuit for leakage compensation employed as the CSA feedback works well for both input charge and leakage current polarities reducing the baseline shift to ± 3mV (in comparison to -50 mV up to 250 mV in case of the simple MOS in the feedback). This solution provides high effective feedback resistance values (up to ~30 MΩ), that are constant even in the presence of excessive leakage (±40 nA). Combining this kind of feedback with pulsed reset can be a good solution if the high input hit rate is expected (up to 1 MHz can be achieved). In sophisticated detection systems, where usage of commercial ultra-low noise LDOs is not possible because of high radiation effects, and LC-filtering is not applicable due to magnetic field (tracking detection stations), a differential charge processing manner can be considered. The measured prototype pseudo-differential channels show good noise performance and power supply induced interference suppression showing only slight (few e^- rms) increase from the 320 e^- rms value measured for clean PS, whereas the ENC grows to over 500 e^- rms in the SE channels. The presented solution, employing charge sensitive amplifier replica, allows for ENC level reduction, increasing, however, the occupied area (0.144 mm^2 vs 0.057 mm^2 of the SE) but keeping reasonable power dissipation (around 10 mW). For more flexible noise level optimization without increasing the channel are (for various sources and dominant types of noise present in the system), switchable shaping amplifier architectures are implemented. Adding a possibility to change the shaper peaking time is also worth considering to adapt even better to the given conditions.

Chapter 4 PRINCSA ASIC, a prototype readout chip for silicon strip detectors

4.1. Overview of the chip architecture

The Programmable Readout with Improved Noise-performance Charge Sensitive Amplifier (PRINCSA) IC was designed based on the requirements for the Silicon Tracking System detection station (CBM experiment, FAIR, Darmstadt, Germany). In this detector system, ~300 μm thick, double-sided silicon strip sensors are used, with lengths ranging from 20 mm to 120 mm, each containing 1024, 58 μm-pitch strips on each of both sides [5], [41]. The ASIC, shown in Figure 84, was fabricated in Q4 2018 in a 180 nm CMOS process. It is built of 6 charge processing channels: three single-ended (SE) and three pseudo-differential (DIFF) channels, each of them dedicated for both negative and positive charges (electrons and holes). The IC comprises also biasing circuitry and an internal calibration circuit. Each channel contains Charge Sensitive Amplifier (CSA) followed by two AC-coupled shaping amplifiers (shapers) divided into two paths: a "fast path" with shaper with short peaking time (40 ns) for time measurements and "slow path" with a shaping amplifier with longer peaking times (from 90 ns to 250 ns) for amplitude (charge) measurements. The design uses a nominal power supply equal to 1.8 V (VDD), lower supply for the CSA main current source 1.2 V (VDDM) and an external 1.2 V reference voltage for a generation of biasing potentials and currents by a voltage-to-current converter and global Digital-to-Analog converters (DACs). The ASIC was designed employing common Radiation Hardening-by-Design (RHBD) techniques, for example, individual guard rings for each transistor, appropriate number and placement of the bulk contacts, enlarged critical transistors or use of the Enclosed Layout Transistors (ELT) for all NMOS devices for improved Total Ionizing Dose (TID) immunity [120].

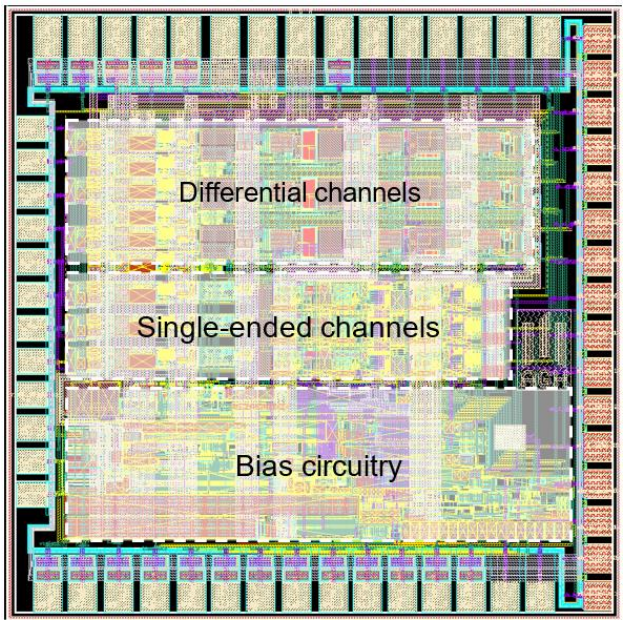


Figure 84 PRINCSA ASIC layout view.

PRINCSA features are programmable and the chip can operate in 24 different modes (Table 20) for the single-ended channels:

- three values of the slow shaper peaking time (90 / 180 / 250 ns),
- two architectures of slow pulse shaping amplifier: unipolar semi-Gaussian CR-RC^2 and with Complex Conjugate Poles (CCP) 3rd order,
- two types of CSA feedback capacitor discharge: with and without the leakage current compensation,
- two input charge polarities (different shapers reference voltage value).

The pseudo-differential channels can be operated in four modes (Table 20):

- two architectures of slow shaping amplifiers (the same as in the SE channels),
- two input charge polarities.

Additional features of the presented design are an internal calibration circuit and in-channel CSA bias filters. The circuitry for test pulses generation can be operated in two basic modes: generating the double pulses of different polarities or pseudo-single pulses of one selected polarity. Every channel of the PRINCSA ASIC is equipped with an internal filter for the CSA input transistor biasing potential filter to improve the Signal-to-Noise Ratio (SNR). The input transistor and its biasing circuit are very important for noise performance.

An internal shift register is used for the configuration of the PRINCSA ASIC biasing potentials and currents as well as for setting the switches to select the particular operation mode. There are 104 configuration bits (see Appendix A – PRINCSA configuration bitstream) divided into 8-bit memory cells based on Dual Interlocked Storage Cells (DICEs) for radiation immunity improvement [48].

Table 20 Summary of PRINCSA ASIC features and operational modes.

<table>
<tr><td colspan="2">Channel type</td><td colspan="2">Single-ended</td><td colspan="2">Pseudo-differential</td></tr>
<tr><td colspan="2"></td><td>Electrons</td><td>Holes</td><td>Electrons</td><td>Holes</td></tr>
<tr><td rowspan="3">CSA feedback type</td><td>MOS resistor</td><td colspan="2">✓</td><td colspan="2">✓</td></tr>
<tr><td rowspan="2">Krummenacher</td><td colspan="2">For negative leakage</td><td colspan="2" rowspan="2">×</td></tr>
<tr><td colspan="2">For positive leakage</td></tr>
<tr><td colspan="2">Fast Shaper</td><td colspan="2">✓</td><td colspan="2">✓</td></tr>
<tr><td rowspan="2">Slow Shaper architecture</td><td>CR-RC^2</td><td colspan="2">✓</td><td colspan="2">✓</td></tr>
<tr><td>CCP 3rd order</td><td colspan="2">✓</td><td colspan="2">✓</td></tr>
<tr><td colspan="2">Polarity selection</td><td>Slow shaper – V_{ref} low
Fast shaper - V_{ref} high</td><td>Slow shaper – V_{ref} high
Fast shaper - V_{ref} low</td><td colspan="2">Slow shaper - switch at the shaper input
Fast shaper - switch between 1st and 2nd shaper stage</td></tr>
<tr><td colspan="2">Slow Shaper peaking time (ns)</td><td colspan="2">90 / 180 / 250 ns</td><td colspan="2">90 ns</td></tr>
<tr><td colspan="2">Fast shaper peaking time (ns)</td><td colspan="2">40 ns</td><td colspan="2">40 ns</td></tr>
<tr><td colspan="2">Shaper core GBW</td><td colspan="2">1.51GHz</td><td colspan="2">1.91 GHz</td></tr>
<tr><td colspan="2">Internal CSA bias filtering</td><td colspan="2">✓</td><td colspan="2">✓</td></tr>
<tr><td colspan="2" rowspan="3">Calibration</td><td colspan="4">External calibration pulse via pad</td></tr>
<tr><td colspan="4">Internal calibration pulse – both charge polarities (square wave)</td></tr>
<tr><td colspan="4">Internal calibration pulse – pseudo-single charge polarity (slow discharge)</td></tr>
<tr><td colspan="2">Area</td><td colspan="2">0,093μm^2</td><td colspan="2">0.146 μm^2</td></tr>
<tr><td colspan="2">Power consumption</td><td colspan="2">8.7 mW</td><td colspan="2">13.7 mW</td></tr>
<tr><td colspan="2">ENC (clean PS, internal filtering, no input capacitance)</td><td>278.2 e$^-$ rms</td><td>275.9 e$^-$ rms</td><td>309 e$^-$ rms</td><td>327.6 e$^-$ rms</td></tr>
<tr><td colspan="2">VDDM-to-output gain (post-layout for e$^-$)
@ 50 Hz
@ 100 Hz
@ 10 kHz
@ 100 kHz</td><td colspan="2">
-108.30 dB
-100.40 dB
-23.68 dB
6.40 dB</td><td colspan="2">
-132.70 dB
-120.70 dB
-40.87 dB
-8.88 dB</td></tr>
</table>

4.2. Single-ended channels architecture

The single-ended channel architecture is presented in Figure 85. The CSA core amplifier architecture is based on a direct cascode with split biasing [33] and its gain-bandwidth (GBW) product equals 9.1 GHz [30], [99], [107]. The input device is an NMOS transistor, providing lower white noise than a PMOS for the same transconductance (because making the NMOS transistor work in weak inversion region is easier than in the PMOS case and this operation region provides lower inversion coefficient for the thermal noise contribution [33], [76]), with an aspect ratio equal to W/L = 2.5 mm/ 320 nm and it is biased with nominal current equal to 2 mA supplied from the 1.2V power supply domain. The sizing and bias current of the large input transistor were optimized to match the input capacitance of the experiment target detectors' and application-specific cables' capacitances, forming a total input capacitance of value up to 30 pF [66], [122]. A 100 fF capacitor is used as the CSA feedback capacitance and the feedback resistance is configurable: a PMOS transistor working in the linear region (R_{fb} in a range from 1 MΩ to 6 GΩ, nominal 25 MΩ) or a double polarity Krummenacher circuit [109], [111] to compensate any leakage current present in the system

(R_{fb} in a range from 3 MΩ to 120 MΩ, nominal 28 MΩ – see Chapter 2.2). The leakage current compensation feedback combined with a digitally triggered reset is a novel solution used in this design (and in SMX_mini ASIC) for shorter baseline restoration time, necessary to process sub MHz input hit rates. The CSA is reset by a small (tens of kΩ) resistance connected in parallel with the feedback circuit (which resistance is around two orders of magnitude larger), through an externally controlled switch. Without proper compensation of the leakage current (stemming from for example the sensor or the ESD protection circuit), the big difference between feedback and reset resistances may lead to problems, like fake hits [75], described in 1.5.4.

The channel area is 1119 µm × 83 µm (Figure 86) and the power dissipation equal to 8.7 mW.

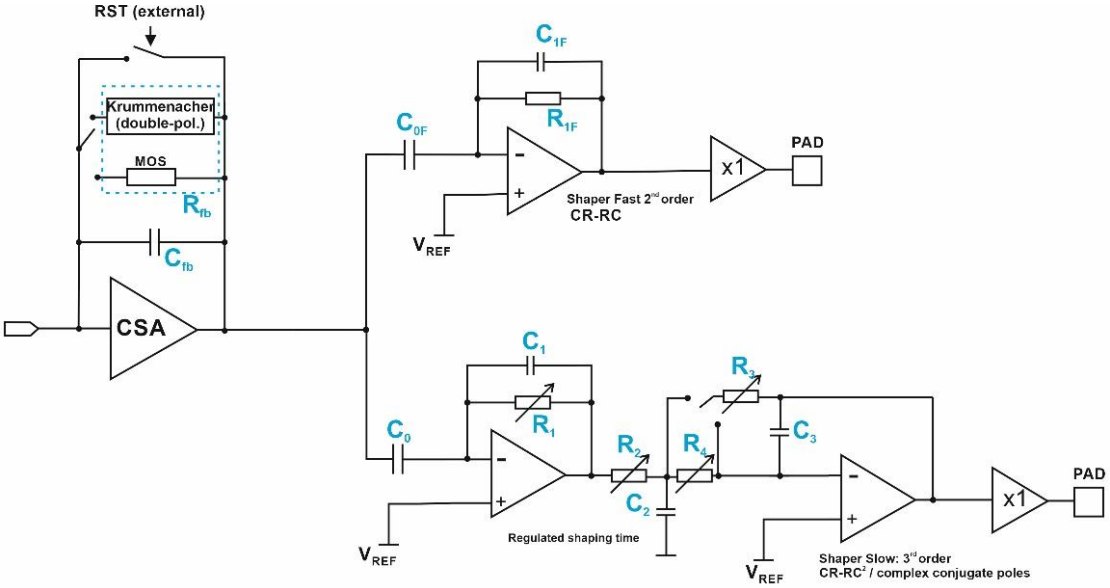


Figure 85 Single-ended channel schematic.

Figure 86 Single-ended channel - layout view

Both shaping amplifiers are designed using a differential folded cascode Operational Transconductance Amplifier (OTA) with diode-connected load, as a core amplifier (Figure 87). This circuit GBW equals 1.51 GHz and it employs PMOS transistors (W/L = 400/0.4 µm) as input devices for more effective usage of power supply range for the allowed output swing. The input pair is biased with nominal current equal to 400 µA (this value can be regulated from 200 µA to 800 µA by internal DACs) and the load cascodes are biased using 200 µA nominally (regulated by separate DACs for NMOS and PMOS cascode from 100 µA to 400 µA).

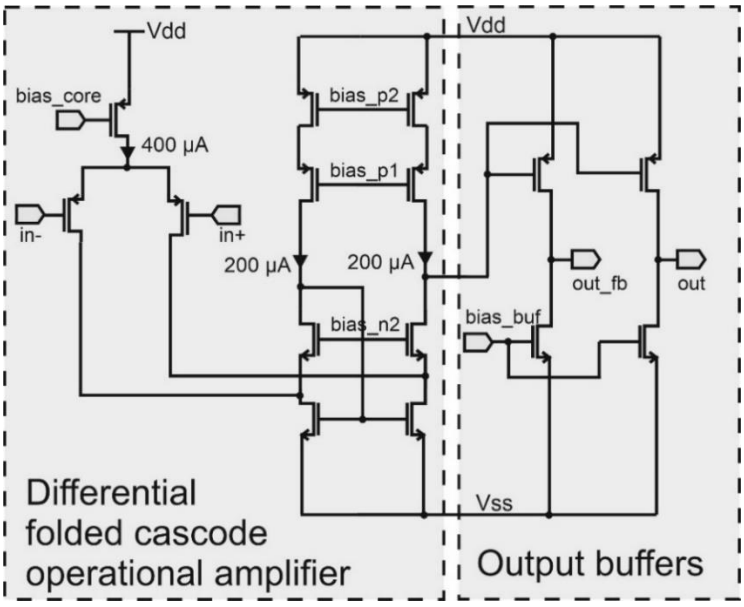
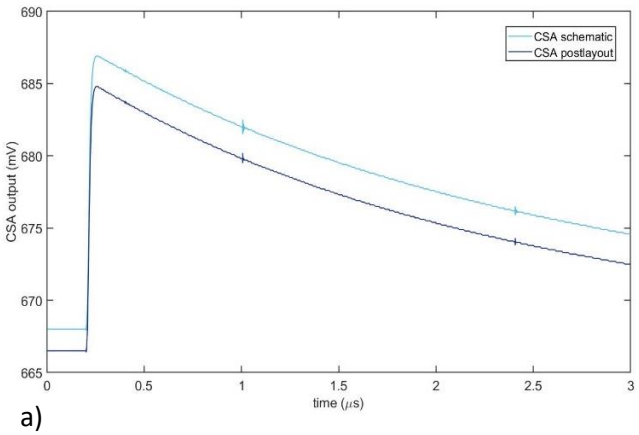


Figure 87 Folded cascode OTA used as shapers core amplifier - schematic.

The fast shaping amplifier architecture is a CR-RC (semi-Gaussian) filter configuration and its peaking time equals 40 ns. The slow shaper poles constellation (real poles CR-RC^2 and complex conjugate poles for the Ohkawa architecture [113]) and the peaking time (90 ns, 180 ns or 250 ns) are selectable using resistors, capacitors and switches as presented in Figure 85. The filter architecture is changed employing only a few switches and a special selection of passive components, that are built with small identical components (this improves also the matching). Instead of using polarity switching or reversing, the shapers dynamic range is regulated by changing the reference voltage. The reference is generated by two internal 6-bit DACs and can be selected within the range from 600 mV to 1.2 V. This allows to obtain linear charge processing characteristic for charges up to 15 fC both for electrons and holes.

Exemplary simulated waveforms at each stage output acquired at schematic and post-layout levels are presented in Figure 88. The simulations were performed for electrons (negative polarity), MOS in the CSA feedback and CR-RC^2 slow shaping amplifier configuration. Good agreement between schematic and post-layout simulations is visible.



a)

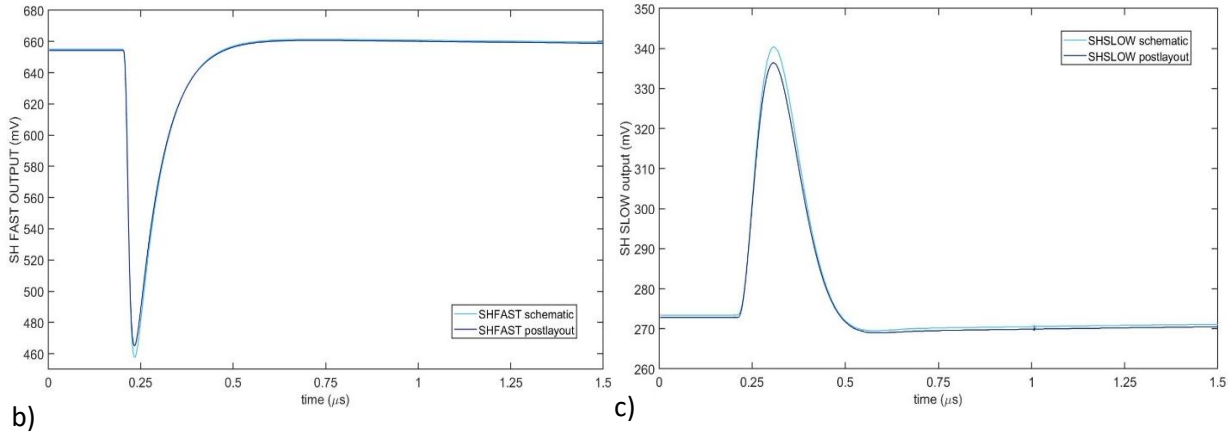


Figure 88 Simulated output waveforms (schematic and post-layout) for the single-ended channel, electrons, no leakage compensation, semi-Gaussian shaping (slow path).

4.3. Pseudo-differential channels architecture

The CSA core used in the pseudo-differential channels for both main CSA and the replica is based on the same architecture as in the single-ended channels. As the feedback capacitor discharging resistance, a MOS transistor is used and it is also combined with fast reset, as in the SE channels. Main CSA input is connected to a pad for wire-bonding to connect a sensor. The replica of the charge amplifier is used to employ differential charge processing in the following stages. No scaling of the replica is applied for the most effective power supply interference subtraction and the Power Supply Rejection Ratio (PSRR) improvement in the full frequency range [116], [123].

The fast and slow shapers core amplifier is based on a fully differential folded-cascode with common-mode feedback (CMFB), which is described in details in section 3.3. The input of the core amplifier is PMOS transistors pair with aspect ratio equal to W/L = 400/0.4 µm biased with 400 µA nominal current (regulated from 200 µA to 800 µA by an internal 3-bit DAC). The simulated GBW equals 1.91 GHz. The output is fully differential and each of the output load branches is biased with the half of the input pair current (see section 3.3). In this design, compared to the SMX_mini, the single-ended shapers core amplifier is replaced with OTA, built using identical transistors (in terms of type and sizes) and biasing currents as the core amplifier in the pseudo-differential channel (the difference is in the load, making the output single-ended or differential). This approach enables comparison of the noise performance between these two kinds of charge processing, limiting the discrepancies caused by different circuit architecture.

To allow for two input charge polarities processing, reversing of the signal polarity is implemented utilizing switches integrated into fast and slow shapers architecture (Figure 89). The reference voltage is kept on a constant level, equal to half of the power supply voltage, for proper operation of the CMFB circuit (and can be regulated through a 6-bit internal DAC for stability adjustment). The slow shaper architecture is configurable by the selection of resistors and switches (CR-RC^2 and CCP 3rd order configuration). The values of the passive components used in the shaper feedback are identical for both channel types. Due to

area limitations and for simplicity, the peaking time switching is implemented only in the single-ended channels.

The differential channel occupies an area of 1213 µm x 120 µm (Figure 90) and dissipates power equal to 13.7 mW for the default settings.

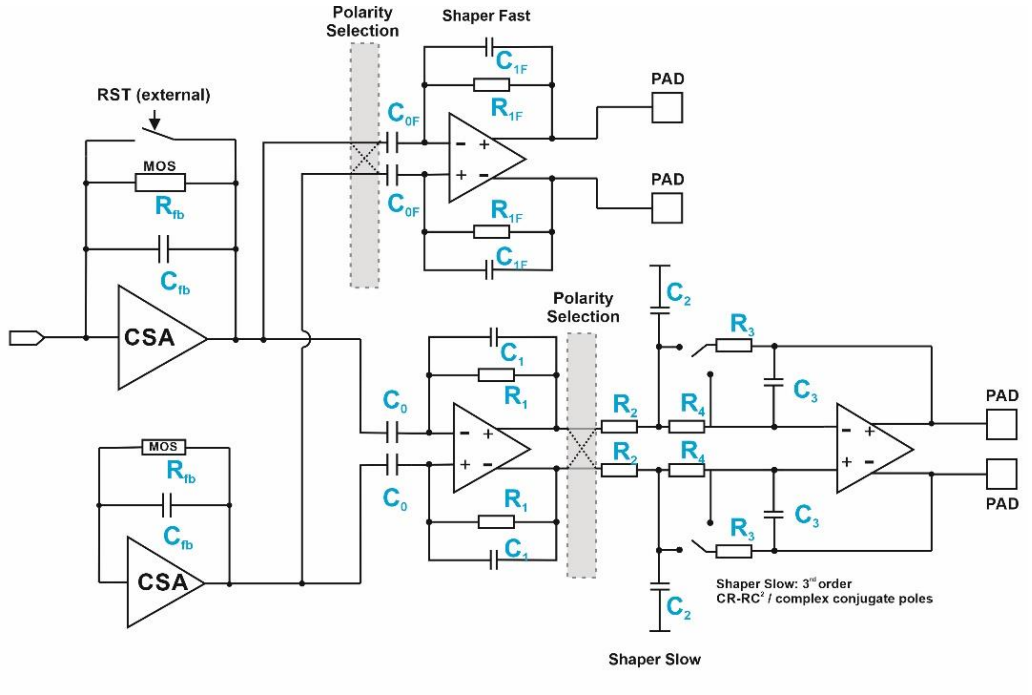


Figure 89 Differential channel schematic

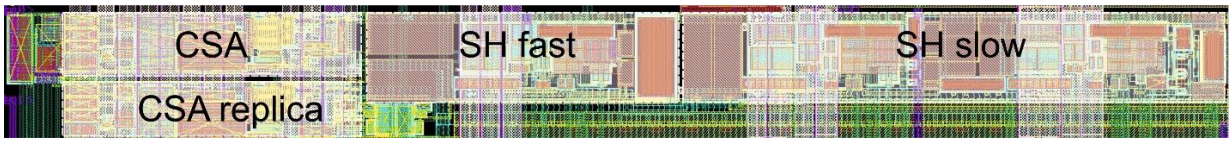
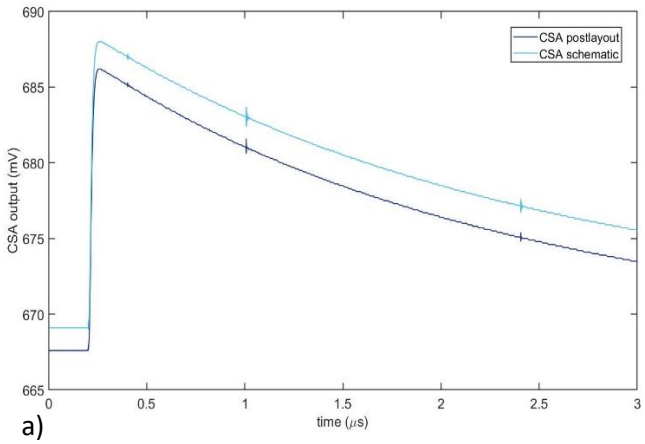


Figure 90 Differential channel - layout view

Simulated output waveforms acquired at the output of each charge processing chain stage are presented in Figure 91. The slow shaping amplifier was configured in the CR-RC^2 mode. The shapers pulse polarity depends on the differential output signals subtraction order.



a)

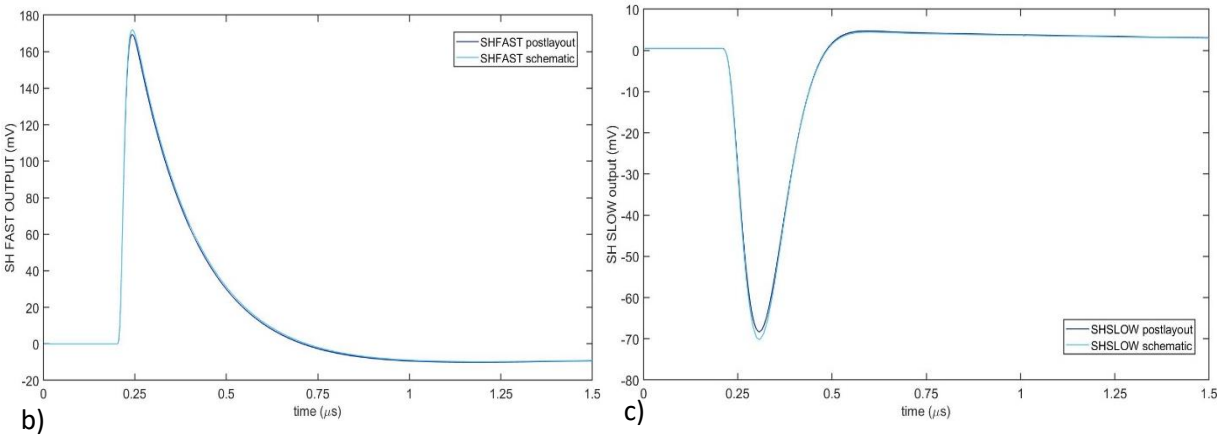


Figure 91 Simulated output waveforms (schematic and post-layout) for pseudo-differential channel, electrons, no leakage compensation, semi-Gaussian shaping (slow path).

4.4. Charge Sensitive Amplifier bias decoupling

The VDDM-to-output transfer function of the single-ended and the pseudo-differential channels simulated (on the schematic and post-layout level) for both types of shaping used in the design is presented in Figure 92. A discrepancy between two types of channels can be seen in particular for lower frequencies. It can be concluded, that differential charge processing diminishes the power supply induced interference (up to 40 dB better rejection for low frequencies – tens of Hz, around 15 dB better for frequencies around 100 kHz - Table 20). This is particularly important in case of the power supply domain, to which the main current source of the CSA is connected, providing high current biasing the input transistor (VDDM domain).

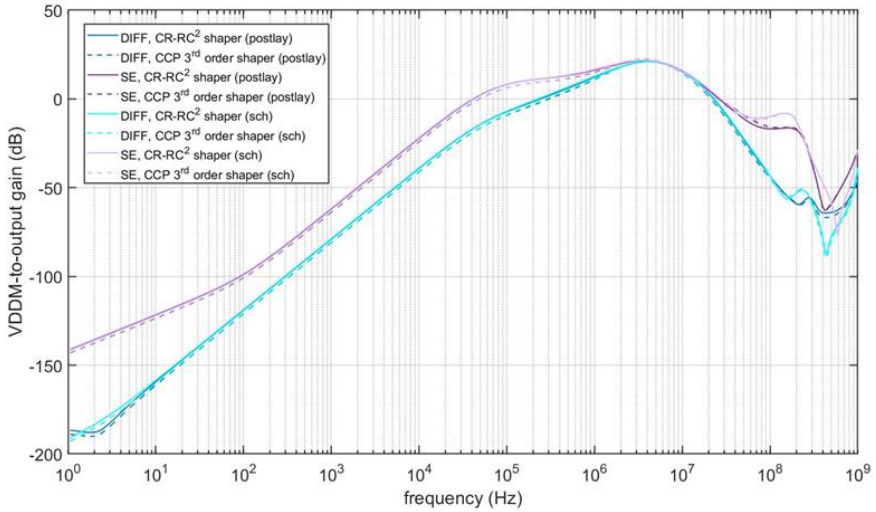


Figure 92 Simulated transfer function VDDM power supply-to-output for single-ended and pseudo-differential channels (filtering not applied).

To further decrease the power supply interference coupling through the 1.2 V VDDM domain, the CSA biasing potential filter, shown in Figure 93, is included in every channel. The filter is built of a MOS-based capacitor (C_f = 10 pF) and resistor with externally regulated gate voltage (R_f = 5.6 MΩ for a V_g nominal value equal to 530 mV), that set the filter cut-off frequency at 28.42 kHz. When the filter is

enabled, the global reference current value is low (ranging from 0 to 800 µA, and the default value is equal to 400 µA), saving power and area consumption. The global reference is scaled up (from 0 to 4 mA, default value 2 mA) in every channel, while the high noise contribution from devices scaled in such way is filtered locally. With no filter, the high global reference current (from 0 to 8 mA, default value 4 mA) is scaled down locally in the channels (from 0 mA to 4 mA, default value 2 mA), to prevent from multiplying the reference noise.

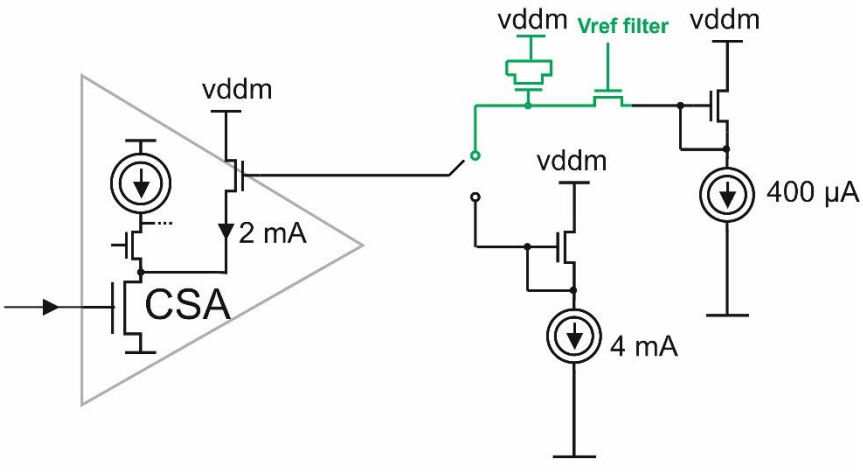


Figure 93 Schematic representation of the internal CSA main bias filtration.

4.5. Calibration circuit

The verification of the charge processing chain functionality requires injecting known charge into the channel input and acquiring waveforms at the output of each stage. In this design, the charge can be injected using a test capacitor implemented inside each channel and applying a voltage step to it [17]. The calibration pulse can be generated externally and applied to a pad or by employing an internal calibration circuit. The internal test capacitor value used in this design is 100 fF, so the 10 mV of voltage step results in approximately 1 fC (6240 e^-) of charge injected into the channel.

The built-in calibration circuit can be used in two operation modes (Table 21): a train of double polarity and pseudo-single polarity pulses generation. The first mode, illustrated in Figure 94, generates a square-wave signal, whereas, in the second one (Figure 95), a waveform with fast leading- and the slow trailing edge is obtained – the simulated behaviour is shown in Figure 96. In the pseudo-single polarity, mode fast rising or falling edge depending on the selected polarity, is achieved by quick charging a capacitor, which is then slowly discharged through a current source to provide controllable discharge time. The duration of the discharge is programmable by a 3-bit DAC and can be set from hundreds of nanoseconds up to 15 µs. The amount of charges injected to the amplifier input at different edges is the same, but making the slope slower in relation to the CSA time constant, results in a negligible signal at the output. The pseudo-single polarity mode is useful if the characterization of the front-end for one selected

input charge polarity is required. The amplitude (and the amount of charge) in both modes is set by an 8-bit DAC (resolution approximately 0.06 fC/LSB).

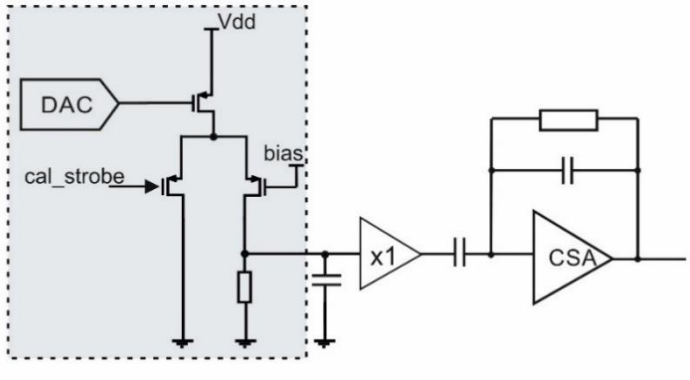


Figure 94 Calibration circuit double charge generation mode - schematic.

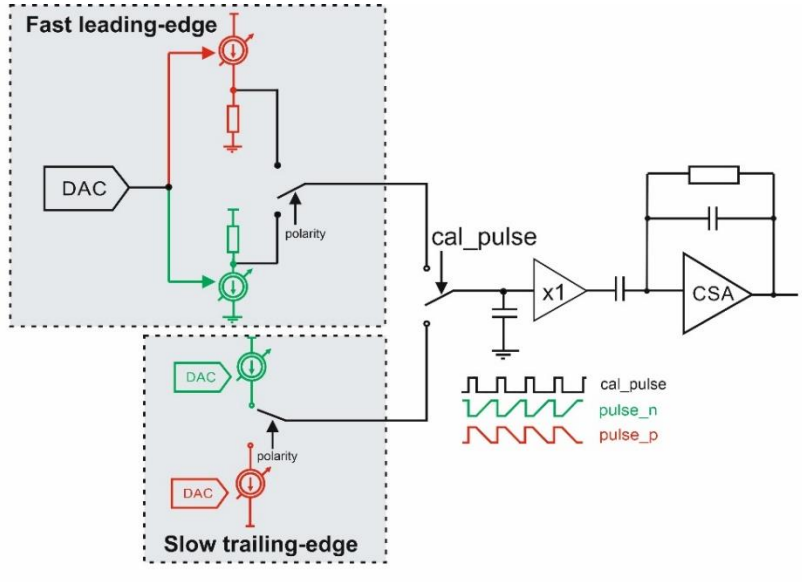


Figure 95 Calibration circuit pseudo-single charge generation mode - schematic.

Table 21 Calibration circuit operational modes.

	Double polarity charge	**Pseudo-single polarity charge**
Charge	Electrons and holes (on each slope)	Electrons OR holes (very slow injection of opposite polarity due to the slope difference)
Amplitude	8-bit DAC, 1-15 fC	8-bit DAC, 1-15 fC
Discharge slope	-	2.8 µs (current 14.39 µA) to 15 µs (current 1.64 µA)
Trigger	**cal_strobe** (cal_pulse high)	**cal_pulse** (cal_strobe high)
Frequency of charge injection	Double the **cal_strobe** rate	The **cal_pulse** rate

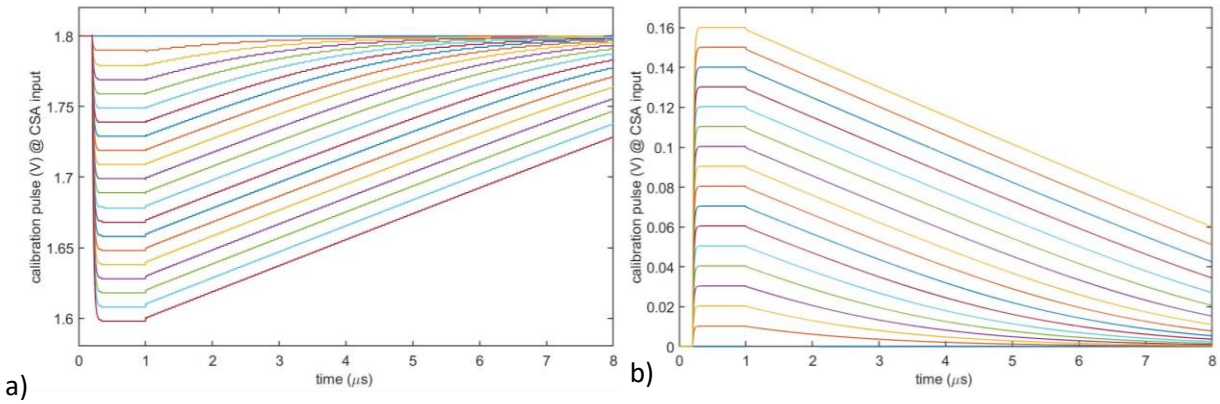


Figure 96 Simulated calibration circuit output waveforms for uni-polar charge generation - various amplitudes (charges). (a) negative charge, (b) positive charge.

4.6. Test setup and software

Measurements and characterization of the fabricated integrated circuits (Figure 97) were taken in all ASIC's operation modes. The integrated circuits were assembled using a wire-bonding technique on dedicated 4-layer Printed Circuit Boards (PCBs). The PCB has a size of 137 mm x 105 mm, and it includes the following components:

- gold plated field for wire-bonding of the IC,
- 100 nF, 0402 SMD decoupling capacitors,
- coaxial connectors (SMA) for each test signal from every channel (two connectors for pseudo-differential channels to enable differential signal acquisition),
- test points for the most important internal biasing potentials,
- footprints for external resistors and trimming potentiometers (if necessary to apply the bias externally),
- power connectors for both power supply domains (VDD and VDDM),
- two sockets for mezzanine boards designed for tests employing various DC-DC converter modules instead of connecting laboratory power supply,
- gold plated area for the semiconductor detector wire-bonding
- 68-pin PCB expansion connector for external detector module.

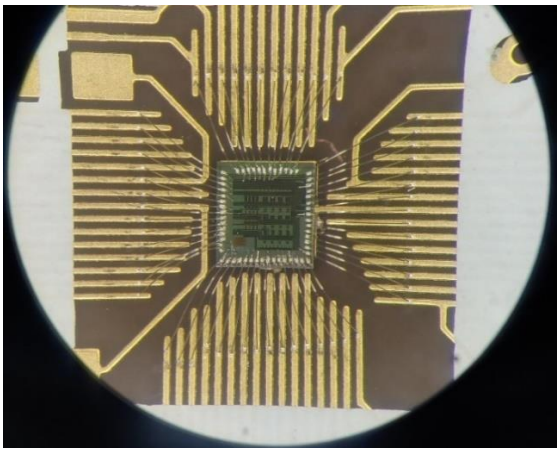


Figure 97 PRINCSA ASIC on the test PCB.

A custom test-software was prepared using the LabVIEW graphical programming environment to perform configuration of the bias voltages and currents (through the internal DACs steering) and to communicate with the measurement equipment. The test-system (Figure 98) composed of measurement devices and test-software was integrated employing National Instruments PXI platform. A Tektronix DPO 7354C oscilloscope equipped with differential 3.5 GHz active probes ($C_{in} \leq 0.8$ pF) was employed for data acquisition. The external pulses (for calibration using both internal calibration circuit and external pulses with configurable amplitude) were provided by a Tektronix AFG 3251C arbitrary waveform generator ($\tau_r = 2.5$ ns).

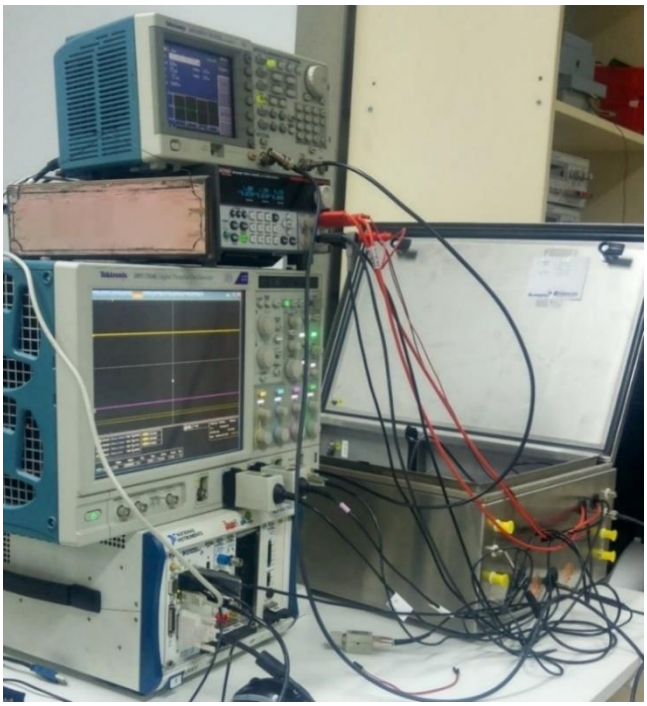


Figure 98 PRINCSA chip test setup at AGH.

The test software designed using LabVIEW environment (Figure 99) is based on two-thread architecture. It enables communication with the test equipment (oscilloscope, waveform generator) via Ethernet using the VISA Application Programming Interface (API). The test application initializes communication with oscilloscope and generator and configures these devices for measurements. The software, through a multifunction I/O device (NI USB-6351), generates signals to control the internal shift register for the biasing DACs programming and setting the ASIC internal potentials and currents. The shift register bitstream contains also bits for selection of the operation mode features. The basic functionalities of the test software are:

- ASIC configuration in the basic, default mode (automatically),
- ASIC configuration by writing a single value to the ASIC's shift register,
- calibration of the IC using internal calibration circuit in both double polarity and pseudo-single polarity modes (switching the polarity, sweeping the pulse amplitude),
- calibration of the IC using external calibration pulse – amplitude sweep using the AFG,
- taking a single measurement for a special set of parameters/conditions,
- acquiring the waveforms from the oscilloscope,
- saving the waveforms to .csv file.

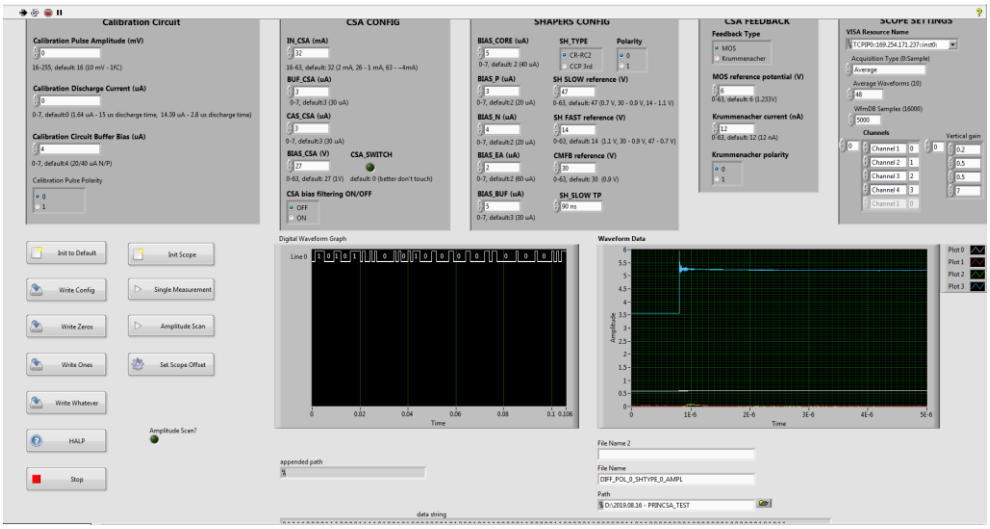


Figure 99 Test software - user interface.

4.7. Performance verification

The results of functional verification proved that the chip operation is correct and consistent with the simulations. The examples of waveforms acquired at each stage of the charge processing channel for positive input charge polarity are presented in Figure 100. The shape of the waveforms confirms that the charge processing chain works as expected. To verify that, the acquired data were used for further processing to evaluate parameters of single-ended and pseudo-differential channels for all operation modes.

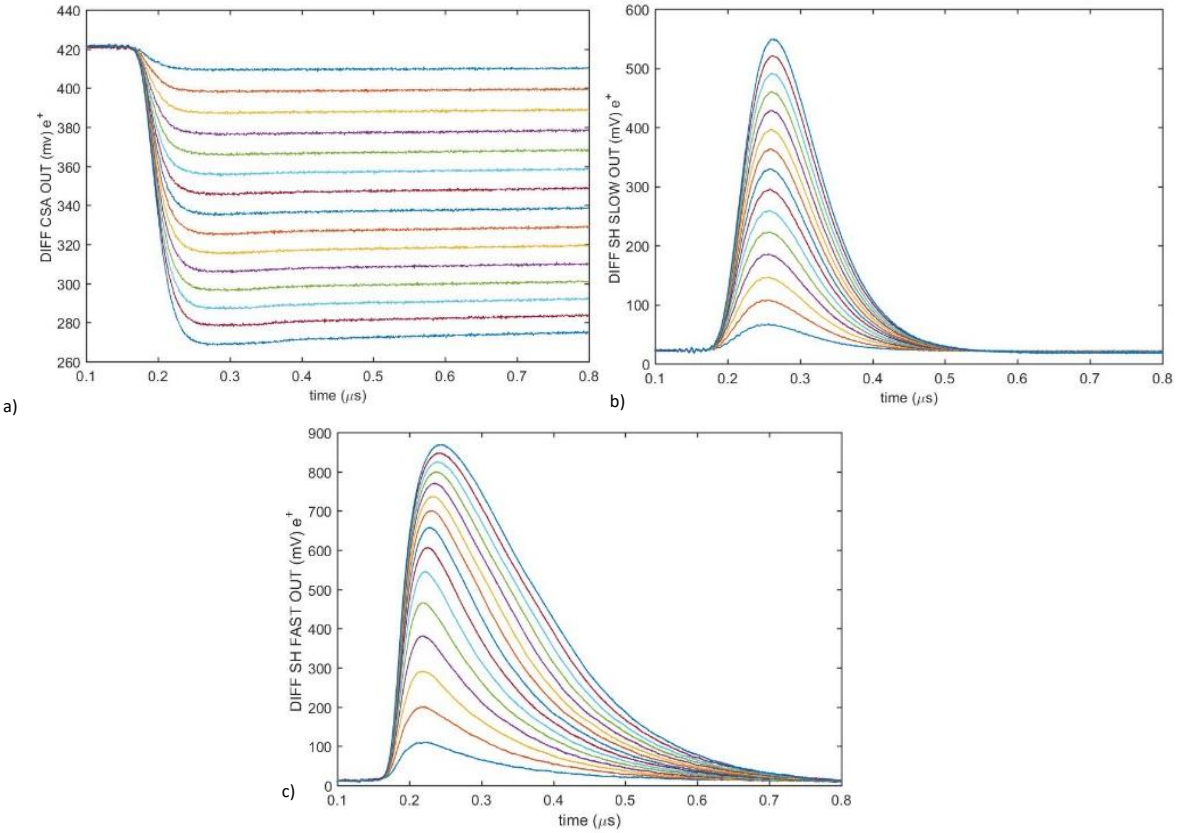


Figure 100 Output waveforms for charges up to 15 fC for the differential channel a) CSA, b) Slow Shaper, c) Fast Shaper. Qin from 1 to 15 fC, step 1 fC.

The gain of each stage in all operation modes and for both channel types was evaluated. It can be seen that for the CSA, the gain is uniform for all settings, as shown in Figure 101 a). Some differences can be seen between slow shaper transfer function in single-ended and pseudo-differential channels (Figure 101 b)). The gain measured for the fast shaper is not uniform in all operation modes (Figure 101 c)) and no trends are visible – it was observed, that the gain depends strictly on the setting of the core amplifier biasing currents. The good characteristics linearity is kept for the input charges up to 15 fC for CSA and slow shaping amplifier, whereas fast shaper transfer function is linear for charges up to 7 fC. The fast path provides fast rising edge (shorter peaking time) and higher gain (around 70 mV/fC) for the low-time walk and low-jitter incoming hits time measurements.

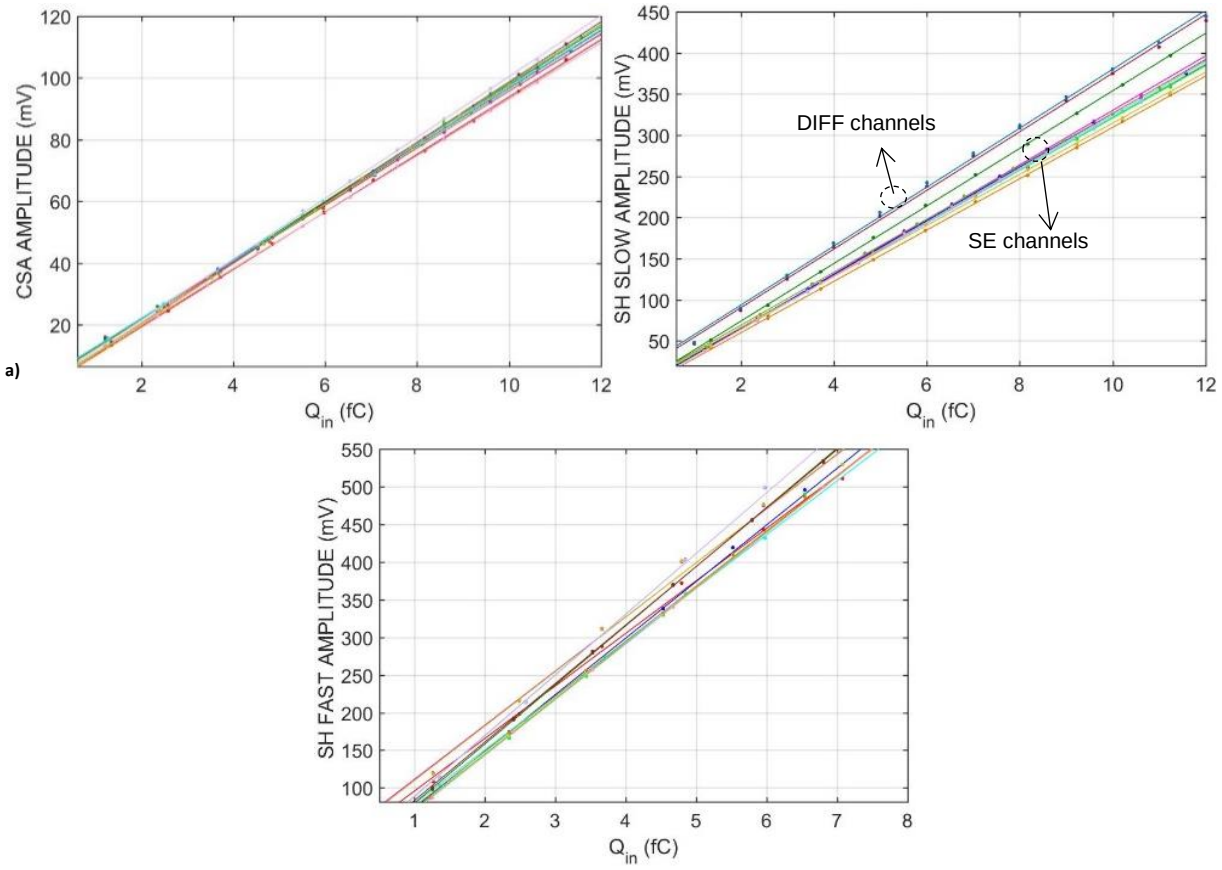


Figure 101 Transfer function of a) CSA, b) Slow Shaper, c) Fast Shaper for various types of operation and two types of channels.

Table 22 summarizes the basic performance of the PRINCSA ASIC. The comparison of the mean values and standard deviations of gain and peaking time for both types of channels averaged between various operation modes is presented. The INL of the CSA, Slow and Fast Shapers transfer function equals 0.22-1%, 0.37-1.08% and 0.37-2.37% respectively (the minimum and maximum value depending on the configuration and charge processing manner).

Table 22 Summary of measured charge processing characteristics

Channel type	Single-ended	Differential
CSA average gain (mV/fC)	9.323 ± 0.134	9.723 ± 0.08
CSA average peaking time (ns)	49.905 ± 4.231	57.166 ± 4.759
Slow Shaper average gain (mV/fC)	32.123 ± 0.716	33.63 ± 1.139
Slow Shaper average peaking time (ns)	95.033 ± 2.261	94.75 ± 3.623
Fast Shaper average gain (mV/fC)	72.85 ± 1.735	79.443 ± 1.518
Fast Shaper average peaking time (ns)	48.203 ± 4.103	58.545 ± 6.064

A comparison between two types of slow pulse shaping is shown in Figure 102 a). The waveforms presented below were acquired at the SE channel output for positive charges from 1 to 15 fC. As expected [33], complex conjugate poles in the filter transfer function give shorter and more symmetrical pulses for the same shaper order (27-28% faster return to the baseline). This feature is beneficial for the noise performance and the maximum processed hit frequency without a pile-up effect. The possibility to set the

peaking time to one of the three possible values was also verified – the results are plotted in Figure 102 b). No significant differences between the peaking times for architectures with real and complex conjugate poles were observed and the values are consistent with the simulations.

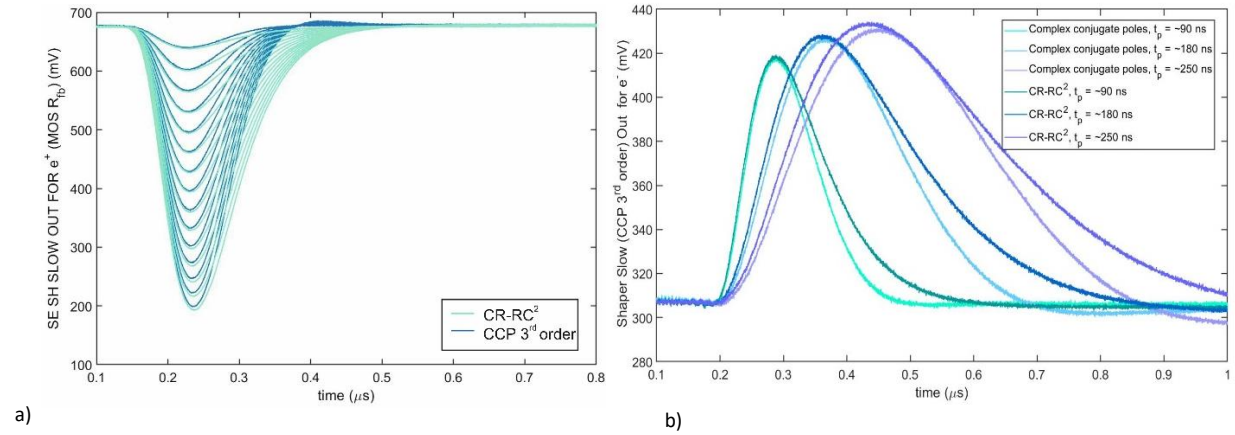


Figure 102 Slow shaper output waveforms a) charges up to 15 fC, two architectures comparison, b) three different values of peaking time (90, 180 and 250 ns).

4.8. Calibration of channels – calibration circuit verification

Two modes of calibration circuit operation were verified by acquiring waveforms generated at the CSA input by probing dedicated pad of the ASIC. First, standard mode enabling generation of both polarity pulses (electrons and holes) was tested for amplitudes from 10 mV to 150 mV (1 fC to 15 fC) and the resulting waveforms are presented in Figure 103.

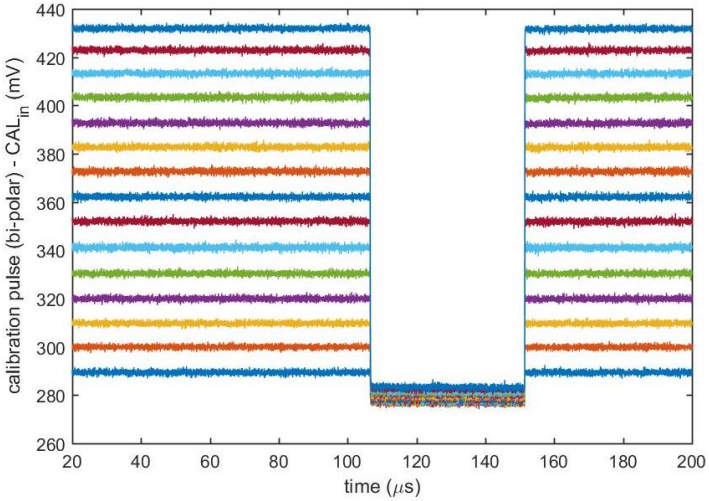


Figure 103 Double-polarity pulse generation waveforms at the CSA input.

The single polarity pulse generation waveforms were acquired for both polarities and amplitudes from 10 mV to 150 mV (charges from 1 fC to 15 fC). The discharge current was set to the minimum value of around 1.6 µA, resulting in discharge time equal to approximately 15 µs. Figure 104 shows the calibration circuit output waveforms acquired at the CSA input.

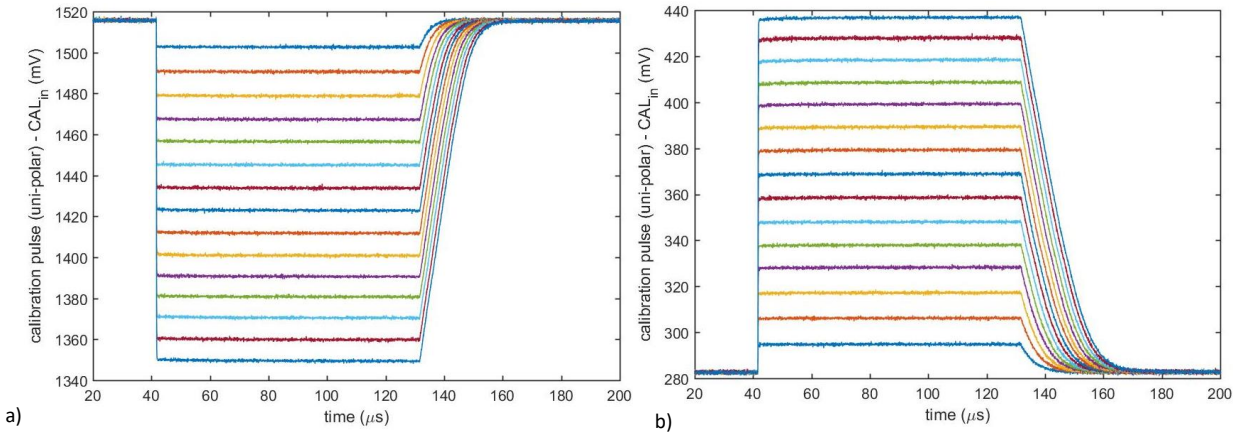


Figure 104 Single-polarity pulse generation waveforms at the CSA input: a) negative charge (electrons), b) positive charge (holes).

The discharge time regulation by the amount of discharge current was also verified. The calibration circuit output waveforms were acquired for constant pulse amplitude (injected charge) equal to approximately 100 mV (10 fC) and for 8 various settings of the discharge current (from 1.6 µA to 14.4 µA) – see Figure 105.

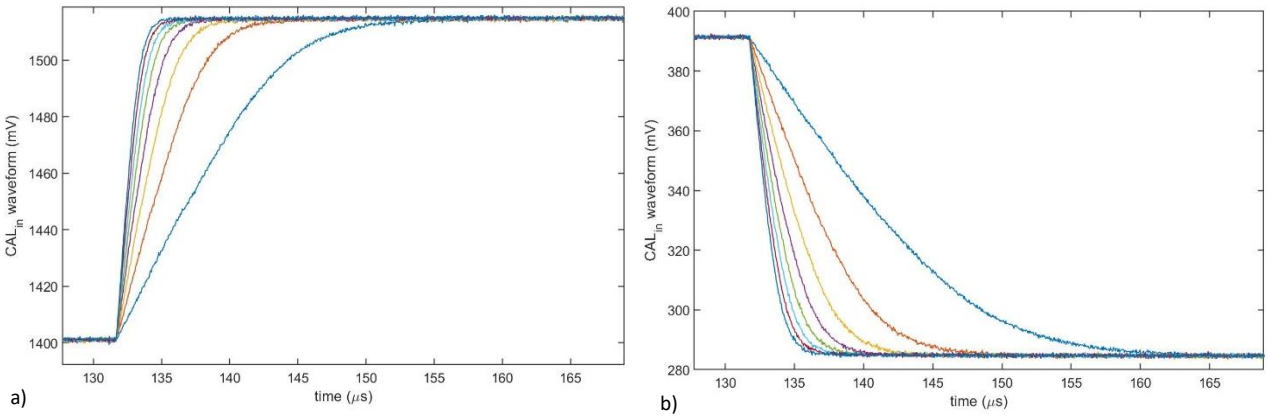


Figure 105 Charge injection - various slopes of the waveform trailing edge: a) negative (electrons), b) positive (holes)

The measured discharge times range from 3 µs to over 20 µs for the highest and lowest current setting approximately which is significantly larger than the shaping amplifiers peaking time (from 90 ns to 250 ns). The transfer function for all three modes of calibration pulse generation is presented in Figure 106, and the CSA output waveforms are shown in Figure 107. The INL for the double polarity, pseudo-single negative, pseudo-single positive is 4.23 mV (1.76%), 3.14 mV (1.31%) and 3.50 mV (1.46%) respectively.

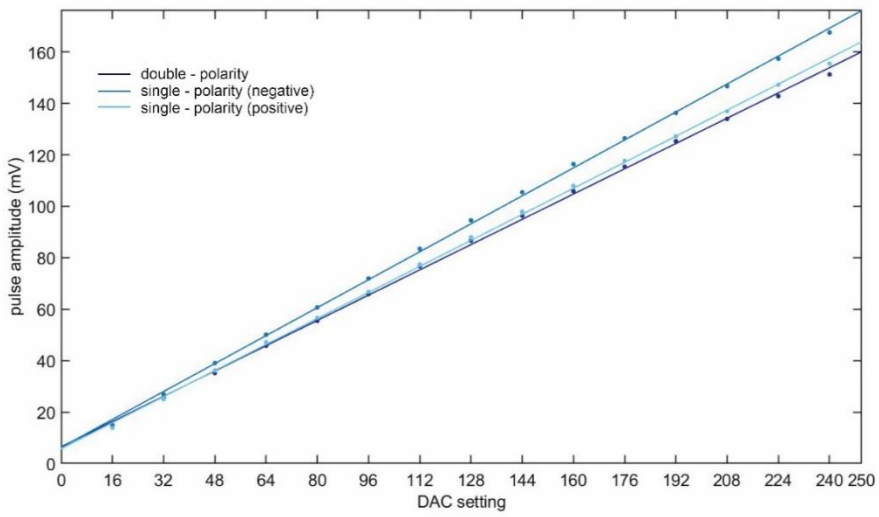


Figure 106 Calibration circuit characteristics for three modes: a) double polarity generation, b) pseudo-single polarity (negative), c) pseudo-single polarity (positive).

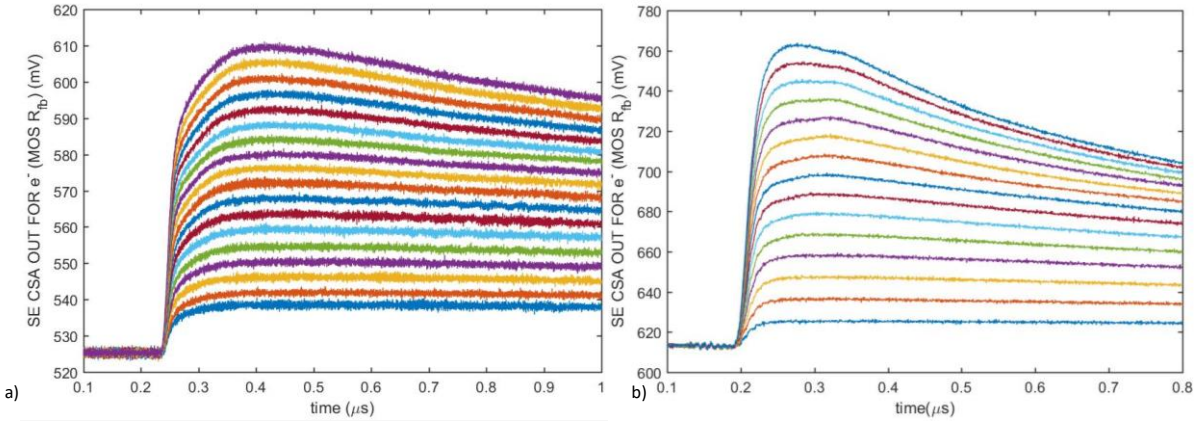


Figure 107 CSA output waveforms for a) external calibration pulse, b) internal uni-polar calibration pulse for charges from approx. 1 fC to ~15 fC.

In the SE channels, both types of CSA feedback were characterized for configurability of the effective feedback resistance for various biasing currents (Figure 108). The effective feedback resistances were estimated measuring the CSA discharge time constant and knowing the feedback capacitance. The values are from around 4 MΩ to over 100 MΩ for the MOS resistor feedback (with a default value of around 16 MΩ for DAC set to 6) and from 3 MΩ to tens of MΩ (default value 12 MΩ when the DAC is set to 12) for the Krummenachare circuit.

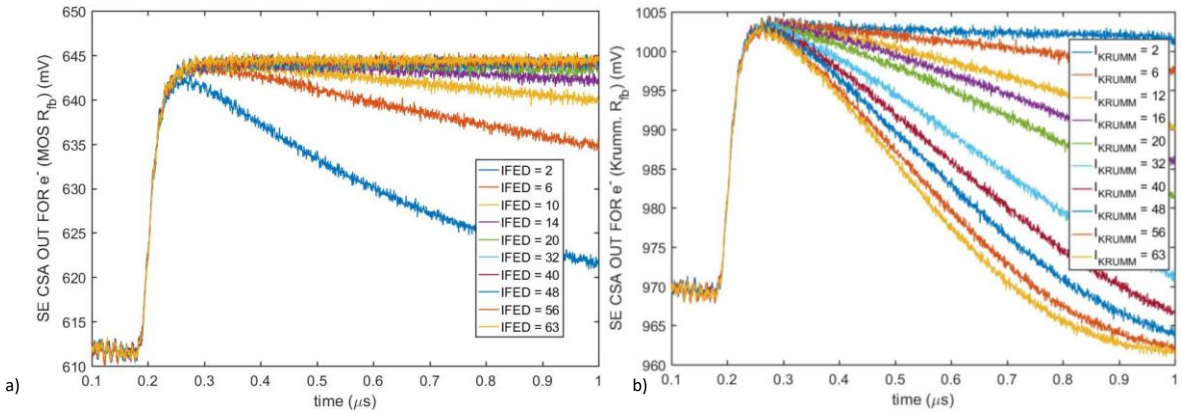
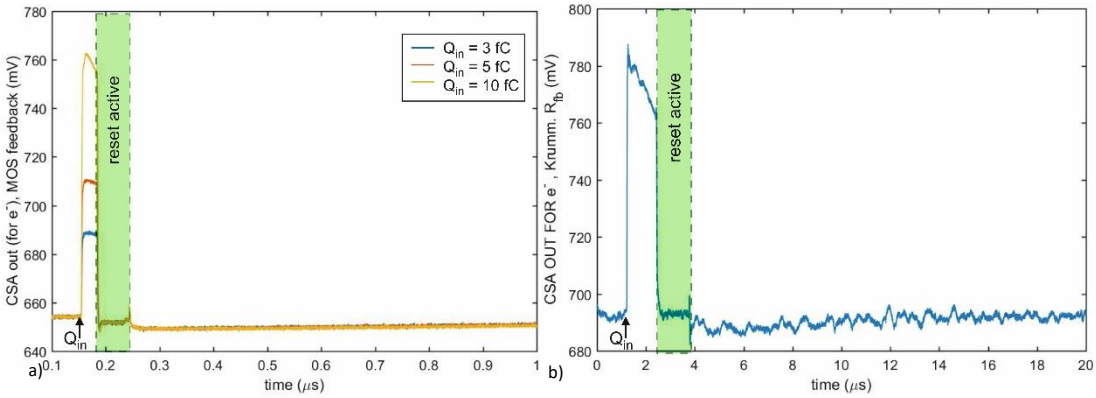


Figure 108 CSA output waveforms for various effective feedback resistances for a) MOS transistor, b) Krummenacher circuit.

The performance of both feedback types with a fast reset functionality was evaluated in measurements with and without the presence of leakage current. The reset was triggered externally and synchronized to a calibration pulse with a delay of 100 ns. The acquired waveforms for the MOS and the Krummenacher feedbacks without any leakage flowing into/from the CSA input node, are presented in Figure 109 a) and b) respectively. The waveform for the Krummenacher feedback is shown without a systematic offset of the input transistor pair, compensated externally (increasing slightly the noise). The data plotted in Figure 109 c) and d) were measured for various values and polarities of the leakage current for the MOS and the Krummenacher feedbacks respectively. The waveforms show the CSA output with the presence of leakage current from -12 nA to 12 nA. A significant DC level shift at the CSA output without the leakage current compensation is visible and this may lead to a "false hit" effect, especially if the leakage polarity is opposite than the incoming charge hit. The double-polarity architecture of the Krummenacher circuit allows for compensation of very large amount of the leakage current (up to ±40 nA) with no effect visible in the CSA output waveform – if the compensation capabilities are close to the limit for the opposite current polarity, the second part of the compensation circuit can be switched on, so that no DC level shift occurs.



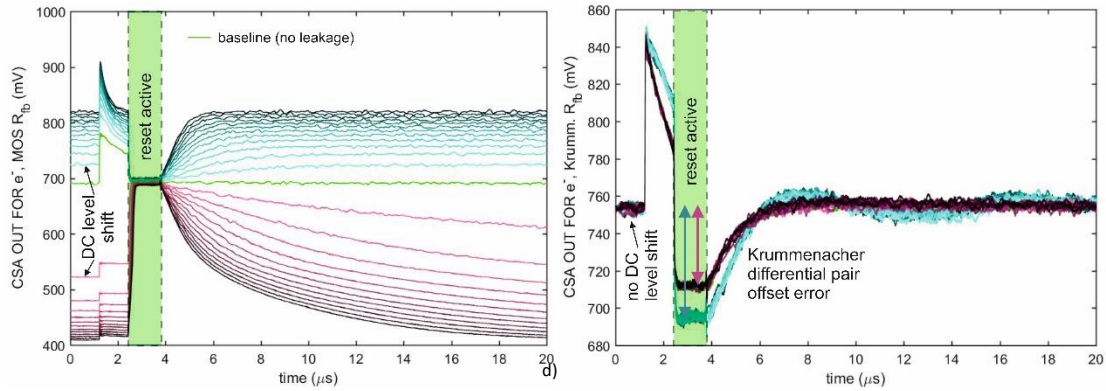


Figure 109 CSA output waveforms a) MOS transistor in the CSA feedback, no leakage current, b) Krummenacher circuit in the CSA feedback, no leakage current, systematic offset compensated, c) MOS transistor, leakage current from -12 nA (blue) to 12 nA (red), d) Krummenacher circuit, leakage current from -12 (blue) to 12 nA (red), no DC offset compensation.

4.9. Noise measurements

The noise performance was investigated for the key operation modes. The measurements were conducted without any detector attached and for C0G dielectric type capacitances up to 14.5 pF (together with PCB trace and wire-bonds parasitic capacitances estimated to be around 4.5 pF) connected to CSA inputs. The measurements were performed using a clean power supply (Keithley 2231A-30-3) and a noisy DC-DC converter (APE1707M). The ENC values acquired at the slow shaper output without the internal CSA biasing potential filtering are plotted in Figure 110 a). Figure 110 b) shows the results measured with the internal filter switched on (for the same operational modes and biasing conditions). The ENC values measured for a clean power supply (300 and 400 electrons rms without filtering, and around 280-300 electrons rms with the filter) are comparable for single-ended and pseudo-differential charge processing. This effect can be attributed to the CSA reference current source, that for example in 180 nm technology can contribute significantly to the overall system noise [77]. A significant power-supply induced interference (for example if DC-DC converters are used) can double the total input-referred noise level in single-ended channels or increase it by an even higher factor (without the usage of internal filter). Even if the filtering is employed, the ENC can rise by one third. The input-referred noise measured in the pseudo-differential channels remains the same for both clean and noisy power supply. The results indicate that, for the pseudo-differential channels, there is no significant improvement in noise performance when the filtering is applied. On the other hand, internal CSA bias filter reduces the ENC level by almost a factor of two (especially for very high power-supply induced interference).

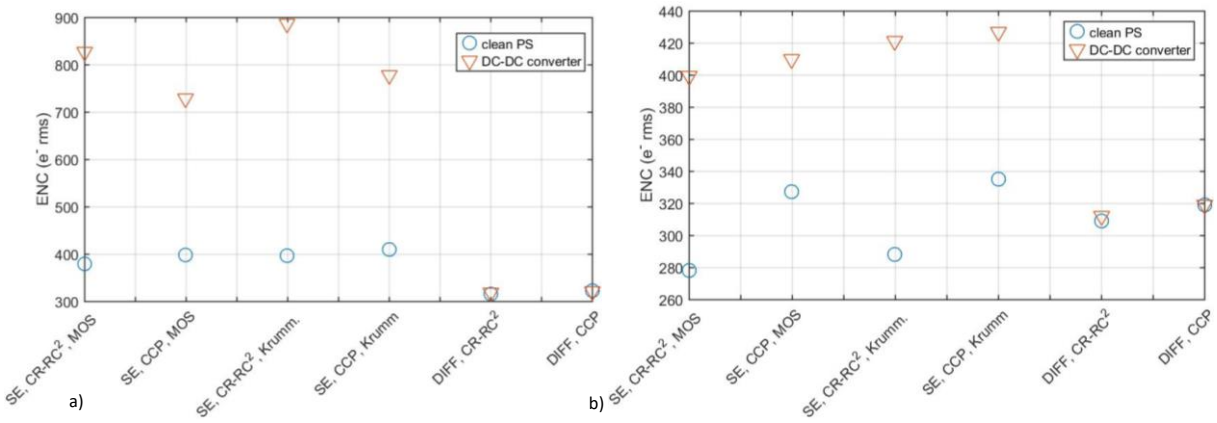


Figure 110 Comparison of measured ENC values with clean power supply and with noisy DC-DC converter for all channels and operation modes for electrons a) no internal CSA bias filter, b) with internal CSA bias filter.

The noise measurements were performed using low-leakage C0G capacitances connected to the CSA inputs to emulate the detector capacitance, and a clean power supply. The obtained slopes are plotted in Figure 111. The maximum capacitance (14.5 pF: capacitor and parasitic capacitances in total) results in an ENC value between 560 and 670 e- rms (for various channel types and operational modes). The noise slope for single-ended seems to be steeper than for the pseudo-differential channels. The mean values for SE and DIFF charge processing manners are: 26.60 e- rms/pF (electrons) / 26.08 e- rms/pF (holes) and 16.50 e- rms/pF (electrons) / 20.10 e- rms/pF (holes) respectively (Figure 111). Using small input capacitances, it can be observed in the single-ended channels, that the noise values are smaller for semi-Gaussian CR-RC^2 shaper, however, with the growing input capacitances, the complex conjugate poles in the filter transfer function result in better noise performance. This may be attributed to the fact, that for very small values of the input capacitance ($C_T \rightarrow 0$) the contribution of the parallel current to the overall output noise is more pronounced and for this noise type, the CCP 3rd order shaper provides lower weighting coefficient. This noise component is multiplied by the peaking time in the total noise calculations, so any difference between the peaking time value the two implemented types of shapers will be visible for smaller input capacitors. With enlarging the total input capacitance, the thermal and flicker noise dominate in the total noise level and the ENC increases linearly with the C_{in} as outlined by equation (50) [33]:

$$\lim_{C_T \to \infty} ENC = \frac{C_T}{q}\sqrt{\frac{v_{nw}^2}{T_p}N_w + N_f A_f} \qquad (50)$$

Where q – charge, T_p – peaking time, vnw2 – white noise spectral density, A_f – flicker noise coefficient for the particular device, N_w - white noise weighting coefficient, N_f – flicker noise weighting coefficient.

The two shaping filters have identical weighting coefficient for white noise, while the coefficients for 1/f or flicker noise and parallel current noise are different for CR-RC^2 and CCP architectures and equal to 3.41 and 3.39 and 0.64 and 0.61 respectively [33].

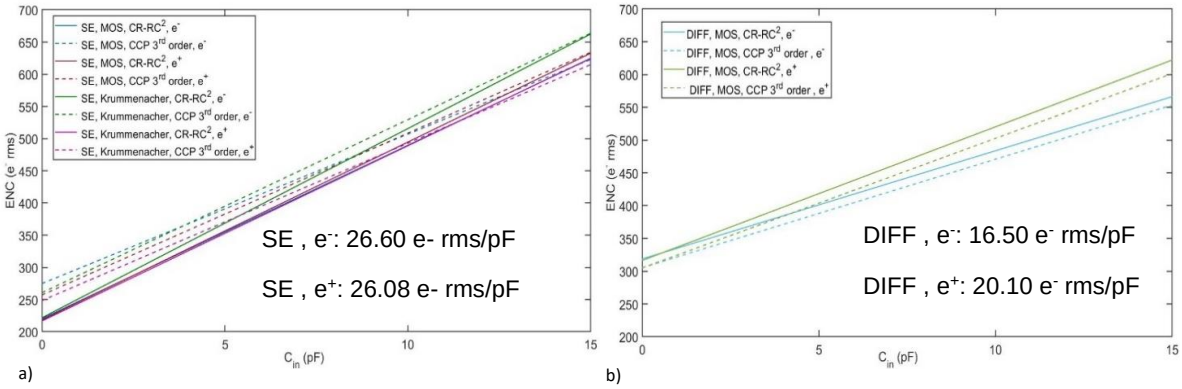


Figure 111 ENC measured for all operation modes and both polarities of input charge vs. input capacitance (detector); a) single-ended channels, b) differential channels.

4.10. Summary

In the readout systems for physics experiments, high incoming hits rate (up to 250 kHit/s/channel in the STS detector, CBM experiment at FAIR) imposes the necessity of employing fast reset of the charge sensitive amplifier for faster return to baseline. Combining fast reset with the presence of the leakage current stemming from for example MOS-based ESD protection circuit may cause performance degradation of the readout channel and false hits seen by the following stages. If the leakage polarity is unknown and the system is designed to process charges of both polarities, a double-polarity Krummenacher type circuit proves useful for leakage current compensation (verified stable operation for leakage values equal to ±40 nA with the measured effective resistance change around 15% and the DC voltage shift only ± 3mV). In this work, a Krummenacher feedback was combined with pulsed reset of the CSA and the measurements proved that it is also possible to achieve high equivalent feedback resistance (up to tens of MΩ) required for stable operation. In the complex detector systems, the conditions are not uniform for all ASICs (for example various sensor types, lengths), some of the parameters may be uncertain (dominant noise sources: voltage, current, flicker). To be able to adjust the charge processing chain to the particular conditions, switchable peaking time values (90 ns, 180 ns and 250 ns) and architecture of the shaping amplifier are proposed for in-system noise optimization. Providing a sufficiently low-noise power supply in such a complex readout system is a challenging task and many designers are facing problems with excessive interferences. Single-ended charge processing scheme is susceptible to these interferences, whereas differential or pseudo-differential architectures are proven to effectively attenuate the power supply interference (for example from 800 e^- rms for the single-ended channels to 400 e^- rms for differential architectures) at the expense of higher power consumption (8.7 mW for the single-ended and 13.7 mW for the differential) and area occupation (0.093µm^2 vs 0.146 µm^2 for the single-ended and differential respectively). To further improve the noise performance, integrated in-channel R-C filtering of the main CSA current reference. The measurements proved that this solution, significantly lowers the ENC level (by the factor of two for the single-ended channels), while no off-chip components are needed.

Chapter 5 Radiation-immune PLL design for the fast digital interfaces

5.1. Overview of the chip architecture

The Phase-Locked Loop circuit designed for fast data transceiver dedicated for applications in radiation fields is schematically shown in Figure 112. The design was aimed at 3.2 GHz output frequency for the 50 MHz reference clock. It is a second-order charge-pump PLL with digital control of the output frequency (selectable divider) and compensation for PVT and radiation-related issues. Some of the radiation immunity improving techniques were applied to the following blocks: phase/frequency detector and divider (hardening of the D-flip-flops), charge-pump, voltage-controlled oscillator - core and bias circuitry devices sizing. The following sections describe each of these elements in more details.

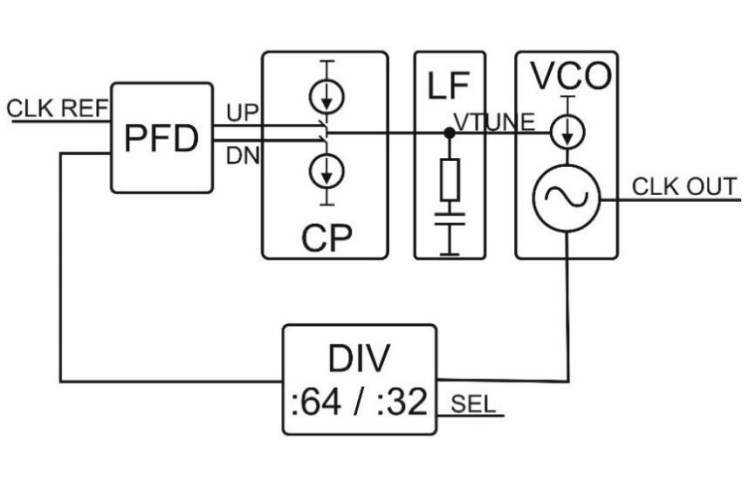


Figure 112 A diagram of the implemented Phase Locked Loop circuit.

5.2. Charge-pump architecture

The charge pump, shown in Figure 113, is based on a drain-switched architecture [124].

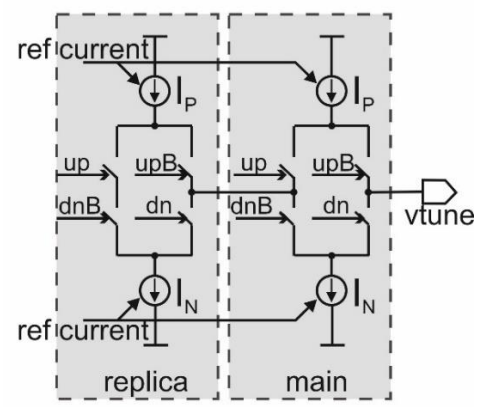


Figure 113 Charge-pump analog block idea.

To minimize the TID effects, the current sources and cascodes transistors (see Figure 114) are large: NMOS 18 µm/1.5 µm, cascode NMOS 45 µm /400 nm, PMOS 36 µm /1.4 µm, cascode PMOS 108 µm /400 nm. Thanks to the use of newer technology in the design with thinner oxide, the ELT devices are not necessary. The switches' sizes are selected to be relatively small (NMOS 2 µm/60 nm and PMOS 3 µm/60 nm) to minimize the charge injection to the output node. The charge injection occurs because NMOS and PMOS switches turning on or off, absorb or release some amount of charge, that does not need to be equal for these devices to compensate themselves during the normal switching operation. It causes a ripple on both the rising and falling edges of PFD pulses [124]. To minimize this effect, the capacitances in the loop filter should be increased, which is also beneficial from the radiation-issues point of view – the value of the capacitor connected to the CP output node directly should be maximized to minimize the voltage shift (and thus the phase deviation). As a result of calculations and taking into account both the radiation-related and charge injection effects minimization, an 11.4 pF LF capacitor was selected. Other possibilities to mitigate the charge injection include the bootstrapping technique [125] or adding a stand-by branch with dummy switches, that ensure a constant current flow through the branch when it is turned off. One possibility to keep the node between two dummy switches constant is to connect a large capacitor to the ground [124], but as shown by the simulations, much better performance can be achieved if a dummy driver is used. The main driver output is connected to the control current generating circuit of the VCO, whereas the second one is used to keep the current flowing through the CP current sources constant when the branch is off. The biasing current mirrors for both the main and the replica driver are identical and the control current is supplied externally for the possibility to adjust the CP current to control the PLL stability for the test purposes.

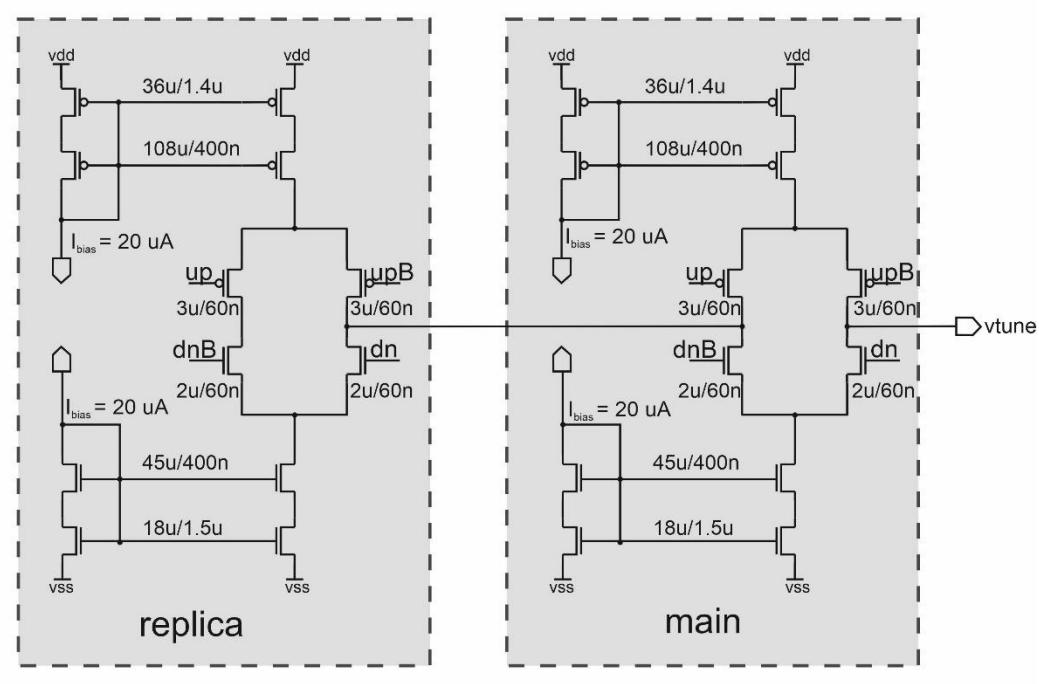


Figure 114 Charge-pump analog block the detailed view - schematics.

The simulated charge pump currents for “up” and ”dn” branches are shown in Figure 115 and the effective output charge versus the output V_{tunei} voltage (Figure 116) does not exceed 600 fC for the whole control range.

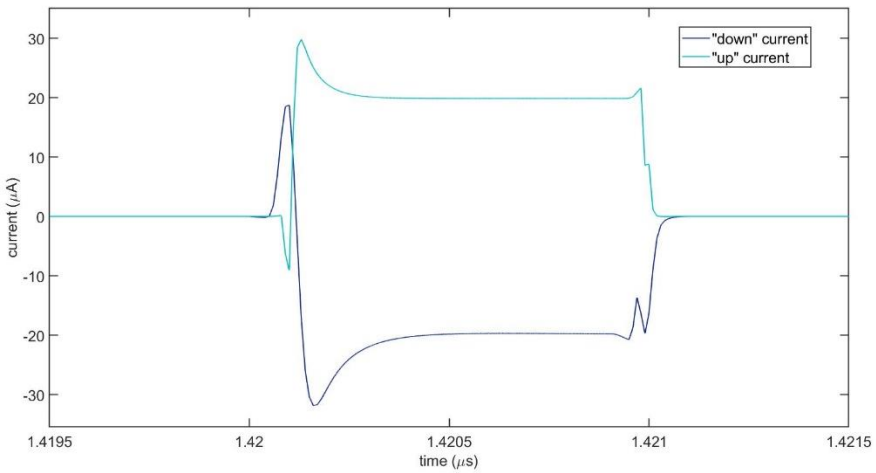


Figure 115 “Up” and “Down” currents simulated waveforms (schematic level). “Up” charge 18.34 fC, “down” charge 19.35 fC.

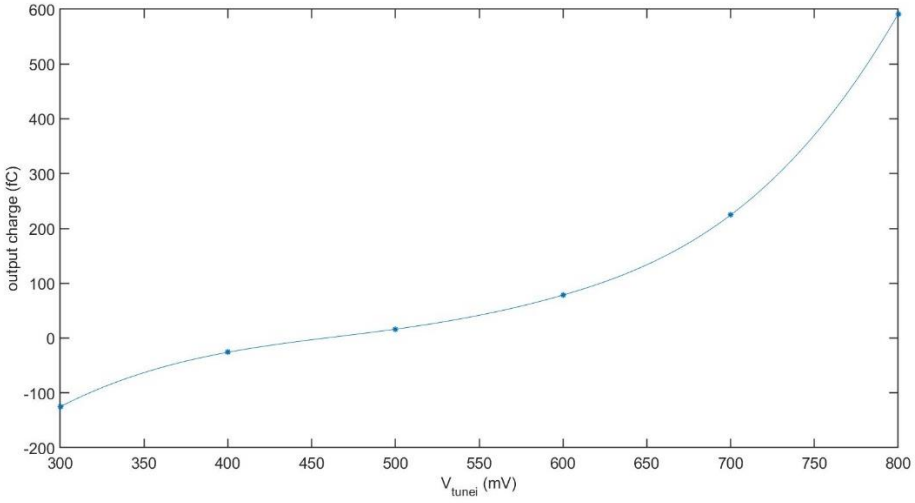


Figure 116 Charge pump output charge (simulated, schematic level).

5.3. Voltage-Controlled Oscillator architecture

The VCO in this design is based on an unbalanced starved current three-stage ring-oscillator architecture [87]. The control voltage (V_{tunei}, see Figure 117) is converted by the ring bias circuit, into a ring-oscillator control current supplying the inverters (V_{ring} supply node - Figure 117). One of the VCO outputs is connected to an AC-to-CMOS converter circuit, that cuts off the DC component and changes the signal from the V_{ring} to the core power supply domain (V_{dd} = 1 V) and is further directly routed to a buffer at the output pad as a CMOS signal. The second output is connected to a level shifter circuit also providing a shift from the lower V_{ring} to V_{dd} level and is fed back to the PFD after division (DIV).

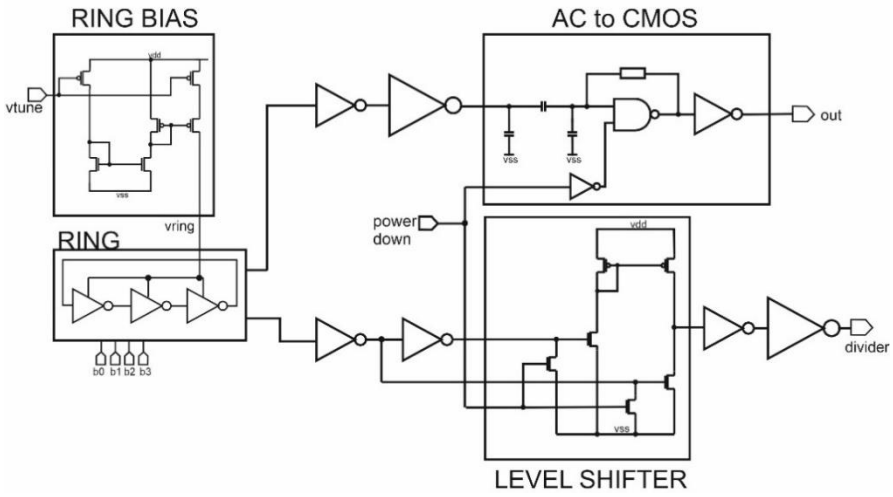


Figure 117 Voltage controlled oscillator overview.

Thanks to the use of modern submicron technology (28 nm), there is no need to employ the ELT devices for improved TID immunity. This allows achieving higher frequencies as there is no limitation in choosing the size of the transistors. However, to minimize the number of SEEs in the oscillator core and

prevent from phase steps, a large output node capacitance is necessary. To achieve this, the inverter transistors are quite large – the NMOS device W/L is 18.4 µm / 130 nm and the PMOS device aspect ratio equals 25.6 µm/ 130 nm.

The performance of the VCO was simulated across various corners and temperatures of operation (nominal 27 °C, -40 °C and 125 °C) and the results are shown in Figure 118.

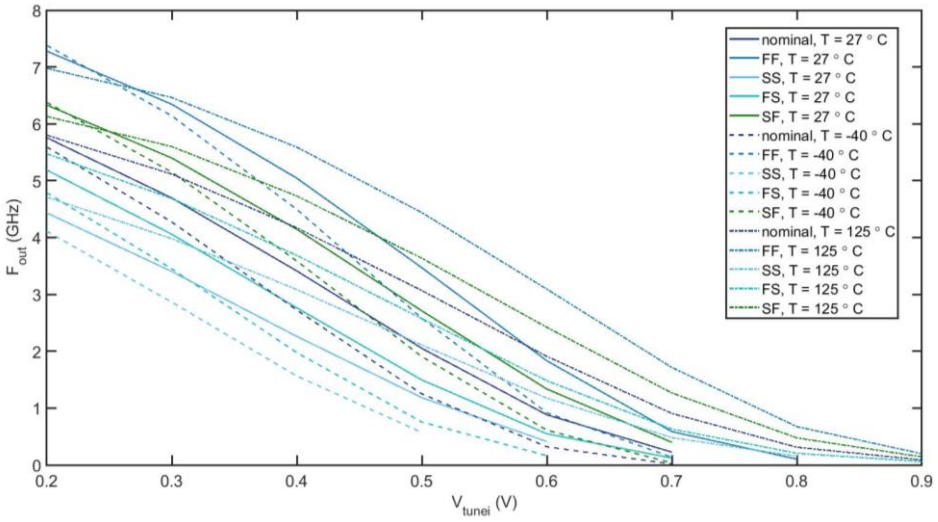


Figure 118 F_{out} vs. V_{tunei} for various corners at three different temperatures (nominal 27 °C, - 40 °C and 125 °C), each inverter in the ring-oscillator loaded with a 23 fF capacitance (wire load).

The coarse frequency tuning was added to reduce the K_{VCO} to allow for a smaller tuning range and to limit the noise coupling on the control line [124]. Smaller K_{VCO} is also beneficial from the SEU-immunity point of view and it can decrease circuit sensitivity to these effects. The coarse tuning is provided by the means of digitally switchable capacitors of total values equal to 10, 30, 50 and 90 fF [124]. The performance of the VCO for various settings of the capacitors used for coarse regulation of the tuning range was simulated and the results are shown in Figure 119. The K_{VCO} can be set between 9 GHz/V and 16 GHz/V, as shown in Figure 120. The tuning curves overlap to ensure covering the whole control range despite the PVT variations [124]. The nominal K_{vco} value is set to 16 GHz/V and for nominal settings covers the output frequencies from 280 MHz to 7.7 GHz for the whole V_{tunei} control voltage range (0.1 – 0.7 V).

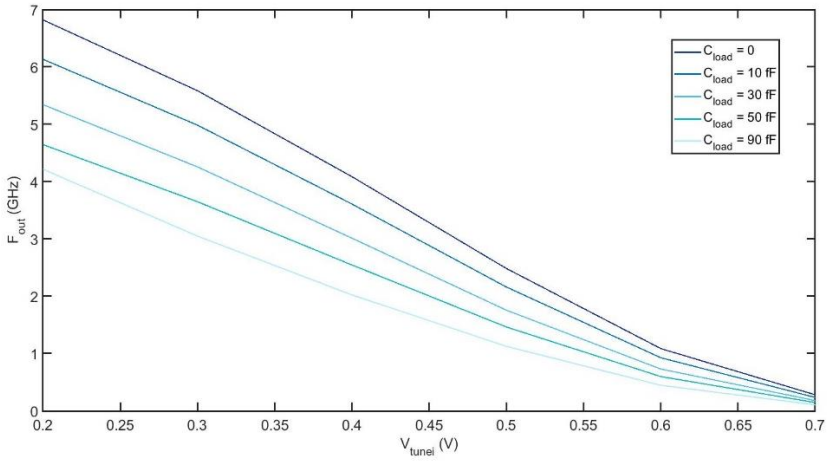


Figure 119 F_{out} versus V_{tunei} for various settings of discrete VCO tuning control word.

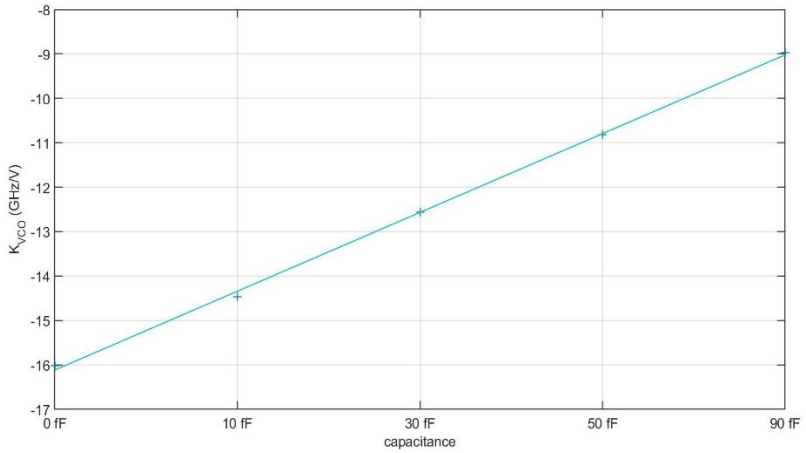


Figure 120 Kvco for various coarse regulation settings.

5.4. Phase-Frequency Detector and Divider architecture overview

The Phase-Frequency Detector, presented in Figure 121, is based on a dual interlocked storage cell (DICE) architecture combined with the Muller C-element at each flip-flop cell [93].

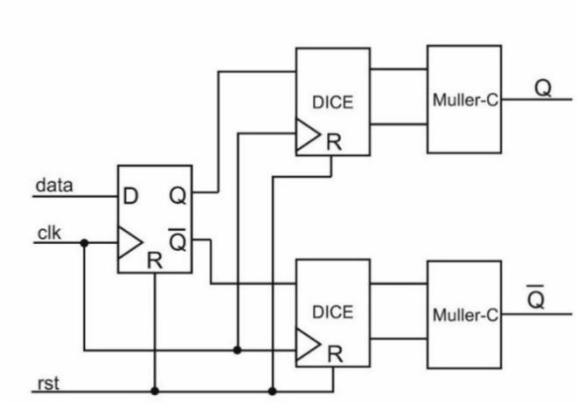


Figure 121 True single-phase clock D flip-flop with DICE latch and C-elements. [126]

A DICE memory cell contains four internal output nodes and a feedback mechanism for improved soft-errors tolerance. The DICE D flip-flop shown in details in Figure 122 comprises two elements: a D flip-flop circuit and DICE latches (at each output), that prevents the outputs change after the state is set [127]. The DICE latch operation during the high value of the clock tracks the D flip-flop output value and the value is transferred to both of the controlling nodes (the latch is transparent) and during the low value of the clock the output values are latched. In case of the change on any of the controlling nodes, the output state will not be affected. To enable incorporation into a PFD, an asynchronous reset was implemented (both in the D FF and the DICE parts). The Muller C-element at the output of the flip-flop acts as a kind of an inverter, when its two inputs have an identical logic value, and allows for the suppression of the SET pulse or, in case of any difference between the inputs, enters the high impedance mode to keep current data and mitigate a SEE [93].

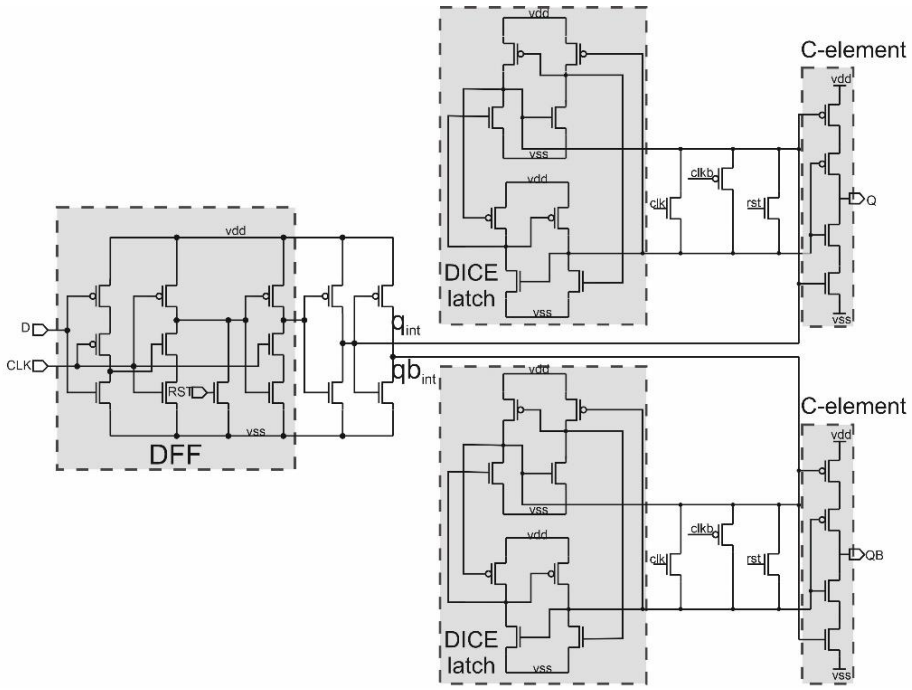


Figure 122 Transistor level schematics of the DICE DFF [93].

The PFD output UP and DN signals before driving the charge pump circuit are buffered by a chain of inverters to equalize the delays and also the reset signal for the PFD is generated with appropriate delay – see Figure 123. The delay in the reset path determines the time when both of the PFD outputs (UP and DN) are in the "high" state, and it should be chosen long enough to provide appropriate hold time for the charge pump (to allow pushing the current into the loop filter) without introducing a large dead zone (that happens if the phase difference is below the PFD sensitivity).

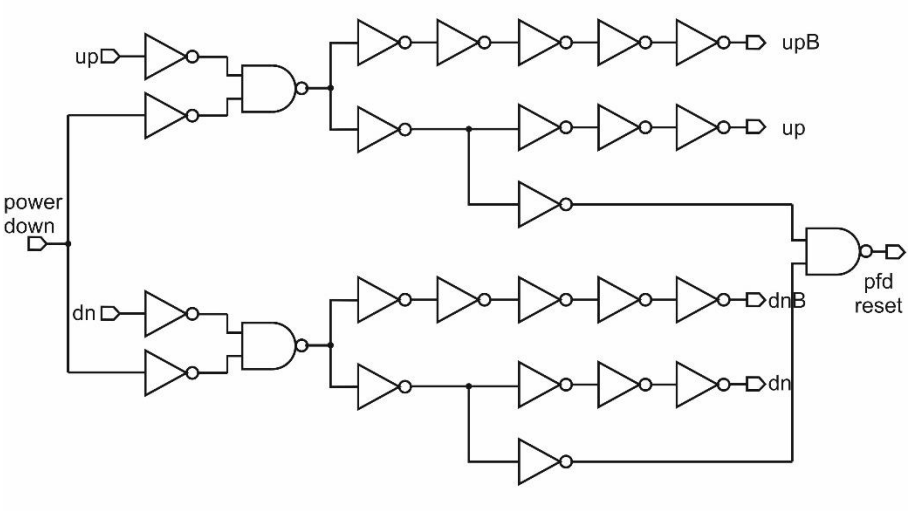


Figure 123 Delay and PFD reset generation block.

The divider (DIV) provides a selectable integer division value (32 or 64) and is a chain of divide-by-two stages realized utilizing D-flip-flops – see Figure 124. All DFFs are implemented as DICE cells combined with Muller C-element (Figure 122). To increase the robustness the last stages can be additionally triplicated (and a voter should be added), as these stages are the most sensitive to the radiation effects (lower frequency causes the errors to be more destructive for the PLL operation).

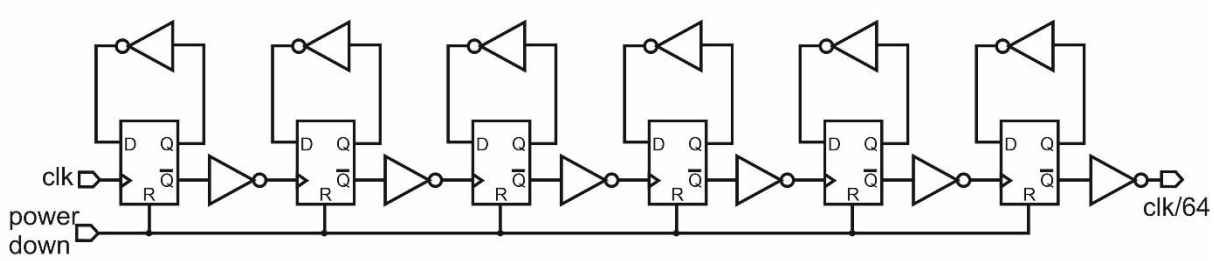


Figure 124 DICE D flip-flop based 1/64 clock divider.

The simulated behaviour of the PFD and the divider during the PLL locking process is shown in Figure 125. The picture below shows the simulated waveforms of the reference clock, divider output and up and down PFD signals in two different time frames for the nominal reference frequency (50 MHz).

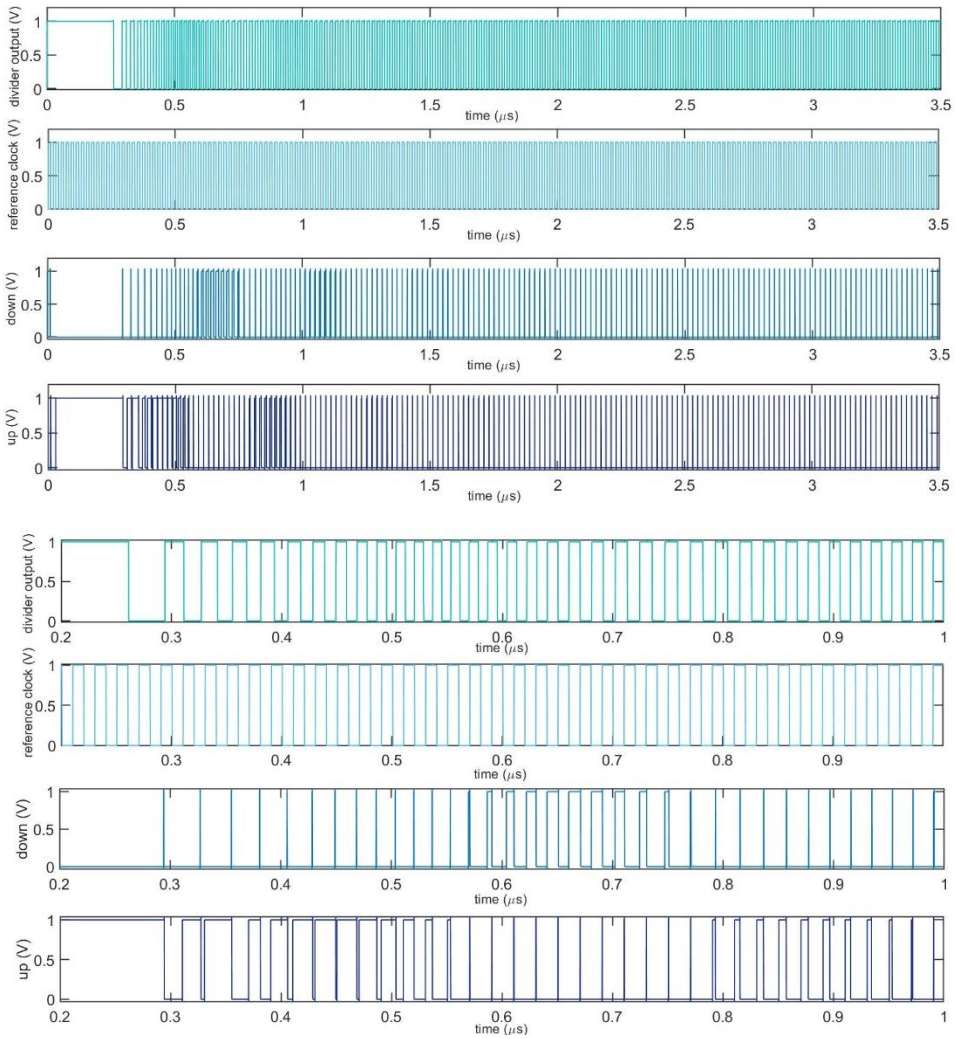


Figure 125 Reference clock, divided PLL output, up and down signals during locking phase - schematic simulation, f_{fref} = 50 MHz.

5.5. Simulated PLL performance verification

The behaviour of the designed PLL was simulated at the schematic and post-layout levels. The locking process is shown in Figure 126 and the output waveform in Figure 127.

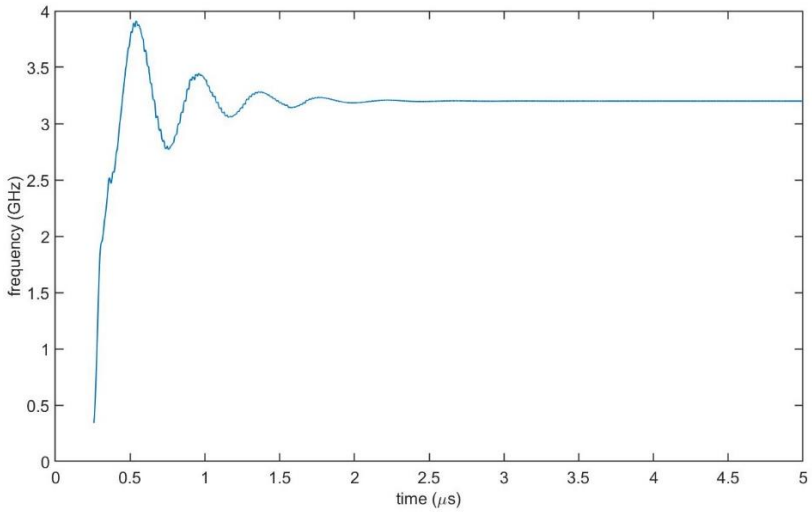


Figure 126 Simulated (schematic) output frequency (3.2 GHz), duty cycle 50.55 %. Divider mode - 1/64 mode

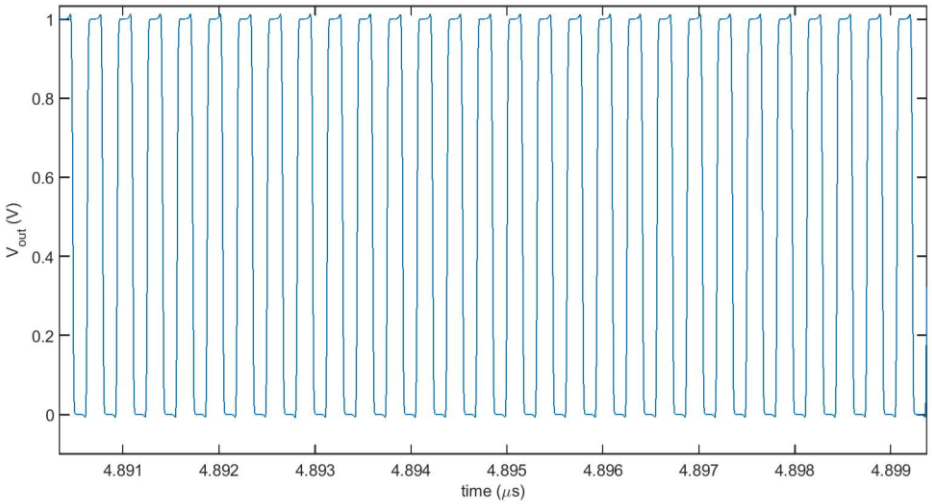


Figure 127 Output waveform in the lock state @ fref = 50 MHz, divider set to 1/64, simulated duty cycle = 50.55 %.

The circuit achieves lock after around 2 µs. The comparison of the default and the maximum achievable frequency performance is presented in Figure 128 a) (output frequency), Figure 128 b) (V_{tunei} CP/LF output voltage) and Figure 128 c) (V_{ring}, ring-oscillator control voltage). The absolute maximum frequency that can be achieved according to the simulations results reaches 8 GHz, but it is not an optimum range for the V_{tunei} to keep the proper operating point of the transistors in the ring-oscillator bias circuit (24 mV is too low). However, the desired output frequency is 3.2 GHz and the stable operation of the PLL is guaranteed up to around 5 GHz.

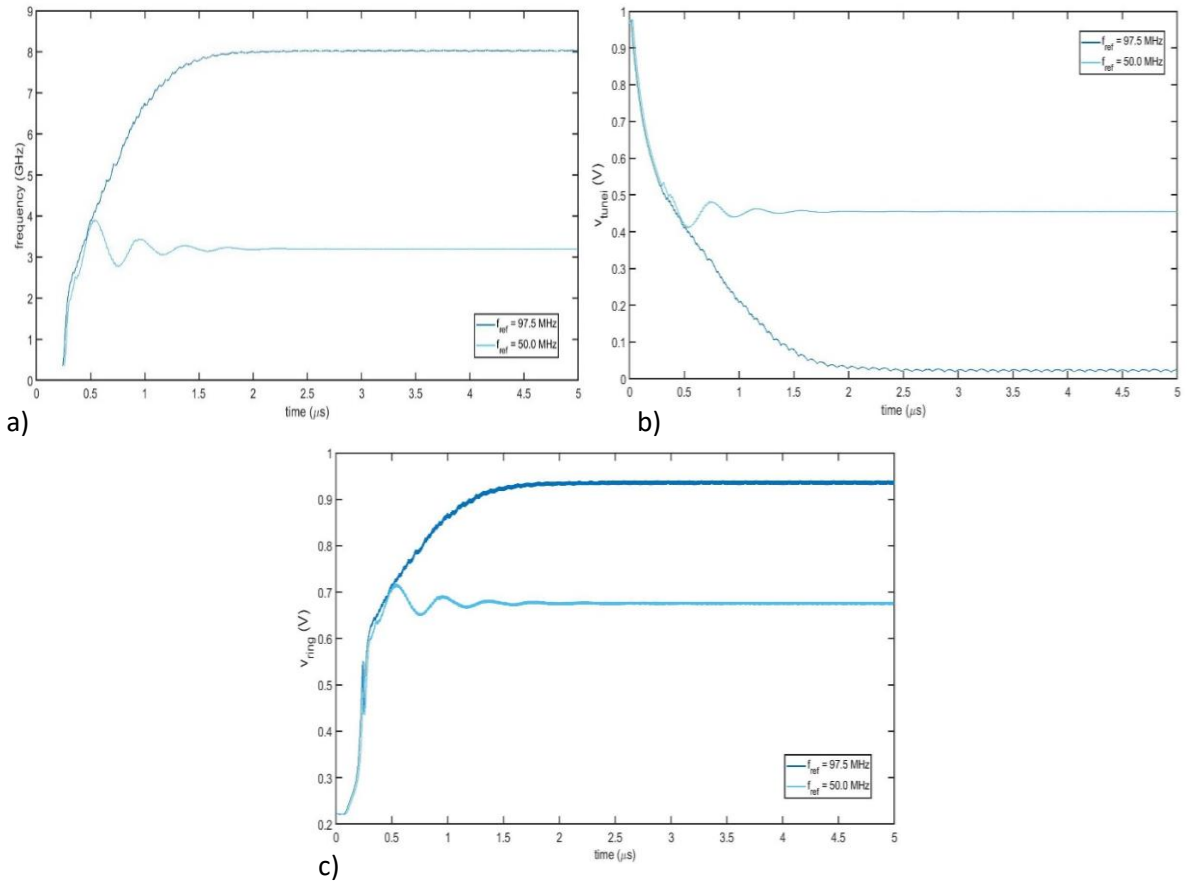


Figure 128 a) f_{out}, b) V_{tune}, c) V_{ring} during locking process - simulation (@ schematic level, f_{ref} = 50MHz and 97.5 MHz).

The layout of the PLL ASIC with the pad ring and decoupling capacitors array is shown in Figure 129. The chip dimensions are 920 µm x 440 µm, and the circuits occupy an area of 650 µm x 101 µm.

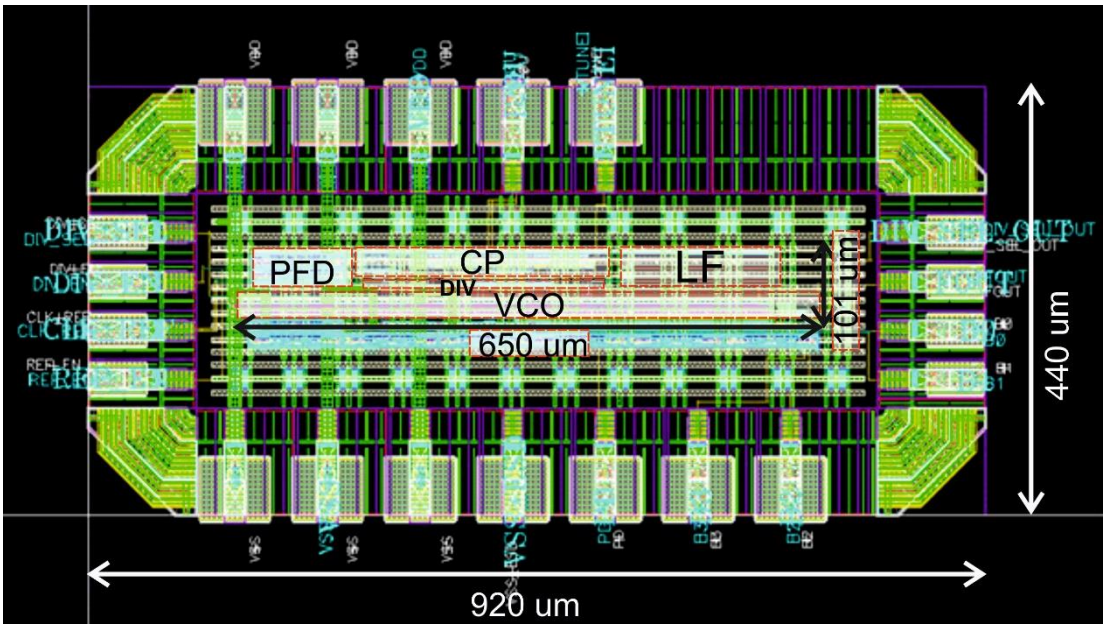


Figure 129 Layout of the PLL circuit.

The post-layout simulations of the circuit show that the performance is compatible with the schematic-level behaviour and meets the design specifications (output frequency 3.2 GHz @ fref = 50 MHz,

slightly longer locking process – see Figure 131). The PFD output signals acquired during the locking process are shown in Figure 130.

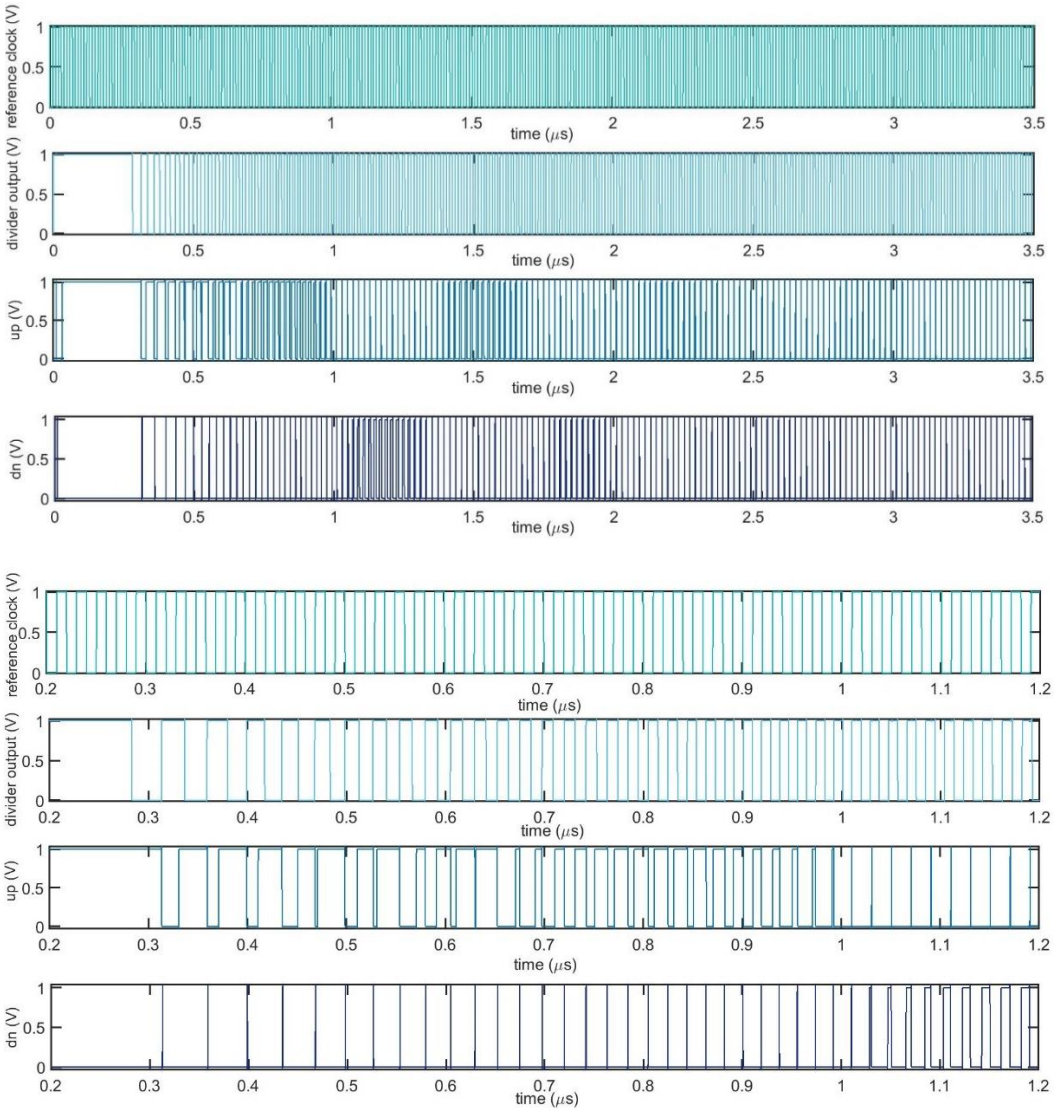


Figure 130 Reference clock, divided PLL output, up and down signals during locking phase - post-layout simulation.

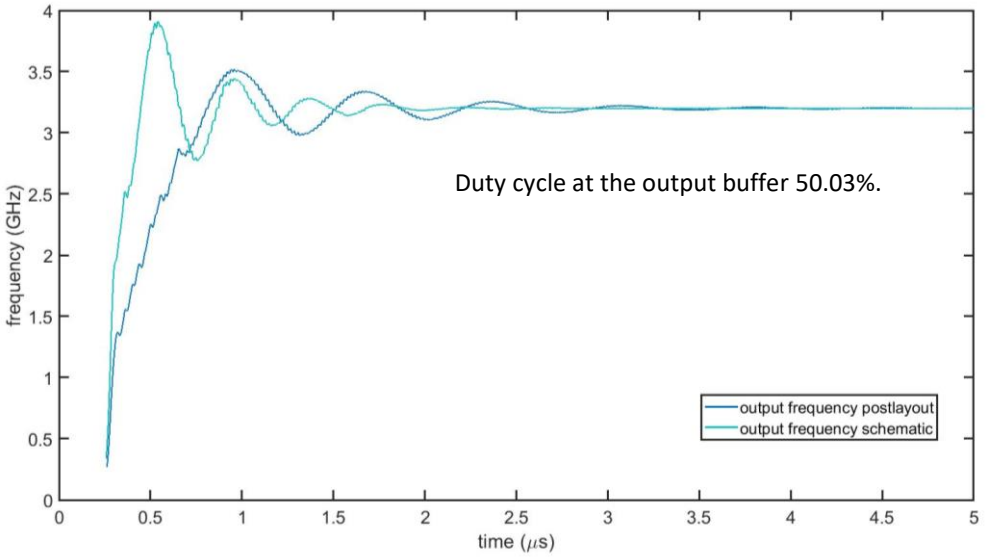
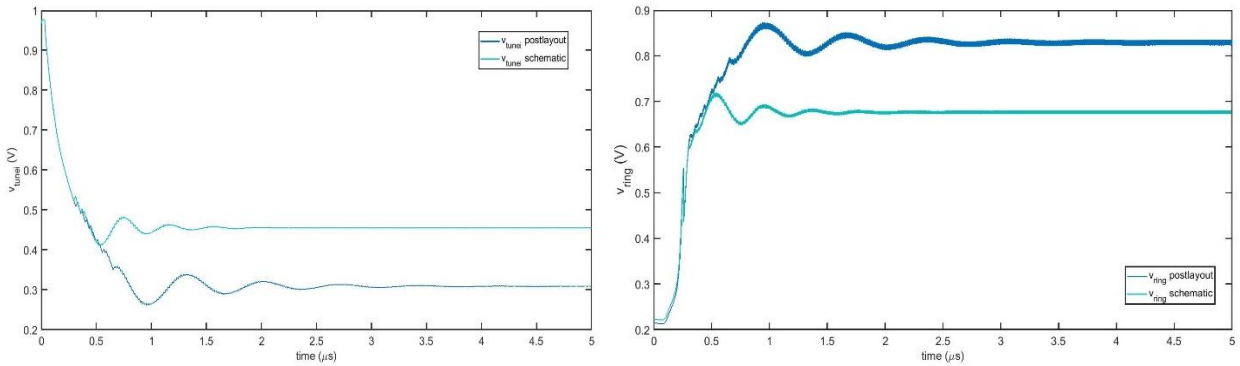


Figure 131 Post-layout (VCO) vs. schematic simulated behavior @fref = 50 MHz, divider 1/64. Fout(post-layout) = 3.198 GHz vs Fout(schematic) = 3.2 GHz.

The comparison of the control voltage V_{tunei} and the ring supply voltage V_{ring} for the schematic and post-layout levels is shown in Figure 132 a) and b) respectively. Some discrepancies in the voltage level are visible but still, the circuits operate within the proper range. In case of any bigger shift in the fabricated dies the coarse tuning is provided to compensate for this offset.



a) b)

Figure 132 Simulated voltages; a) Vtunei, b) Vring.

The coarse regulation waveforms acquired for V_{tunei}, V_{ring} voltages and the output frequency in the post-layout simulations are shown in Figure 133 a), b) and c) respectively.

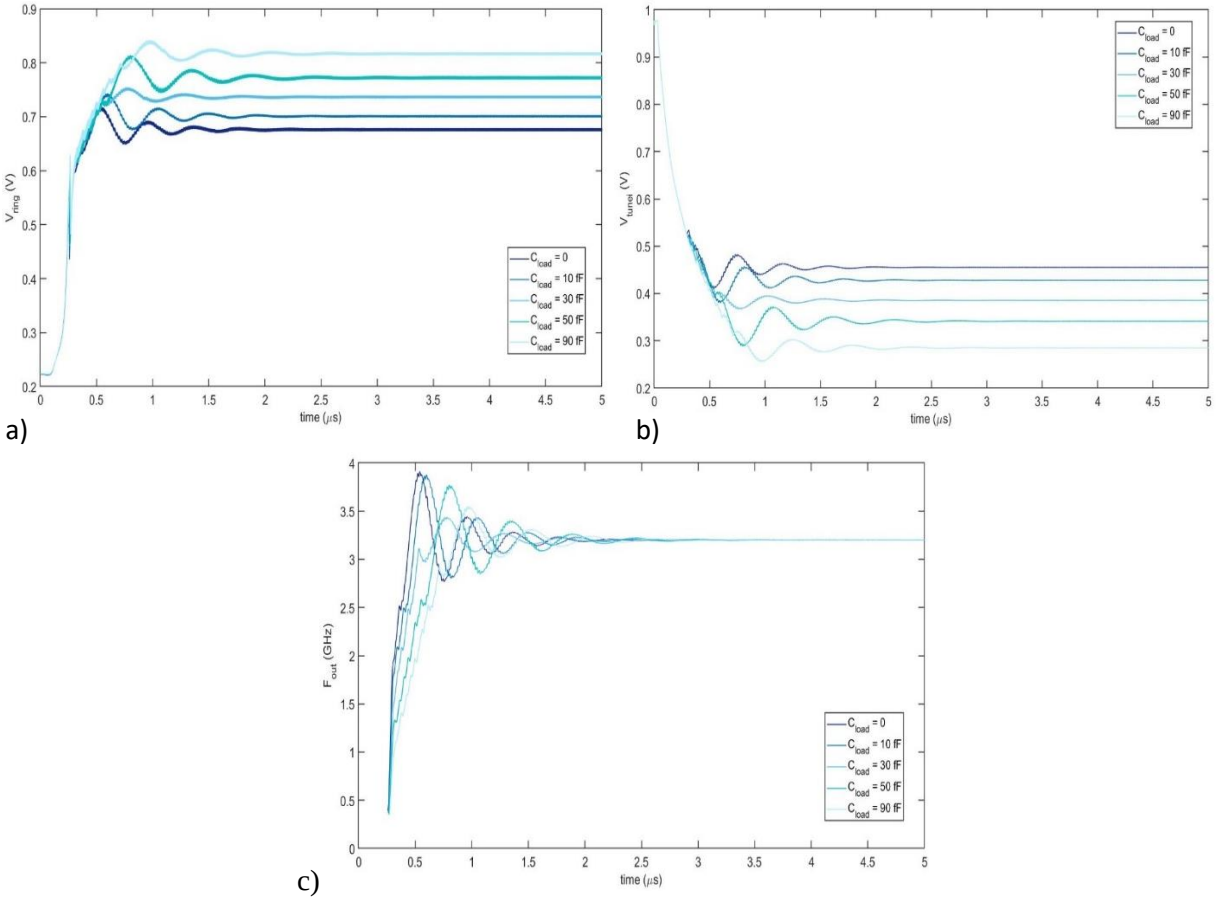


Figure 133 Locking process for various settings of coarse regulation; a) v_{ring} voltage, b) v_{tunei} control voltage, c) output frequency.

The period distribution histograms for nominal case (both for schematic and post-layout simulations) are presented in Figure 134. The comparison of the values of period jitter, the rms period jitter and the peak-negative period jitter is shown in Table 23.

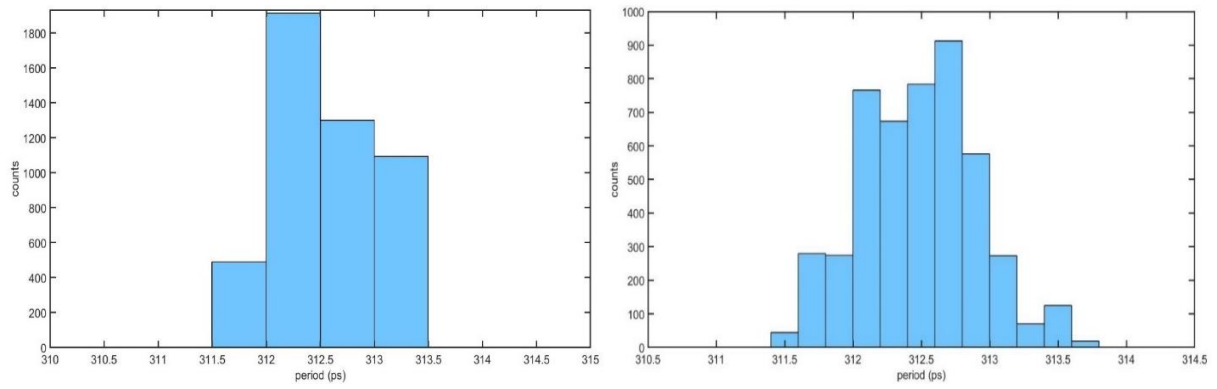


Figure 134 Output waveform period distribution histogram after lock @f_{ref} = 50 MHz; a) schematic simulation, b) post-layout simulation.

Table 23 Schematic vs post-layout performance comparison

	Schematic	Post-layout
Output frequency	3.200 GHz	3.198 GHz
Period jitter p-p	1 ps	2.2 ps
rms period jitter p-p	0.5 ps	0.4 ps
Peak-negative period jitter	0.5 ps	0.9 ps

The circuit immunity to the SEEs was tested using a 2.4 mA current injected into a node in a 10 ns pulse, 1 ns rising and falling edges to generate a charge of 24 pC. From Figure 135 it can be seen that, as expected, the node that is most sensitive to the radiation-related effects is the charge pump output/loop filter node. The SEE in this place results in large transient visible on the output frequency and the lock loss which is recovered after approximately 1.5 – 2 μs. Other nodes that result in smaller transients if hit by a radiation particle are the divider and VCO outputs. Smaller or no effect on the output frequency is visible if the SEE happens on the PFD output signals, the PFD reset signal or the DFF-based divider internal nodes.

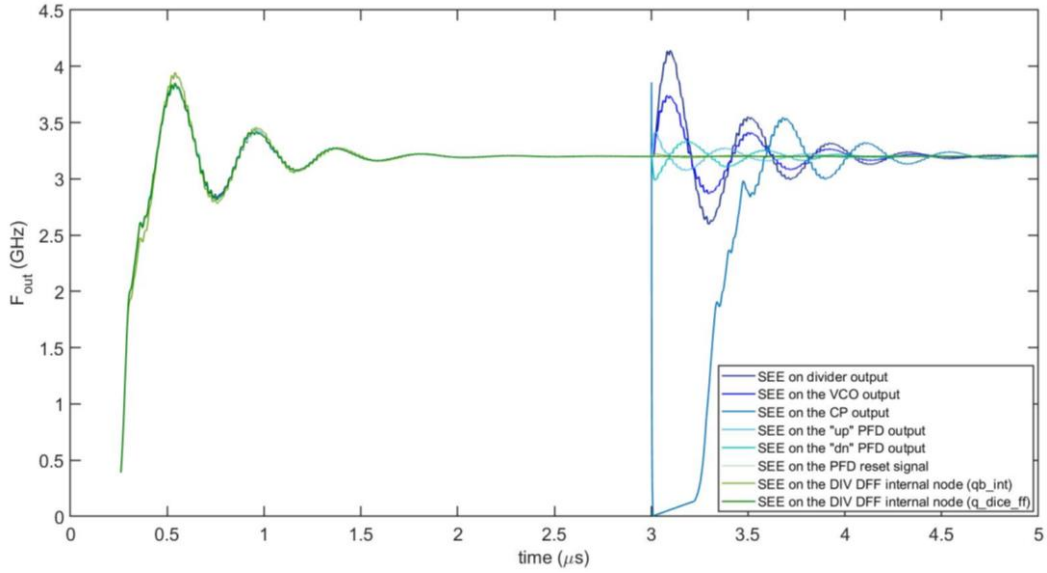


Figure 135 The effect of a simulated SEE effect on various PLL nodes on the output frequency.

5.6. Summary

The works presented in this chapter aimed to explore the possibility to employ newer technologies in the design of data transceivers for the High-Energy Physics experiments detector readout electronics. As shown in Section 1.6, the most common technologies used in such experiments are 180 nm, 130 nm, 90 nm, whereas more modern technology nodes (like for example 65 nm or 28 nm) can benefit from the higher speed, lower power, smaller occupied area and less sensitivity to the total irradiation dose (TID) errors (due to thinner transistors oxide). However, according to the literature study, there are still very few research works towards employing the 40 nm or 28 nm planar technologies in the field of High-Energy Physics experiments. In this project, the main emphasis was put on ensuring radiation-tolerance against Single-Event Effects of the main component of the transceiver, which is the phase-locked loop circuit. Application

of the radiation-hardening by design (RHBD) techniques in the design of the circuit aimed to achieve high operation speed, is always related to the degradation of the maximum circuit frequency. It is due to the application of redundancy (duplication- DMR or triplication – TMR of the critical design blocks and adding a majority voter), enlarging the transistors connected to the critical nodes, or use of the enclosed-layout (ELT) devices (in older technologies mostly) to prevent from TID-effects.

The author of this work used some RHBD techniques for the design of the PLL including an alternative approach to the TMR, that is based on the dual-interlocked cells (DICE) combined with the Muller-C element to radiation-harden the main building block of the frequency divider. The transistors in the charge pump are enlarged as well as the capacitance in the loop filter to minimize the influence of the radiation on the sensitive analog parts of the circuit. Also, the size of basic elements of the ring oscillator is enlarged and there are scaled capacitors added at each stage of the ring, to decrease the sensitivity to the SEEs as well as provide coarse tuning in case of any PVT variations or radiation-related damages. The simulation results show that the desired output frequency can be set to 3.2 GHz nominally, or even higher, despite the use of the more complex circuitry. The post-layout simulations are promising, and also the results of the simulated performance after a radiation-induced event show, that the PLL loose lock only when it happens on the most sensitive node (loop filter input) and the circuit recovers within a reasonable time. The circuit is implemented in the 28 nm CMOS technology, and, once fabricated, the performance will be verified also with the use of the radiation. The simulation results show that a PLL circuit implemented in this can be further incorporated in the design of the data transceiver dedicated for the HEP experiments and is very promising for the development of the new facilities, that can enable much higher data transmission speed and throughput, especially for the self-triggered or event-based detector readout. The PLL can be used to build RHBD serializers for future use in the detector readout systems.

Chapter 6 Summary and conclusions

The works included in this doctoral project were focused on the design of the low-noise analog front-end for the readout of the silicon strip sensors and the research towards new technologies and solutions application in the circuits for fast data transmission in the radiation environments. As a result of the research, the author designed three prototype integrated circuits: two analog front-ends and a PLL circuit aimed for the application in the High-Energy Physics Experiments. The main achievements and goals leading to the conclusions and Dissertation Theses confirmation are listed below:

- Design, simulation, layout and performance verification of the multichannel SMX_mini read-out ASIC.
- Design, simulation, layout and performance verification of the multichannel PRINCSA read-out ASIC.

The optimization of the analog charge processing circuitry included the following tasks:

- Measurements, analyses and circuits design for the full-size prototype readout circuit for the CBM experiment (SMX2.1 and SMX2.2).
- Design of on-chip internal bias potentials monitoring circuit that can withstand extended temperature and supply voltage variations.
- Implementation of double-polarity leakage current compensation method (switchable Krummenacher circuit) in combination with the CSA fast reset for high input count rate.
- Detailed noise studies including all the system components: internal (related to the read-out electronics) and external (concerning the sensor, power-supply network, interconnect etc.) basing on the sensor and cables models for the CBM experiment modified and evaluated for this purpose.
- Optimization of the read-out electronics towards lower noise (ENC) in the varying environment (various cables' and sensors' lengths). Development of new readout architectures adjustable to external conditions by employing a wide range of configurability in the charge processing channel such as switchable shapers architecture using a minimum number of the passive component divided into small components for better matching.
- Evaluation of the differential/pseudo-differential charge processing advantages in the specific conditions of high power supply interference coupling and minimization of crosstalk in mixed-mode designs.
- Implementation of internal CSA input transistor bias filters and study on the maximum achievable read-out electronics noise mitigation.
- Implementation of an improved internal calibration circuit for the pseudo-single polarity charge studies (with a minimum injection of the opposite polarity charge to the read-out channel) and more flexible characterization of the charge processing circuits.
- Study on the possibility to speed-up the charge processing capabilities in the presence of leakage current while providing stable, low noise performance of the CSA

The research towards faster data transmission and increased link throughput to be implemented in the radiation environment applications was summarized by designing and simulation verification of a radiation-tolerance improved Phase-Locked Loop for future use in the read-out systems for data transmission. The works included the following tasks:

- Study on fast data transmission, towards the development of a transceiver in newer technology (still rarely employed in the ICs for the HEP experiments), evaluation of the technology limits and possibilities to ensure radiation-hardened performance.

1. Thesis: Differential charge processing can be efficient in low-noise systems with the tight area and specific environmental constraints. Differential charge processing in the read-out electronics for

detectors is rarely used due to higher power dissipation, larger area occupancy and intrinsically higher noise. However, this assumption is true only if the clean supply voltage can be provided. There are applications where the use of differential or pseudo-differential charge processing architectures may become beneficial. These applications include tracking detection stations where the power supply induced interference coupling is not negligible, cannot be externally filtered due to magnetic field and influences the electronics performance significantly. – The expected radiation dose and high magnetic field prevents the use of the commercial off-the-shelf low noise DC-DC converters/linear voltage regulators and ferrite-based inductors. **In the complex tracking detectors readout systems, where it is impossible to provide a clean power supply, a differential or pseudo-differential charge processing manner can prove useful. As shown by the measurements, differential channels, that in the laboratory conditions with the clean power supply show higher output noise level than the single-ended ones, are almost insensible to the external interference coupling, while in the single-ended channels a significant noise growth is observed. In the tracking detectors where external noise filters are not feasible, differential charge processing is worth considering at the expense larger area, power dissipation.**

2. Thesis: It is possible to improve the noise performance in the harsh and variable environment with varying and complex dominant noise sources contribution by in-depth analysis and simulation of the longitudinal and transverse architecture of the detector and connection to the read-out electronics and by employing configurability in the read-out electronics, especially in the shaping filters to adapt and a better match to the external conditions. **– The improvement of the noise performance by detailed models analysis based on both calculations and simulations of various combinations of environmental variables: going beyond the standard approach and classical optimization for the particular detector capacitance (matching the CSA input transistor size to obtain C_{in} = 1/3 C_{det}), as there are various detector lengths and therefore capacitances (together with the interconnect capacitance), and taking into account all noise contributions of the entire readout system, adding configurability in filter type and shaping time (while not complicating the design more than adding few more switches in the shapers' feedback network).**

3. Thesis: Stable operation of the Charge Sensitive Amplifier (CSA) with high equivalent feedback resistance while providing fast input charges processing in the presence of excessive leakage current of the unknown and variable amount and flowing direction, can be obtained by the combination of digitally-assisted fast reset with the leakage current compensation techniques. - **For the Compressed Baryonic Matter experiment, for example, an incoming charges average hit rate assuming Landau-distribution is equal to 250 kHit/s/channel is required. The combination of the CSA feedback resistance with the digitally assisted fast reset (employing externally triggered switch) helps to achieve processing speed high enough to handle the rate**

of the incoming hits up to 1 MHit/s/channel. If there is no leakage current present in the readout system, it can be easily achieved. However, in the presence of even 1 nA leakage, the processing speed is degraded to 375 kHit/s/channel, while if the leakage grows to 5 nA, the maximum achievable channel occupancy falls to 150 kHit/s/channel.

4. Using newer technologies in the design of data transmitting circuitry is beneficial not only in terms of speeding up the operation and data transmission which is required in the complex read-out systems generating a huge amount of data but also can decrease the sensitivity of the circuit to the radiation-related effects (Total Irradiation Dose) and enable employing acceptably effective Single Event Effects mitigation techniques without compromising the available area and possible operating speed. - **The radiation-hardening by design (RHBD) techniques applied in the high-speed circuitry unavoidably cause degradation of the maximum circuit operating frequency. The use of for example 28 nm, according to the simulated behaviour of the circuit implemented in this technology, is promising for future use in the SERDES circuits dedicated for the HEP experiments and development of the new facilities. The main advantage of the use of newer technology nodes is higher data transmission speed and throughput while providing radiation-immunity of the transceiver circuit. Such circuits can be employed especially in self-triggered or event-based readout systems.**

The results of the ongoing work were presented by the author at various international conferences, such as the IEEE Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), International Workshop on Radiation Imaging Detectors (iWoRiD), International Conference Mixed Design of Integrated Circuits and Systems (MIXDES), MOS-Ak India, IEEE-SPIE Joint Symposium on Photonics, Web Engineering, Electronics for Astronomy and High Energy Physics Experiments, CBM Collaboration Meeting. The author published her work in the international journals from the JCR list, such as Journal of Instrumentation (2 articles - [75], [118]) or Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment (one article published [37], one being revised and will be published soon) and many other papers (SPIE [66], [80], [128], CBM collaboration reports – e.g. [52], [129]) and conference proceedings ([130], [131]) – 18 articles in total during the PhD project duration.

The future works will focus on the development of the circuitry for the fast data transceivers dedicated to future HEP experiments. The Phase-Locked Loop performance will be tested with the use of the radiation and evaluated for further improvement. The study on the radiation-immune SERDES circuits is also considered.

Appendix A – PRINCSA configuration bitstream

	Name	Default value	Bits	Default value	Description
1	CALamp	16	<0:7>	17.57uA ->10 mV ampl.	Calibration circuit - > pulse amplitude
2	CALdisch	0	<8:10>	1.64 uA -> 15 us	Calibration circui discharge current
3	CALbias	4	<11:13>	20/40 uA (N/P)	Calibration cirucit buffer bias current
4	CAL_pol	0/1	<14>	0/1.8V	Calibration pulse polarity
5	in_csa	32	<16:21>	2 mA (536.1 mV)	CSA input transistor bias
6	buf_csa	3	<24:26>	30 uA (416.9 mV)	CSA output buffer bias current
7	cas_csa	3	<27:29>	30 uA (935.7 mV)	CSA cascode bias current
8	bias_csa	27	<32:37>	1V	CSA cascode gate voltage
9	csa_switch	0	<38>		
10	ifed	6	<40:45>	330 nA (1.233 V)	CSA feedback transistor reference current
11	ikrumm	12	<48:53>	12 nA	Krummenacher feedback reference current
12	bias_core	2	<56:58>	40 uA (580.6 mV)	Shapers core bias current
13	bias_p	2	<59:61>	20uA (463.7 mV)	slow shaper core (1st, 2nd) load cascode (PMOS) bias, from 10uA to 40uA, 20uA nominal
14	bias_n	2	<64:66>	20uA (1.136 V)	slow shaper core (1st, 2nd) load cascode (NMOS) bias, from 10uA to 40uA, 20uA nominal
15	bias_EA	2	<67:69>	60uA (579.4 mV)	Error amplifier core bias
16	bias_buf	3	<72:74>	30 uA (1.089 V)	Shapers output buffers bias
17	in_csa_sel	1	<75>	on	in_csa filtering selection, 1- on, 0-off
18	pol	0/1	<76>	electrons/holes	
19	pol_krumm	0/1	<77>		Ileak from/to csa input node
20	sh_type	0/1	<78>	CR-RC2/CCP 3rd	sh slow type
21	fb_sel	0/1	<79>	MOS/Krumm	CSA feedback type
22	vref_shslow	47	<80:85>	700mV	shslow reference voltage
23	shslow_tp	0	<86:87>	0, 1, 2	peaking time selection
24	vref_shfast	14	<88:93>	1.1 V	shfast reference voltage
25	vref_cmfb	30	<96:101>	0.9V	cmfb reference voltage

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