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Faculty of Electrical Engineering, Automatics, Computer Science and Biomedical Engineering

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Ph. D. dissertation

*DIGITALLY-ASSISTED ANALOG CIRCUITS FOR HYBRID
PIXEL X-RAY DETECTORS*

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Rozprawa doktorska

*WSPOMAGANE CYFROWO UKŁADY ANALOGOWE DLA
POTRZEB HYBRYDOWYCH DETEKTORÓW
PIKSELOWYCH PROMIENIOWANIA X*

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ABSTRACT

The dissertation describes the theoretical studies and experimental tests of the multichannel readout circuits for hybrid X-ray detectors, addressing aspects of the design of integrated circuits which contain both analog circuitry as well as digital logic integrated on the same silicon substrate. Combining more and more functionality inside a pixel is a trend observed in nowadays readout integrated circuits. However, integration of several blocks of diverse functionality in each readout channel and implementation of inter-pixel communication impose new challenges in the process of simulation, design, implementation and verification of the integrated mixed-mode systems.

Scientific problems addressed by this dissertation aim at improving design process of mixed-mode readout integrated circuits, in particular, with the algorithms dealing with charge sharing implemented inside a chip. To achieve this goal, the basic concepts of X-ray detector systems and their limitations are studied. Then, the algorithms implemented in mixed-mode integrated circuits for dealing with charge sharing and selected solutions from the literature are discussed. The C8P1 algorithm, developed by the ASIC group from the AGH University of Science and Technology, is a subject of detailed conceptual analyses and simulations as a known solution to the charge sharing problem. The simulation approach to this algorithm and implementation of realistic models, including practical aspects, for example non-ideal comparators, noise or analog parameters spread is presented. The influence of analog parameters spread on the detector registration is analysed. The simulations are conducted in static and dynamic modes.

The target of the experimental part of the thesis is to confirm the conclusions obtained through the simulations. Firstly, the architecture and design aspects of the multichannel readout integrated circuit named Chase Jr. chip with the C8P1 algorithm are presented. The operation and configuration of the chip with an emphasis on analog path reconfiguration for the purpose of testing and trimming is revealed. The dedicated measurement environment implemented for the Chase Jr. tests and the practical realisation of the testing procedures for the Chase Jr. chip are described. The measurement results for the Chase Jr. chip bonded to a silicon sensor are shown. Three types of experiments are conducted: the preliminary integrated circuit tests without X-ray radiation performed for calibration purposes, the experiments using an X-ray tube and the experiments using specialised synchrotron source, used mainly for the assessment of the algorithm dealing with charge sharing in this work. The experiments include the tests of signal reconstruction in the case of charge sharing, the tests of registration at pixel borders, the tests of influence of correction on the C8P1 algorithm and the high count rate tests.

The results of the simulations and measurements lead to the conclusions that the integrated circuit with the C8P1 algorithm switched on allows reconstruction of the total photon energy from fractional signals in the case of charge sharing between two or four pixels, and thus, the photons

can be detected even at pixel borders, where the standard approach fails. This proves that the charge sharing effect occurring in hybrid pixel detectors can be compensated by mixed analog-digital circuits implemented inside the readout electronics using inter-pixel communication strategies. However, increasing pixel-to-pixel gain spread, DC offset spread and noise, result in the significant degradation of the detection efficiency in the C8P1 mode. Therefore, there is a need for dedicated correction circuits to minimise the analog parameters spread between channels and assure the proper operation of the detector. The results of the tests of the Chase Jr. chip prove in practice, that it is possible to overcome technology limitations regarding analog parameters spread of the multichannel integrated circuits for hybrid pixel detectors with inter-pixel communication, using digitally assisted correction blocks.

ABSTRAKT

Niniejsza rozprawa przedstawia rozważania teoretyczne, wyniki symulacji oraz pomiarów wielokanałowych układów odczytowych dla hybrydowych detektorów promieniowania X. Układy takie zawierają zarówno część analogową jak i cyfrową, zintegrowane w jednym układzie scalonym. Widocznym trendem w projektowaniu tych układów jest zwiększanie funkcjonalności pojedynczego kanału, co stawia nowe wyzwania w procesie symulacji, projektowania i testowania zintegrowanych systemów analogowo-cyfrowych.

Podjęte w ramach tej pracy rozważania naukowe mają na celu optymalizację procesu projektowania analogowo-cyfrowych scalonych układów odczytowych, w szczególności zawierających algorytmy do minimalizacji efektów związanych ze zjawiskiem podziału ładunku. We wstępie wprowadzono podstawowe pojęcia, opisano zjawiska i rozwiązania dedykowane detekcji promieniowania X. Następnie, przedstawiono algorytmy i implementacje układowe podejmujące próby rozwiązania problemu podziału ładunku w detektorach pracujących w trybie pojedynczego zliczania fotonów opisane w literaturze. Przedmiotem szerszych badań koncepcyjnych i symulacyjnych stał się algorytm C8P1, zaproponowany przez grupę projektowania układów scalonych z Katedry Metrologii i Elektroniki, Akademii Górniczo-Hutniczej. W pracy zaproponowano statyczne i dynamiczne modele układu odczytowego uwzględniające m.in. rozrzuty parametrów analogowych pomiędzy kanałami, wynikające z efektów niedopasowania technologicznego oraz szumy.

W eksperymentalnej części pracy zaprezentowano architekturę, zasadę działania oraz konfigurację układu scalonego Chase Jr. z zaimplementowanym algorytmem C8P1. W celu przeprowadzenia zautomatyzowanych testów samego układu oraz detektora składającego się z układu Chase Jr. zbondowanego do krzemowego czujnika, zaprojektowano oraz zaimplementowano dedykowane środowisko testowe. Przeprowadzono trzy rodzaje eksperymentów: wstępne testy układu scalonego bez promieniowania X w celach kalibracyjnych, testy z użyciem lampy rentgenowskiej oraz testy synchrotronowe. Przedmiotem szerszej analizy były procedury korekcyjne i wpływ korekcji na poprawność detekcji, rekonstrukcja sygnału w detektorze w przypadku podziału ładunku oraz działanie detektora w warunkach promieniowania o dużym natężeniu.

Zarówno wyniki symulacji jak i pomiarów pokazują, że układ scalony z zaimplementowanym algorytmem C8P1 pozwala na odtworzenie pierwotnej energii padającego fotonu w przypadku podziału ładunku pomiędzy dwa lub cztery piksele, zatem fotony mogą zostać zarejestrowane nawet na krawędziach pomiędzy pikselami. Oznacza to, że podział ładunku może zostać skompensowany przy wykorzystaniu

układów analogowych wspomaganych cyfrowo wykorzystujących komunikację międzypikselową. Jednakże, zaobserwowano i udowodniono, że znaczący wpływ na jakość detekcji mają szумы elektroniki odczytu oraz rozrzut parametrów analogowych układu, takich jak offset DC na wejściu dyskryminatora czy wzmocnienie. Wskazano na konieczność stosowania dedykowanych układów i procedur korekcyjnych do minimalizacji rozrzutów pomiędzy kanałami, co jest warunkiem poprawnej pracy detektora. Wyniki uzyskane w testach układu Chase Jr. bezpośrednio udowadniają, że możliwe jest pokonanie ograniczeń technologicznych dotyczących rozrzutów parametrów analogowych w hybrydowych pikselowych detektorach promieniowania X, wykorzystując cyfrowe wspomaganie bloków analogowych.

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