AGH University of Science and Technology
Faculty of Electrical Engineering, Automatics,
Computer Science and Biomedical Engineering

Doctoral thesis

Tomasz Dziwiński

Selected Methods of Real-Time Digital Signal Processing for Control of the Power Electronic Converters

Kraków, 2017

Principal supervisor	prof. dr hab. inż. Wojciech Grega AGH University of Science and Technology Faculty of Electrical Engineering, Automatics, Computer Science and Biomedical Engineering Department of Automatics and Biomedical Engineering al. Mickiewicza 30, 30-059 Kraków, Poland
Co-supervisor	dr inż. Paweł Piątek AGH University of Science and Technology Faculty of Electrical Engineering, Automatics, Computer Science and Biomedical Engineering Department of Automatics and Biomedical Engineering al. Mickiewicza 30, 30-059 Kraków, Poland

Declaration of the author of this dissertation:

Aware of legal responsibility for making untrue statements I hereby declare that I have written this dissertation myself and all the contents of the dissertation have been obtained by legal means.

date, signature

Acknowledgements

First and foremost, I am deeply grateful to my principal supervisor prof. Wojciech Grega for five years of support, patience and encouragement. As much I am grateful to my co-supervisor dr Paweł Piątek, who introduced me into the world of scientific research and took care of my individual scientific development. It has been an honor to work under their supervision. I am feeling gratitude for the experience they have shared, for the valuable comments they have given and for time they have spent supporting my research. This work certainly could not have been done without their help.

I would like to thank all the personnel working at the Department of Automatic Control and Biomedical Engineering for the experience they have shared. The members of this department have contributed immensely to my personal and professional time at the University. I would like to give a heartfelt, special thanks to dr Andrzej Tutaj, dr Jerzy Baranowski and Paweł Zagórski for hours spent in discussions, exchange of views and exploration of knowledge and for being source of friendship. Together they have known answer to almost every question.

I would like to thank to the chief of the Electrical Power Quality and Utilization Laboratory, prof. Zbigniew Hanzelka for creating favorable conditions for cooperation between departments and to my colleagues from Department of Power Electronic and Energy Control Systems as well. Mainly due to them I became interested in the topic of power electronic systems. I would like to express my deepest thanks to dr Krzysztof Chmielowiec and dr Krzysztof Piątek.

I would like to express my gratitude to ABB Corporate Research Center in Västerås, Sweden for the opportunity of internship in Electric Machine and Motor Control Department, especially to dr Mikael Dahlgren, the R&D Manager, dr Robert Chin, EMMC Group Manager, dr Luca Peretti, dr Ville Särkimäki and Giovanni Zanuso, my friends. Thank You for making my time in Sweden such valuable and pleasant as well and full of positive experience.

Last, but not least I offer my regards to all of those who supported me in any respect during the completion of this work.

Tomasz Dziwiński
Kraków, 21st of February 2017

Research has been carried out within the framework of EIT InnoEnergy International PhD School.

This research work has been carried out at the AGH University of Science and Technology in Kraków. The research has been partially funded by:
"Doctus – Małopolski fundusz stypendialny dla doktorantów", scholarship program co-funded by the European Union under the European Social Fund

Contents

List of Acronyms

AC	Alternating Current
ADC	Analog-to-Digital Converter
BJT	Bipolar Junction Transistor
CCM	Continuous Conduction Mode
DC	Direct Current
DCM	Discontinuous Conduction Mode
DSP	Digital Signal Processor
EMC	Electromagnetic Compatibility
FET	Field Effect Transistor
FIFO	First-In, First-Out
FIR	Finite Impulse Response
FPGA	Field Programmable Logic Array
GTO	Gate Turn-Off thyristor
IGBT	Insulated Gate Bipolar Transistor
JFET	Junction gate Field Effect Transistor
LFT	Linear Fractional Transformation
LSB	Least Significant Bit
LTI	Linear Time-Invariant system
MCT	Metal-oxide-semiconductor Controlled Thyristor
MIMO	Multiple Input and Multiple Output
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PID	Proportional-Integral-Derivative controller

PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulator
RMS	Root Mean Square
SISO	Single Input and Single Output
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface bus
THD	Total Harmonic Distortion

List of Symbols

B	Viscous friction coefficient
C	Capacitance
D	Duty cycle
$G_{\mathrm{C}}(s)$	Controller transfer function
I_{L}	Average inductor current
J	Moment of inertia of a shaft
K_{m}	Armature constant
L_{a}	Armature winding inductance
L_{f}	Field winding inductance
L_{m}	Entire motor winding inductance
L	Inductance
N	Buffer length
$P(s)$	Plant transfer function
R_{L}	Inductor ohmic resistance
R_{a}	Armature winding resistance
R_{f}	Field winding resistance
R_{m}	Entire motor winding resistance
R_{o}	Load ohmic resistance
$S(s)$	Sensitivity function
$T(s)$	Complementary Sensitivity function
T_{s}	Switching period, $\frac{1}{f_s}$
U_{C}	Average capacitor voltage
U_{g}	Input DC voltage
η	Efficiency
$\langle\cdot\rangle_{T_{\mathrm{s}}}$	Average value over period T_{s}
ω	Angular rate
ϕ_{m}	Phase margin
τ_{L}	Load torque
Φ_{f}	Field excitation flux
ε	Quantization error
e_{m}	Back electromotive force
$f * g$	Convolution of functions f and g
f_{s}	Switching frequency
g_{m}	Gain margin

i_{L}	Inductor current
i_{m}	Series motor current
s_{m}	Stability margin
u_{C}	Capacitor voltage

1 Introduction

1.1 Purpose

This Thesis is devoted to analysis and investigation of digital control methods for power converters. The effective power processing relies on a switching-mode technique. Switching converters find many applications in modern electronic devices, such as Alternating Current (AC) motor inverters, switching-mode power supplies, uninterruptible power supplies or grid-connected photovoltaic inverters. Moreover, as there is a growing demand for miniaturized devices, it is important to reduce power processing losses. Higher efficiency resulting in smaller heatsink and cooling components can significantly reduce the overall size and the temperature of device.

The topic of efficient and small power converter seems to be very actual and demanded. On July 2014 Google Incorporation and the Institute of Electrical and Electronics Engineers Power Electronics Society (IEEE PELS) announced the competition to design and develop a very small inverter for 2 kVA load. The specification list contained numbers of limitations, such as power density greater than or equal to 50 W/in^3, electromagnetic compliance confirmation, low harmonic distortion factor, etc. The organizers of the competition assumed that developing such a small power converter unit could benefit in lower price of industrial and domestic photo-voltaic systems, affordable microgrids for remote regions of the globe or supplementary function of electric cars for stabilizing the electrical grid (see [26]).

The topic of power electronic converters is very interesting not only from electronics and solid-state physics perspective, but also from a control engineering point of view. The dynamics of electronic switching-mode converters, as well as linear voltage regulators can be accurately modeled (in opposite to e.g. electromechanical systems, where the friction dynamics is usually very difficult to model). State vector variables (voltages and currents) can be easily measured with very high accuracy. Therefore, the gap between simulation and experimental evaluation of control algorithms is not so great as it might be for other applications of control engineering. This property is extremely helpful when testing and verifying complex control algorithms.

Despite the numerous switching converters circuits and topologies, some common principles and general rules can be pointed out. First and most important fact is that power processing is always associated with losses. The efficiency of switching converter can be expressed as a ratio of output power (P_{out}) and input power (P_{in}):

$$\eta = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} \tag{1.1}$$

The relationship between output and input voltage and current is found by:

$$\frac{i_{\mathrm{out}}}{i_{\mathrm{in}}} = \eta \frac{u_{\mathrm{in}}}{u_{\mathrm{out}}} \tag{1.2}$$

Highly efficient solutions are of a particular interest mostly due to limiting heat dissipation in semiconductors and passive elements. Power-efficient switching-mode converter can be built from more accessible and smaller transistors and requires less surface of the heat sink, therefore might be more portable. Another major factor, which usually greatly impacts overall converter size is inductor dimension. Switching converters generally use inductor-based filters to limit undesirable effect of voltage and current ripples. In buck converter for example, the magnitude of the output current ripple is inversely proportional to the inductance L and switching frequency f_{s} (eq. 2.10). Therefore to reduce the dimension of inductor L, while keeping the output distortion at the same level, one can increase the switching frequency f_{s}. That option, however is limited by the inability of control system to act suitably fast and by the power transistors to have short transition state and react promptly enough. This creates a need for research on high-speed and advanced methods of control systems.

The generalized block diagram of switching-mode converter is shown in Fig. 1.1. The controller of the converter block has three input signals and one output signal. Feedforward and feedback signals come from analog sensors – current and voltage transducers, that measure the converter input and output waveform parameters, respectively. The reference value is the desired parameter of converter power output waveform. The reference signal can be either analog, wired physically to control system or digital representation of the expected output waveforms parameter, present in microprocessor memory only. Depending on the converter type, reference signal can be constant (DC/DC and AC/DC converters) or variable in time (DC/AC and AC/AC converters).

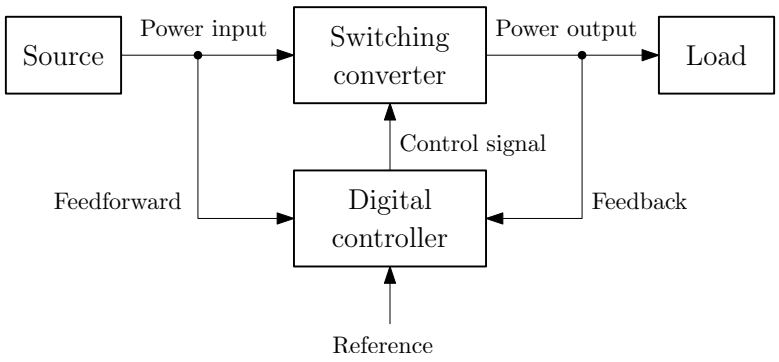


Figure 1.1: Basic configuration of power processing block and controller (based on [21])

Well designed control system plays a critical role to guarantee tracking of the reference signal within the specified steady-state error. The disturbances in process control are associated mostly with changes in the power source parameters or the load parameters. Controller should observe variations of input voltage and output current and react promptly to stabilize the system. Furthermore, controller can be designed for reduction of power losses related to unnecessary power switch operations (transitions) and therefore increase power processing efficiency.

The following Thesis addresses the problems of real-time algorithms embedded in digital control systems designed for power electronic converters. The scope of the considered field is very wide and has connection points with many other areas and disciplines, like computer engineering, power electronics, software and hardware engineering. Therefore, only limited part of the subject and selected issues are contemplated in this work. The Author of the doctoral dissertation decided to verify the following theses:

1. Adapting control algorithms of electrical power converters for the realization on dedicated hardware platforms can improve the quality and reliability of energy supply.

2. Despite the complexity of the control algorithms, it is possible to effectively implement it in real-time platform based on Field Programmable Logic Array (FPGA) / Digital Signal Processor (DSP).

The objective of this doctoral Thesis is to propose real-time control algorithm, which exhibits superior properties in terms of selected quality indicators – especially parameters related to the quality of the output voltage. The realization of a very fast and complex control scheme requires very fast computation unit. The greatest opportunities of an ultra fast and complex signal processing are given by reconfigurable devices, like FPGA, which allows for parallel hardware algorithms implementation. The hardware realization of algorithms in FPGA is a great challenge and is subjected to a number of restriction:

the propagation times of signals in the device, a limited number of macrocells, long time of structure synthesis, difficulties of system integration etc.

In year 2016 many controllers for switching-mode power supplies are still realized in analog technique, using operational amplifiers and passive components (e.g. power supply units in personal computers). Analog electronics in control systems offer many advantages, like wide bandwidth, continuous-time design, maintainability, fast reaction time and low price. Nevertheless, analog signals are susceptible to noise and a desirable operating point varies with temperature. Moreover, analog control circuits are very difficult to tune or adapt. The implementation of high-order, complex linear system in analogue manner can be difficult. Therefore, the analog technology of controllers is dominated by very simple control systems, like PI controller or lead-lag compensator. If it was possible to develop and apply cost-effective digital control system with robust and optimized control algorithms, then so common analog control circuit of power electronic converters might be displaced in the future.

1.2 Thesis structure

The content of this Thesis is organized in two main parts. The first part provides theoretical analysis and derivation of models of the selected power-electronic converters. The second part contains design and practical realization of digital control system for one selected converter topology.

Chapter 1 is an introduction to the subject of control of power electronic converters. It defines motivation, objective, the primary theses, scientific contribution and presents the state of the art.

Chapter 2 explains the basics of power processing for selected switching-mode converters. General information about common converter structures are presented. The chapter introduces the theory of a buck converter circuit operation. Moreover, it contains characteristics and the mathematical models of the selected converters.

Chapter 3 describes the principal algorithms of the digital control system. Analog-to-digital conversion, switching-ripple suppression digital filters, robust control algorithms and modulation techniques are thoroughly analyzed.

The second part of the Thesis is focused on the analysis of the control methods for selected structure – buck converter topology. Chapter 4 explains in details step-by-step the design of digital control algorithms described in the previous chapter. Finally, it contains results of experiments on a real system, carried out in order to verify designed control algorithms.

The conclusions of the Thesis and possible directions for further work are presented in chapter 5. Bibliography and appendices form the last part of the Thesis.

1.3 Scientific contribution of the Thesis

The Author considers selected parts of the work as his scientific contribution of this Thesis. The main contributions concern the following:

1. Comparison study of selected digital modulation algorithms and their evaluation for selected quality indicators. The comparison includes classical digital realization of Pulse Width Modulator (PWM) and Delta Modulator (DM).
2. Design, development and realization of a reconfigurable digital control system dedicated for driving switching-mode power converters including custom digital signal processing units realized in FPGA technology. The Author has designed hardware (including i.a. analog circuits for signal conditioning, analog-to-digital conversion, fiber-optic digital signal transmission), as well as firmware of the device.
3. Development of simulation models and environment.
4. Simulation studies and numerical verification of the developed control algorithms.
5. Design and verification of two linear controllers for selected case study: lead-lag compensator and $\mathcal{H}_\infty$ controller.
6. Comparison study of selected robust control algorithms designed for electronic switching power converters and their applicability for selected topologies of converters.
7. Design, development and realization of a buck converter working with digital control system for comparing properties of control system design, as an experimental unit for conducting and verification of the proposed control algorithms.
8. Implementation of selected signal processing algorithms in FPGA and experimental evaluation of their performance.
9. A dedicated test bench developed for measurement of transient responses (step) and voltage spectrum analysis (PSRR measurement).
10. A dedicated test bench developed for measurement of performance during load variations.
11. A dedicated test bench developed for measurement of frequency responses.

1.4 State of the art

The effective power processing based on the switching power converters is present in industrial applications and consumer electronics since the beginning of 1970s. The increased interest in switching-mode converters was associated mainly with the development of semiconductor technology. However, the switching power converters were also used before silicon revolution – mainly thanks to vacuum tubes technology and electromechanical relays. The principles of switching power supplies were known since the 1930s [10].

The great increase of efficiency came in the end of 1980 decade, since the Field Effect Transistor (FET) started replacing bipolar transistors. FETs provided lower conduction and switching losses and were able to switch at higher frequencies. Since that time, many innovative integrated circuits to control switching power supplies have appeared on the market. One of the most famous monolithic integrated circuit for regulating switching converters with Pulse Width Modulator (PWM) is SG1524. The inventor of this circuit, Robert Mammano was awarded in 2005 for a huge contribution to the development of integrated switching converter controllers discipline [47]. Another big step in high-effective power processing applications was done recently by improvement of Silicon-Carbide (SiC) and Gallium-Nitride (GaN) semiconductors, which offer very low resistance and allows for high frequency switching.

The SG1524 integrated circuit was an inspiration for many researchers to develop more complex and powerful silicon structures. Since the power semiconductor have been able to switch much faster and have become easily available, switching power converters started to be very popular [61]. However, nowadays the majority of control systems in power processing units, especially in area of switching-mode power supplies are still entirely based on the analog technology.

On the other hand, for the last 30 years the digital control methods have become popular in motor drives application or three-phase power converters for utility interfaces [41]. The control system in that application is very often realized using microcontrollers, digital signal processors or programmable logic devices. Despite the complexity of algorithms in such applications, the switching frequency does not exceed few tens of kilohertz. The conclusions of the paper [41] forecast the increased interest in digital control technology in high-frequency power electronic applications, such as DC-DC converters, switching mode power supplies, power factor correction rectifiers or electronic ballasts.

Digital realizations of fast responding controllers have been possible mainly due to the accessibility of accelerated signal processing devices, like reconfigurable circuits (commercially available FPGA devices have been offered by Xilinx Inc. since 1984 [57]) and DSP (Texas Instruments introduced successful and widely utilized TMS32010 fixed-point signal processor in 1983). The hardware acceleration gave a great opportunity for reducing the cycle time of control algorithms.

In [58] the author proposed a robust digital voltage-mode controller for soft-switching boost converter. In the paper the author have identified the proposed plant obtaining discrete transfer function. Then a simple second order digital compensator was proposed to receive a closed-loop system with gain margin of 10.9 dB and phase margin of 70°.

The design and implementation of a nonlinear model reference adaptive control applied to a three-phase three-level boost rectifier was extensively described in work [62]. The authors realized complex digital control algorithm utilizing universal dSPACE platform DS1104.

Selected types of predictive control methods used in power electronic applications and drives were revised in [14]. The author highlights that using predictive controllers one can take the advantage of the discrete nature of the switching power converters and choose from the possible switching states the optimal solution according to the minimization of predefined cost function.

The first known to the Author application of $\mathcal{H}_\infty$ robust control technique for power processing system was described in [32] in 1999. That controller was realized practically in analog scheme using the cascade of active filters based on the operational amplifiers, shown in Fig. 1.2. Furthermore, the performance of $\mathcal{H}_\infty$ method was compared with a linear-quadratic regulator scheme (LQR).

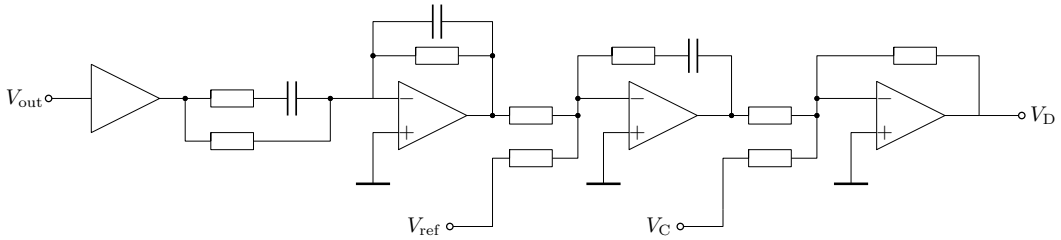


Figure 1.2: 4^{th} order $\mathcal{H}_\infty$ controller realized in analog scheme [32]

Another theoretical research regarding $\mathcal{H}_\infty$ in power electronic application was carried out and summarized in [60]. The authors have designed and performed simulation analysis of combined $\mathcal{H}_\infty$ compensator and repetitive controller for a power grid single-phase inverter.

Publication [23] presents custom optimization algorithm that minimizes the transient response of a voltage under current step change.

Doctoral thesis [1] is focused on optimizing energy conversion efficiency of a boost converter. The work covers numerous control methods including adaptation techniques, non-linear controllers and various optimization methods. Unfortunately, only simulation studies are presented in the thesis [1].

2

Power Converter Models

In this chapter the ideal mathematical models of the selected power electronic converters are introduced. The converters dynamic is described by means of linear equations. In general, most of real physical systems are nonlinear. Especially, the concept of linearity requires all state variables, inputs and output signals to be unbounded, which is never met in practical applications. On the other hand, linear models can be used in many cases to characterize the system in a certain operating range. The advantages of linear models include well developed mathematical apparatus, especially stability analysis methods. For the purpose of this chapter, the following equations describing the dynamic behavior of the system are considered

$$\begin{aligned} \frac{\mathrm{d}x(t)}{\mathrm{d}t} &= f\left(x(t), u(t), t\right), \\ y(t) &= h\left(x(t), u(t), t\right), \end{aligned} \tag{2.1}$$

where $x \in \mathbb{R}^n$, $u \in \mathbb{R}^p$ and $y \in \mathbb{R}^q$, $t \geq 0$, $x(0) = x_0$ and functions f and h are linear. The general form of a linear state space system can be also rewritten using state space matrices

$$\begin{aligned} \frac{\mathrm{d}x(t)}{\mathrm{d}t} &= \mathbf{A}x(t) + \mathbf{B}u(t), \\ y(t) &= \mathbf{C}x(t) + \mathbf{D}u(t), \end{aligned} \tag{2.2}$$

where $\mathbf{A} \in \mathbb{R}^{n \times n}$ is called the state (or system) matrix, $\mathbf{B} \in \mathbb{R}^{n \times p}$ is called the input matrix, $\mathbf{C} \in \mathbb{R}^{q \times n}$ is called the output matrix and $\mathbf{D} \in \mathbb{R}^{q \times p}$ is called the feedforward (or feedthrough) matrix.

After transformation from continuous-time domain to discrete-time domain, the time-invariant system can be described by the difference equations

$$\begin{aligned} x\left(T(k+1)\right) &= \mathbf{\Phi}x(kT) + \mathbf{\Gamma}u(kT), \\ y(kT) &= \mathbf{C}x(kT) + \mathbf{D}u(kT), \end{aligned} \tag{2.3}$$

where $\mathbf{\Phi} \in \mathbb{R}^{n\times n}$ is called the discrete state matrix and $\mathbf{\Gamma} \in \mathbb{R}^{n\times p}$ is called the discrete input matrix. The discrete-time state matrix is the state-transition matrix for the continuous-time system evaluated at the sampling period $T > 0$ [22].

2.1 Topologies and applications

Power processing systems usually can be classified into a few categories. Each of them can be classified in accordance with the voltage waveforms of input and output signals. Four basic blocks (Fig. 2.1) are:

- AC to AC (transformer, cycloconverter)
- AC to DC (rectifier)
- DC to AC (inverter)
- DC to DC (chopper)

(a) (b) (c) (d)

Figure 2.1: Basic types of converters: a – AC to AC, b – AC to DC, c – DC to AC, d – DC to DC

This thesis is devoted to fully controlled power converters which, in addition to power processing systems, include measuring and control systems. The controller may adjust output voltage, output current, frequency or phase by driving power switches.

Power electronic converters make use of semiconductor devices which operate in switching mode instead of linear mode. Switching mode converters allow to greatly reduce conversion losses and the efficiency is essential for power processing systems. The ideal switch operates in two states: the "off" state, when the current through the switch i_s is zero and the "on" state, when the current flow through the switch but voltage on a switch u_s is zero. In both cases it is assumed that the power losses of the ideal switch, expressed as $P_s = i_\mathrm{s}u_\mathrm{s}$, are zero (see Fig. 2.2).

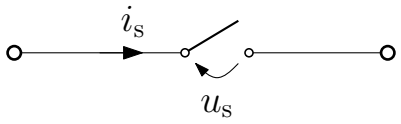


Figure 2.2: Model of ideal switch

Some models in this Thesis refer to the ideal switch model. However, nowadays the switch is realized using a semiconductor device. Symbols of basic semiconductor devices that can be found in switching-mode converters are shown in Fig. 2.3. Semiconductor switches can be classified with regard to their ability of control. One can distinguish uncontrolled switches, semi-controlled switches and fully controlled switches. They can be also classified regarding the direction of the current through the device and the polarity of the voltage that the device can block. The semiconductor characteristic can be presented by quadrant operation. Power switches can operate in one quadrant, two quadrants or four quadrants. The idealized characteristics of basic types of semiconductor are shown Fig. 2.4. Diodes (Fig. 2.3a) operate in the second quadrant (Fig. 2.4A), BJTs (Fig. 2.3d), JFETs (Fig. 2.3e) and MOSFETs (Fig. 2.3g) typically operate in the first quadrant (Fig. 2.4B), thyristors (Fig. 2.3b), IGBTs (Fig. 2.3h), MCTs (Fig. 2.3f) and GTOs (Fig. 2.3i) typically operate in the first and second quadrants (Fig. 2.4C) and TRIACs (Fig. 2.3c) operate in all four quadrants (Fig. 2.4D).

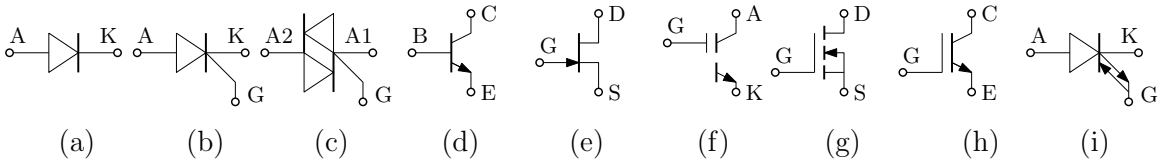


Figure 2.3: Basic types of semiconductor switches. Uncontrolled switches: a – diode. Semi-controlled switches: b – thyristor (SCR); c – triac. Fully controlled switches: d – Bipolar Junction Transistor (BJT); e – Junction gate Field Effect Transistor (JFET); f – Metal-oxide-semiconductor Controlled Thyristor (MCT); g – Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET); h – Insulated Gate Bipolar Transistor (IGBT); i – Gate Turn-Off thyristor (GTO)

The choice of controllable switches is usually limited not only by operating quadrant but also by the specified voltage and current through the semiconductor device and the specified switching frequency. The capabilities of modern semiconductor switches are presented in Fig. 2.5. The power transistor in switching-mode converters operates only in either the cutoff or saturated mode [61].

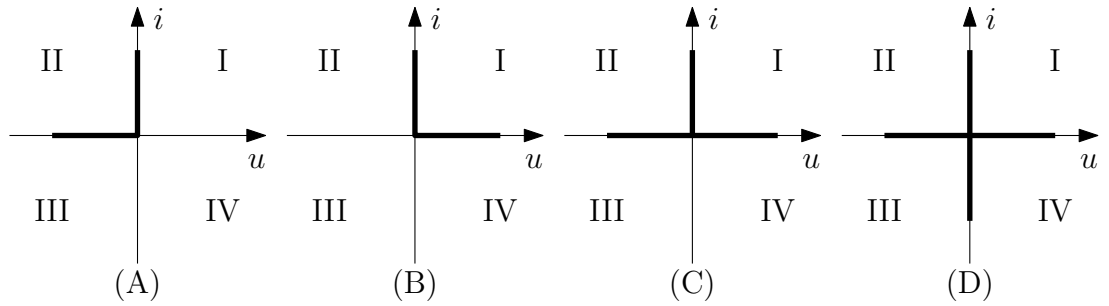


Figure 2.4: Idealized switch characteristics of semiconductor elements. A – the second quadrant device; B – the first quadrant device; C – two quadrant device; D – four quadrant device

2.2 Buck converter

One of the simplest switching-mode converters, used for generating a lower output DC voltage from higher DC input voltage is called 'Buck converter'. In this section, a simplified model of buck converter is presented. The model is only approximate reflection of reality and does not take into account all converter loss elements except inductor series resistance. The accuracy of analyzed model is not sufficient for efficiency estimation, but is suitable for control system design.

The model of the buck converter circuit is shown in Fig. 2.6. The circuit includes two-state switch S, two energy storage: inductor L and capacitor C, a DC voltage source U_g and resistors which represent loss elements and load. The energy is transferred in one direction – from the voltage source U_g to the load. A switch S operates between two states: 1 and 2. Let us assume, that the switch position varies periodically with a constant switching frequency f_s. It is further assumed for the model, that the switch reaches each state instantly. Hence, a switching period can be expressed as $T_\mathrm{s} = 1/f_\mathrm{s}$. The duty cycle D is defined as the ratio between the time spend in state 1 (time t_1) and the switching period (T_s)

$$D = \frac{t_1}{t_1 + t_2} = \frac{t_1}{T_\mathrm{s}}, \qquad D \in [0, 1], \tag{2.4}$$

From Fourier analysis one can know that the DC component of a periodic function $g(t)$ with period T_s is equal to its average value

$$\langle g(t) \rangle_{T_\mathrm{s}} = \frac{1}{T_\mathrm{s}} \int_{t-T_\mathrm{s}}^{t} g(t)\mathrm{d}t, \tag{2.5}$$

where $\langle \cdot \rangle_{T_\mathrm{s}}$ denotes the average of signal over time T_s. Hence, from steady-state analysis it can be shown, that for considered model, the DC component of output voltage u_C

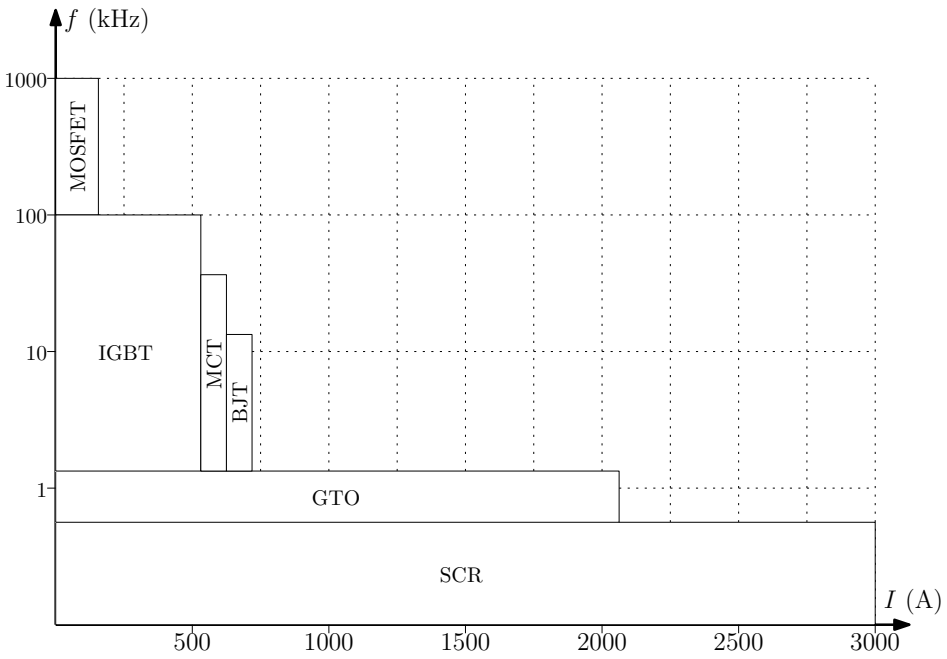


Figure 2.5: The comparison of maximal switching frequency and current of various semiconductor switches (based on [51])

averaged over switching period T_s can be expressed as follows

$$U_\mathrm{C} = \langle u_\mathrm{C} \rangle_{T_\mathrm{s}} = U_\mathrm{g}\, D \frac{R_\mathrm{o}}{R_\mathrm{L} + R_\mathrm{o}}, \tag{2.6}$$

where R_o is the load resistance, R_L is the parasitic series resistance of the inductor L (which is related to the copper losses of the inductor) and U_g denotes the input DC voltage. The capacitor voltage u_C in Fig. 2.6 is the output voltage as well.

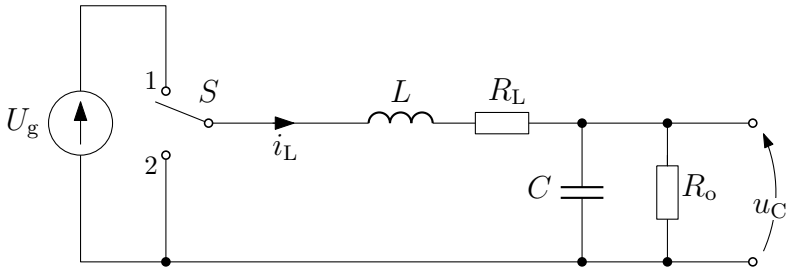


Figure 2.6: Buck converter power-stage circuit diagram

2.2.1 Linear time-invariant dynamic model

From (eq. 2.6) it can be seen, that the algebraic relation between average voltage $\langle u_C \rangle_{T_s}$ and the duty cycle D can be used for achieving demanded output voltage. A steady-state linear characteristic of the output voltage against duty cycle is shown in Fig. 2.7. The characteristic does not describe the exact input-output behavior of the buck converter since the operating modes are not considered yet (they will be described further in the section 2.2.4).

It is obvious, since the duty cycle D is bounded and is defined over the [0, 1] interval, that the averaged output voltage $\langle u_C \rangle_{T_s}$ is always less than or equal to the input voltage U_g.

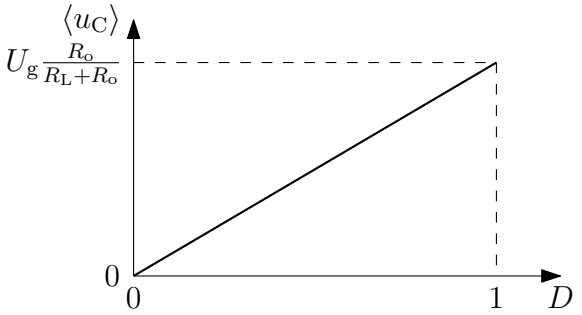


Figure 2.7: Buck converter steady-state control characteristic

The inductor L and the capacitor C form a lowpass filter designed to pass the DC component U_C and attenuate the fundamental switching frequency component $u_{ripple}(t)$ and its harmonics [21]. Let us assume that the capacitor voltage $u_C(t)$ consists of two components: DC voltage U_C and attenuated switching voltage $u_{ripple}(t)$

$$u_C(t) = U_C + u_{ripple}(t). \tag{2.7}$$

In a well-designed power converter, the magnitude of voltage $u_{ripple}(t)$ arised from switching harmonics is much smaller then the DC output voltage U_C

$$\|u_{ripple}\| = \Delta u_C \ll U_C. \tag{2.8}$$

In such case, the output voltage ripples do not have to be considered in calculation – this method is known as the small-ripple approximation.

Hence, the dynamics of the second-order system in Fig. 2.6 can be approximately modeled through the use of ordinary linear differential equations

$$\begin{cases} \dfrac{\mathrm{d}\langle i_L(t)\rangle_{T_s}}{\mathrm{d}t} = \dfrac{1}{L}\big(D\,U_g - \langle i_L(t)\rangle_{T_s} R_L - \langle u_C(t)\rangle_{T_s}\big) \\ \dfrac{\mathrm{d}\langle u_C(t)\rangle_{T_s}}{\mathrm{d}t} = \dfrac{1}{C}\left(\langle i_L(t)\rangle_{T_s} - \dfrac{\langle u_C(t)\rangle_{T_s}}{R_o}\right) \end{cases} \tag{2.9}$$

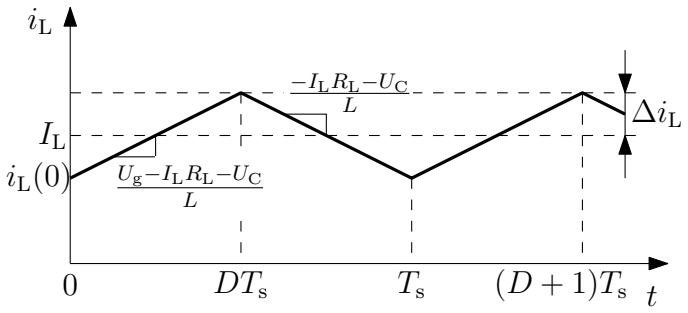


Figure 2.8: Inductor current waveform in steady-state (based on [21])

The simplified waveform of inductor current which highlights DC component I_L and switching ripple component $i_\mathrm{ripple}(t)$ in steady-state[1] is shown in Fig. 2.8. The amplitude of ripple current is denoted by Δi_L and can be expressed as

$$\Delta i_\mathrm{L} = \frac{U_\mathrm{g} - I_\mathrm{L}R_\mathrm{L} - U_\mathrm{C}}{2L} DT_\mathrm{s} \tag{2.10}$$

Hence, the Root Mean Square (RMS) current through the inductor is equal to

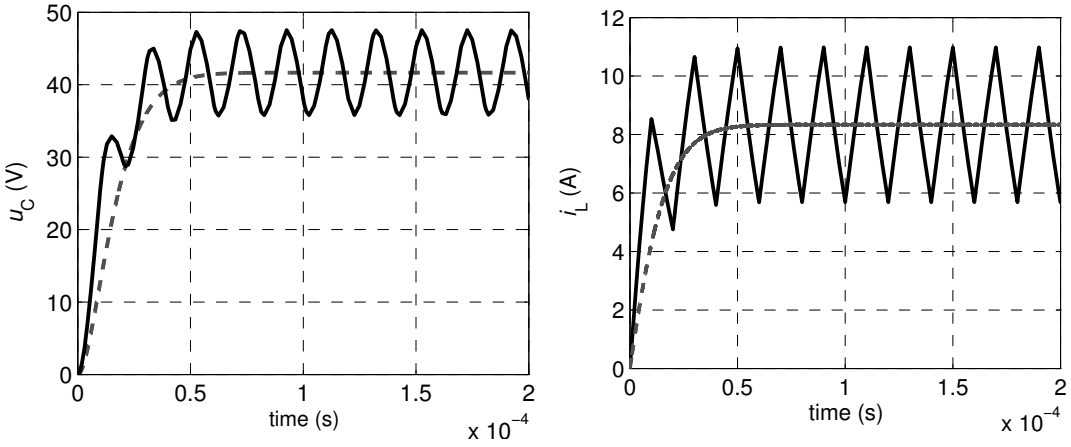
$$i_\mathrm{LRMS} = \sqrt{\frac{1}{T_\mathrm{s}} \int_0^{T_\mathrm{s}} {i_\mathrm{L}}^2 \mathrm{d}t} = I_\mathrm{L} + \frac{\Delta i_\mathrm{L}}{\sqrt{3}}. \tag{2.11}$$

The step response of the output voltage u_C and the inductor current i_L for D changing from 0 to 0.5 is shown in Fig. 2.9. As can be seen from the figure, the rectangular waveform of the voltage that supply inductor L effects in "triangular" inductor current waveform (b) and quadratic output voltage waveform (a). Precisely, the inductor current waveform is not triangular but it can be described by exponential function, that come from solving the differential equations (eq. 2.9) (further discussed in sec. 3.2). However, the triangular waveform of inductor current is usually sufficient approximation for small-ripple case.

2.2.2 State space representation

The system described by ordinary differential equations (eq. 2.9) can be converted into the standard linear state space representation, by defining the following variables. The averaged inductor current $\langle i_\mathrm{L} \rangle_{T_\mathrm{s}}$ and the averaged capacitor voltage $\langle u_\mathrm{C} \rangle_{T_\mathrm{s}}$ form

[1] The 'steady-state' term in control theory reflects the condition of the system, where the state vector remains constant with $\frac{\mathrm{d}\mathbf{x}(t)}{\mathrm{d}t} = 0$. Although, in case of switching converters the instantaneous values of capacitor voltage u_C and inductive current i_L are changing in time, their averaged values U_C and I_L do not vary in time in steady-state.



(a) (b)

Figure 2.9: The Step response of a – an output voltage u_{C}, b – an inductor current i_{L}, for the duty cycle step from 0 to 0.5. The dashed lines correspond to the averaged voltage $\langle u_{\mathrm{C}}\rangle_{T_{\mathrm{s}}}$ and the averaged current $\langle i_{\mathrm{L}}\rangle_{T_{\mathrm{s}}}$, while the solid lines emphasize ripple voltage and current for $f_{\mathrm{s}} = 50$ kHz, $U_{\mathrm{g}} = 100$ V

a state vector x. The duty cycle D is defined as an input to the system and the averaged capacitor voltage $\langle u_{\mathrm{C}}\rangle_{T_{\mathrm{s}}}$ as a system output

$$x = \begin{bmatrix} \langle i_{\mathrm{L}}\rangle_{T_{\mathrm{s}}} \\ \langle u_{\mathrm{C}}\rangle_{T_{\mathrm{s}}} \end{bmatrix}, \qquad u = D, \qquad y = \langle u_{\mathrm{C}}\rangle_{T_{\mathrm{s}}}. \tag{2.12}$$

The system can be described by the following linear state space form

$$\begin{cases} \dot{x} = \mathbf{A}x + \mathbf{B}u \\ y = \mathbf{C}x \end{cases}, \tag{2.13}$$

where state-space matrices $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$ are defined as follows

$$\begin{aligned} \mathbf{A} &= \begin{bmatrix} -R_{\mathrm{L}}/L & -1/L \\ 1/C & -1/(CR_{\mathrm{o}}) \end{bmatrix} \qquad \mathbf{B} = \begin{bmatrix} U_{\mathrm{g}}/L \\ 0 \end{bmatrix} \\ \mathbf{C} &= \begin{bmatrix} 0 & 1 \end{bmatrix} \end{aligned} \tag{2.14}$$

Assuming positive values of L, C, R_{L} and R_{o} the system is globally asymptotically stable, since the characteristic polynomial has two roots $\lambda_{1,2}$ (eigenvalues of matrix $\mathbf{A}$) in the left-hand side of the s-plane

$$\lambda(\mathbf{A}) = \{s \in \mathbb{C} : \det(s\mathbf{I} - \mathbf{A}) = 0\} \tag{2.15}$$

$$\alpha = \frac{CR_{\mathrm{o}}R_{\mathrm{L}} + L}{CLR_{\mathrm{o}}} \qquad \lambda_{1,2} = -\frac{1}{2}\alpha \pm \frac{1}{2}\sqrt{\alpha^2 - 4\frac{R_{\mathrm{L}} + R_{\mathrm{o}}}{CLR_{\mathrm{o}}}} < 0 \tag{2.16}$$

Trajectories of the system head toward steady-state point, where voltage $\langle u_{\mathrm{C}}\rangle_{T_{\mathrm{s}}}$ and current $\langle i_{\mathrm{L}}\rangle_{T_{\mathrm{s}}}$ remain constant. This asymptotically stable equilibrium point x_{e} can be found by substituting right-hand side of equations (eq. 2.9) with zero $\dot{x} \equiv 0$

$$x_{\mathrm{e}} = \begin{bmatrix} \dfrac{D\,U_{\mathrm{g}}}{R_{\mathrm{L}} + R_{\mathrm{o}}} \\ \dfrac{D\,U_{\mathrm{g}}\,R_{\mathrm{o}}}{R_{\mathrm{L}} + R_{\mathrm{o}}} \end{bmatrix}. \tag{2.17}$$

When the system reaches the equilibrium point x_{e}, it stays at x_{e} until the input value D, the load resistance R_{o} or any other parameter is changed or the disturbance occurs [44]. The behavior of system can be investigated by plotting typical trajectories in the state space. This can be observed in a phase portrait in Fig. 2.10.

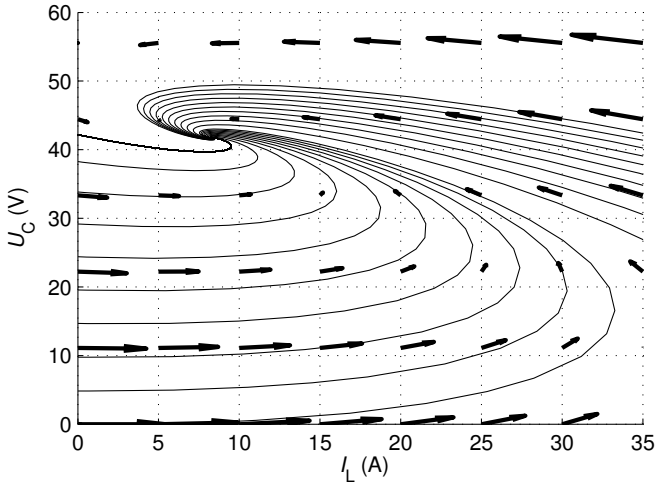


Figure 2.10: Phase portrait of buck converter linear model for a set of initial conditions ($U_{\mathrm{g}} = 100\,\mathrm{V}$, $D = 0.5$). Phase portrait can be classified as nodal sink type (when eigenvalues are real and negative) or spiral sink type (when eigenvalues are complex with negative real part)

2.2.3 Transfer function representation

A general state space model can be converted to transfer function form using the following formula:

$$\mathbf{G}(s) = \mathbf{C}\,(s\mathbf{I} - \mathbf{A})^{-1}\,\mathbf{B}, \tag{2.18}$$

The SIMO (Single-Input Multiple-Output) model described by (eq. 2.14), can be converted into transfer function matrix $\mathbf{G}(s)_{[2\times1]}$.

$$\mathbf{G}(s) = \begin{bmatrix} G_{\mathrm{ID}}(s) \\ G_{\mathrm{UD}}(s) \end{bmatrix} \tag{2.19}$$

Let us consider the second transfer function G_{UD}, which describes the relation between duty cycle D and output voltage $\langle u_{\mathrm{C}} \rangle_{T_{\mathrm{s}}}$

$$G_{\mathrm{UD}}(s) = \frac{U_{\mathrm{C}}(s)}{D(s)} = \frac{U_{\mathrm{g}}\, R_{\mathrm{o}}}{CLR_{\mathrm{o}}s^2 + (CR_{\mathrm{L}}R_{\mathrm{o}} + L)\, s + R_{\mathrm{L}} + R_{\mathrm{o}}}. \tag{2.20}$$

Let us substitute the following constants:

$$G_{d0} = \frac{U_{\mathrm{g}}\, R_{\mathrm{o}}}{R_{\mathrm{L}} + R_{\mathrm{o}}}, \qquad \omega_0 = \frac{1}{\sqrt{L\,C}}, \qquad Q = (R_{\mathrm{L}} + R_{\mathrm{o}})\, \frac{\sqrt{\frac{R_{\mathrm{o}}\, L\, C}{R_{\mathrm{L}} + R_{\mathrm{o}}}}}{CR_{\mathrm{L}}R_{\mathrm{o}} + L}, \tag{2.21}$$

where ω_0 denotes the undamped natural frequency of the system and Q is the quality factor defined as the ratio of the energy stored to the energy dissipated in the circuit per cycle by damping process [3].

$$G_{\mathrm{UD}}(s) = \frac{G_{d0}}{\frac{1}{\omega_0^2}s^2 + \frac{1}{Q\omega_0}s + 1}. \tag{2.22}$$

The equation (eq. 2.22) is a standard normalized form of a two-pole resonator transfer function. The effect of quality factor Q on the shape of frequency response is illustrated in Fig. 2.11. It can be noticed that the resonance peak (observed for $Q > 0.5$) increases with increasing Q. The magnitude at the natural frequency ω_0 is equal to the product of DC-gain component G_{d0} and Q-factor value.

$$|G(j\omega_0)| = |G_{d0}| \cdot Q. \tag{2.23}$$

The notation (eq. 2.22) is equivalent to the canonical form for a second-order homogeneous system with damping coefficient ζ

$$G_{\mathrm{UD}}(s) = \frac{G_{d0}}{\frac{1}{\omega_0^2}s^2 + \frac{2\zeta}{\omega_0}s + 1}, \tag{2.24}$$

where $\zeta = \frac{1}{2Q}$. The oscillatory properties of the system can be observed, when $Q > 0.5$ or $\zeta < 1$ (complex poles). Higher value of Q causes the rapid change of the phase response, which tend towards $-180°$ lag. These properties are well illustrated in Fig. 2.11. One can notice that the buck converter system is always stable, since the damping coefficient ζ is in practice always greater than 0.

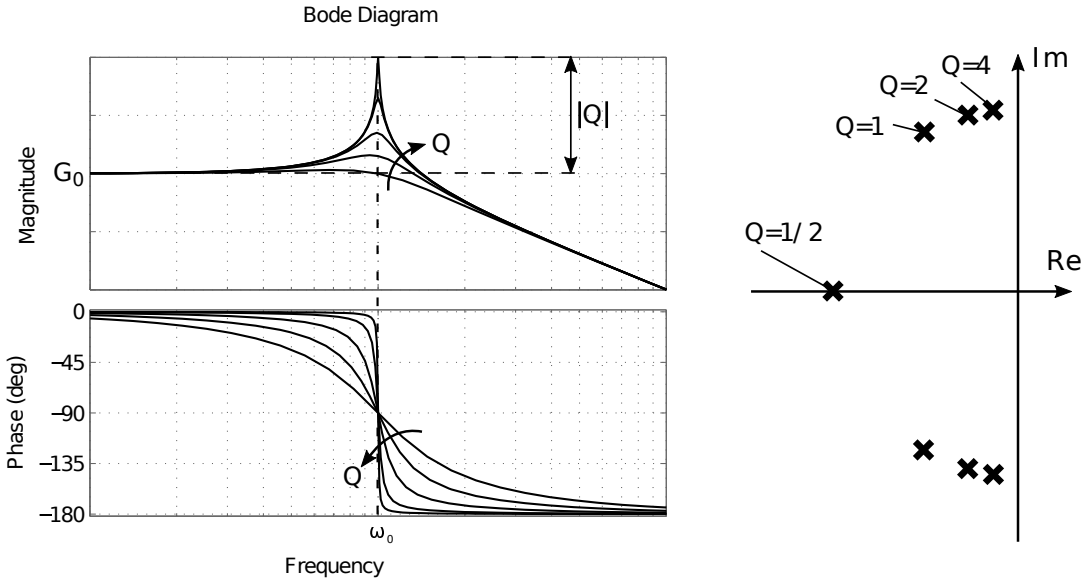


Figure 2.11: Frequency response of quadratic pole system, a – Bode characteristic, b – pole locations on a complex plane (based on [6])

2.2.4 Output filter design

The output filter of the buck converter is composed of two reactive elements: inductor and capacitor. The effectiveness of power conversion rely on relatively low dissipation of power in the output filter. However, the LC filter needs to be always terminated by the load resistance R_o to operate properly [42]. Therefore, the filter has to be always designed with respect to the specified load resistance value.

To discuss the principles of output filter design, firstly operation modes need to be introduced. Buck converter can operate in two basic modes, with respect to inductor current waveform:

- Continuous Conduction Mode (CCM),
- Discontinuous Conduction Mode (DCM).

In CCM operation mode the inductor current i_L never reaches zero, while in DCM operation mode the inductor current i_L is zero for certain time in every switching cycle. In principle, the operation mode can be determined by the amplitude of the ripple current

Δi_{L} [21]

$$\begin{aligned} I_{\mathrm{L}} > \Delta i_{\mathrm{L}} &\longrightarrow \text{CCM} \\ I_{\mathrm{L}} < \Delta i_{\mathrm{L}} &\longrightarrow \text{DCM}. \end{aligned} \tag{2.25}$$

Hence, the following condition for operation in continuous conduction mode can be formulated, by substituting equations (eq. 2.10) and (eq. 2.17)

$$\frac{DU_{\mathrm{g}}}{R_{\mathrm{L}} + R_{\mathrm{o}}} > \frac{U_{\mathrm{g}} - I_{\mathrm{L}}R_{\mathrm{L}} - U_{\mathrm{C}}}{2L} DT_{\mathrm{s}} = \frac{U_{\mathrm{g}} - I_{\mathrm{L}}R_{\mathrm{L}} - U_{\mathrm{g}}D\frac{R_{\mathrm{o}}}{R_{\mathrm{L}}+R_{\mathrm{o}}}}{2L} DT_{\mathrm{s}}. \tag{2.26}$$

The above inequality can be simplified to

$$\frac{2L}{(R_{\mathrm{L}} + R_{\mathrm{o}})T_{\mathrm{s}}} > 1 - \frac{I_{\mathrm{L}}R_{\mathrm{L}}}{U_{\mathrm{g}}} - D\frac{R_{\mathrm{o}}}{R_{\mathrm{L}} + R_{\mathrm{o}}}. \tag{2.27}$$

In most cases the operation in CCM is advisable, due to linear model describing the behavior of the system and insensitivity of output voltage u_{C} to the load R_{o}. Moreover, the Discontinuous Conduction Mode results in much higher disturbances and risk of Electromagnetic Compatibility (EMC) infringement, when current across the inductor reaches zero. This effect is illustrated in Fig. 2.12, where waveform of continuous and discontinuous operation are shown (waveforms based on experimental data). Increasing the inductance L or reducing the switching period T_{s} can move the operating conditions to CCM mode. However, most of power converters have to work in DCM at light load (high R_{o} value). To achieve CCM operation for target load resistance and obtain small current ripple amplitude, one have to design the output filter of the buck converter with large-enough inductance L or increase the switching frequency f_{s}. The value of inductance L can be chosen by specifying the desired amplitude of ripple current (solving eq. 2.10)

$$L \geq \frac{U_{\mathrm{g}} - I_{\mathrm{L}}R_{\mathrm{L}} - U_{\mathrm{C}}}{2\Delta i_{\mathrm{L}}} DT_{\mathrm{s}}. \tag{2.28}$$

The choice of inductance value is a trade-of between the magnitude of the ripple current and the weight and size of magnetic core. Usually, the acceptable ripple current magnitude Δi_{L} is specified as 10% to 20% of an average inductor current I_{L} (rule of thumb).

Analogically, the value of capacitance C can be selected by specifying the desired amplitude of ripple voltage Δu_{C}

$$C \geq \frac{U_{\mathrm{C}}}{2R_{\mathrm{o}}\Delta u_{\mathrm{C}}} DT_{\mathrm{s}}. \tag{2.29}$$

Generally, the acceptable magnitude of the ripple voltage is specified below 1% of an average output voltage U_{C} [21] (rule of thumb).

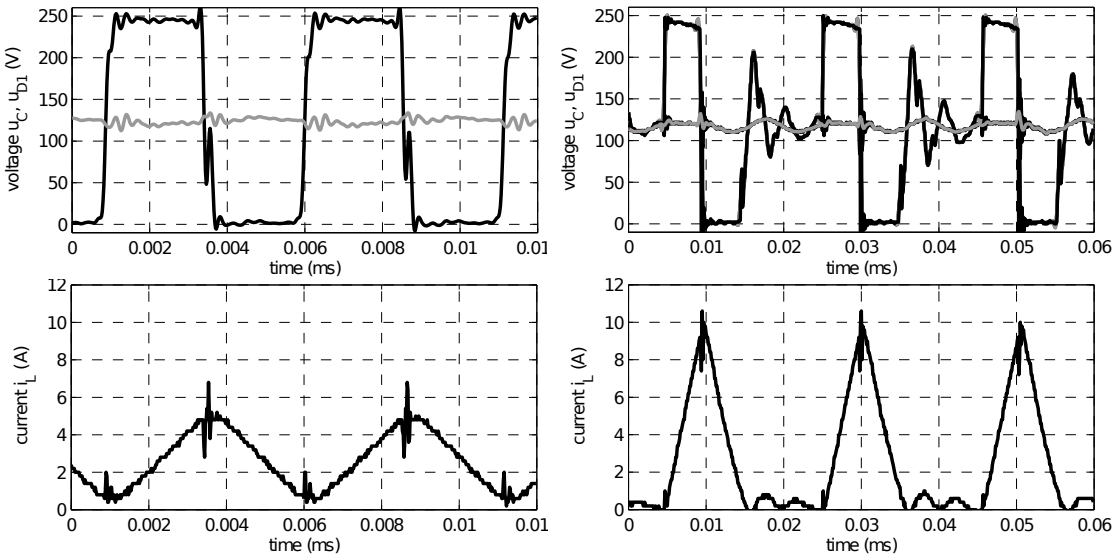


Figure 2.12: Examples of the waveforms of the buck converter in continuous conduction mode (a) and discontinuous conduction mode (b) (the gray line represent output voltage u_{C}, while the black line diode voltage u_{D1}). The converter entered DCM, when the switching frequency f_{s} was decreased from 200 kHz to 50 kHz. In consequence, when inductor current reaches 0 A, transient oscillations appear in both voltage and current waveforms. One can notice, that higher instantaneous inductive current are present in DCM for the same average current

2.2.5 Selection of semiconductor switches

Fig. 2.6 presents the model of a buck converter. In practical realization the ideal switch S has to be replaced with semiconductor devices. Two-state switch must be replaced with two separate semiconductor switches. The analysis of the current flow in the circuit helps in determination of operating points for the switches. One of them must block the positive voltage and conduct positive current, while the second one must block negative voltage and conduct positive current. Hence, the first switch operates in the first quadrant (Fig. 2.4B), and the second switch in the second quadrant (Fig. 2.4A). Thus, the list of semiconductors able to operate in the buck converter circuit is limited. One commonly chosen set of semiconductor devices that operates in correct quadrants in buck converter are MOSFET and diode, as it is shown in Fig. 2.13.

Another choice is to use two MOSFET transistors for synchronized switching. This approach substitutes the voltage drop on the diode for the voltage drop on a conducting

MOSFET equal to $U_{\mathrm{T}} = I_{\mathrm{L}} R_{\mathrm{DSon}}$, which is very important for low-voltage applications. R_{DSon} denotes the resistance of the MOSFET when the device is in linear region, while U_{T} denotes the voltage drop on the conducting transistor.

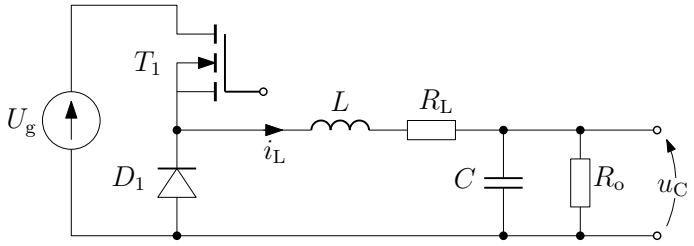


Figure 2.13: Example of the buck converter power-stage realization with MOSFET transistor and diode rectifier

2.3 First quadrant chopper DC motor drive

The analysis in sec. 2.2 concerns electric power conversion, where the lower output voltage is generated from a higher input voltage. However, the considered system and whole thesis has more universal nature. The proposed model can be applied in other types of conversion, i.e. where electric power is converted to mechanical power. In this section a converter for series wound DC motor drive is proposed. The series wound DC motor is a commutator-based machine with field winding and armature winding connected in series. The electrical diagram of series DC motor is shown in Fig. 2.14. To simplify the model, a field winding inductance L_{f} and an armature winding inductance L_{a} are added together and denoted by L_{m} as well as the sum of field winding resistance R_{f} and the armature winding resistance R_{a} is denoted by R_{m}.

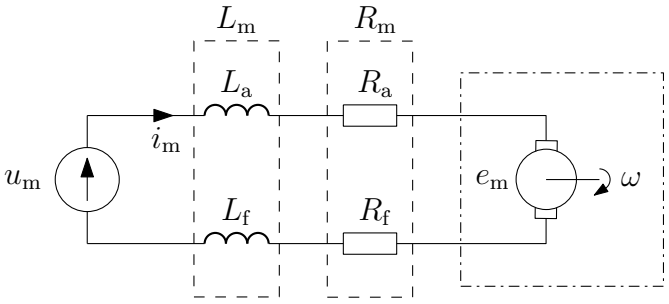


Figure 2.14: Electrical diagram of series excited DC motor

The mathematical model of a series excited DC motor can be described with the following nonlinear differential equations

$$\begin{cases} \dfrac{\mathrm{d}\left(L_\mathrm{a} i_\mathrm{m} + \Phi_\mathrm{f}(i_\mathrm{m})\right)}{\mathrm{d}t} = U_\mathrm{m} - i_\mathrm{m} R_\mathrm{m} - K_\mathrm{m} \Phi_\mathrm{f}(i_\mathrm{m})\omega \\ J\dfrac{\mathrm{d}\omega}{\mathrm{d}t} = K_\mathrm{m} \Phi_\mathrm{f}(i_\mathrm{m}) i_\mathrm{m} - B\omega - \tau_\mathrm{L} \end{cases} . \tag{2.30}$$

Assuming that the field circuit is not in magnetic saturation, the state equations (eq. 2.30) can be reformulated by linearization of simplified magnetization curve (see [43]). To take the advantage of a linear part of the magnetization curve it has to operate in a certain current range ($i_\mathrm{m} < I_\mathrm{m}$) (see Fig. 2.15).

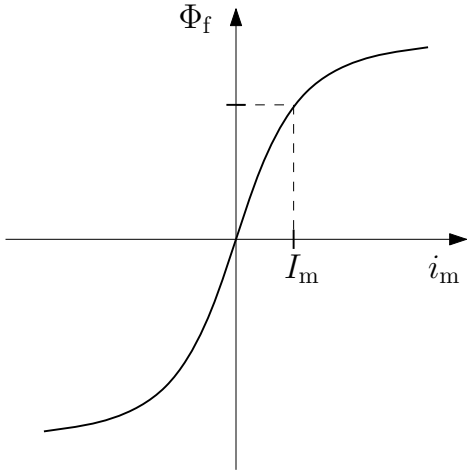


Figure 2.15: Simplified magnetization curve without hysteresis

Now, one can assume that field-excitation flux equals $\Phi_\mathrm{f}(i_\mathrm{m}) = L_\mathrm{f} i_\mathrm{m}$ [8]. The system from (eq. 2.30) reduces to

$$\begin{cases} \dfrac{\mathrm{d}i_\mathrm{m}(t)}{\mathrm{d}t} = \dfrac{1}{L_\mathrm{m}}\Big(U_\mathrm{m} - i_\mathrm{m}(t) R_\mathrm{m} - K_\mathrm{m} L_\mathrm{f} i_\mathrm{m}(t)\omega(t)\Big) \\ \dfrac{\mathrm{d}\omega(t)}{\mathrm{d}t} = \dfrac{1}{J}\Big(K_\mathrm{m} L_\mathrm{f} {i_\mathrm{m}}^2(t) - B\omega(t) - \tau_\mathrm{L}\Big) \end{cases} . \tag{2.31}$$

The angular velocity, a viscous friction coefficient and a load torque are denoted by ω, B and τ_L, respectively. The back electromotive force marked in the Fig. 2.14 as e_m can be expressed as the product of the angular rate ω, armature constant K_m, current i_m and field winding inductance L_f. One can notice that the second equation (eq. 2.31) is still nonlinear, since current i_m is raised to the second power.

Analogically as in buck converter diagram, the series DC motor can be connected to DC power supply by a switch (Fig. 2.16). Let us find some analogies between system

(eq. 2.31) and system (eq. 2.9). A moment of inertia of the shaft along its principle axis denoted by J replaces the capacitor C and the motor winding (field winding inductance L_f + armature winding inductance L_a) denoted by L_m replaces the inductor L in buck converter. Now, the input voltage U_m can be expressed as $D\,U_\mathrm{g}$. Once again, the average operator is applied to neglect the value changes over the single switching period T_s.

$$\begin{cases} \dfrac{\mathrm{d}\langle i_\mathrm{m}(t)\rangle_{T_\mathrm{s}}}{\mathrm{d}t} = \dfrac{1}{L_\mathrm{m}}\Big(D\,U_\mathrm{g} - \langle i_\mathrm{m}(t)\rangle_{T_\mathrm{s}} R_\mathrm{m} - K_\mathrm{m} L_\mathrm{f} \langle i_\mathrm{m}(t)\rangle_{T_\mathrm{s}} \langle \omega(t)\rangle_{T_\mathrm{s}}\Big) \\ \dfrac{\mathrm{d}\langle \omega(t)\rangle_{T_\mathrm{s}}}{\mathrm{d}t} = \dfrac{1}{J}\Big(K_\mathrm{m} L_\mathrm{f} \langle {i_\mathrm{m}}^2(t)\rangle_{T_\mathrm{s}} - B\langle \omega(t)\rangle_{T_\mathrm{s}} - \tau_\mathrm{L}\Big) \end{cases}. \tag{2.32}$$

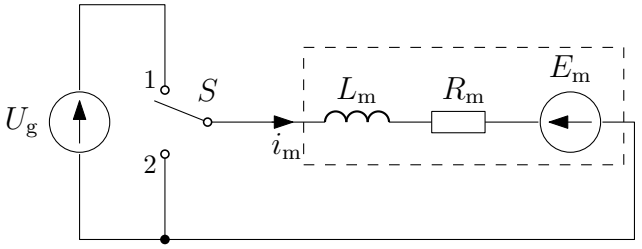


Figure 2.16: Electrical diagram of the first quadrant chopper DC motor drive

2.4 Quality of energy supply

One of the major goals in the design of power electronic converter is to achieve the assumed output power quality. It is important to define and specify the objective in terms of the voltage and current quality. The term power quality can refer to many aspects and requirements, where some of them are addressed in this Thesis:

- output voltage ripple,
- output current ripple,
- the ratio of the change in input supply voltage to the change in converter output voltage,
- overshoots and damping ratio at set-point variations,
- steady state error,
- voltage regulation at load current transients.

Voltage and current ripples depend only on the converter design – specified switching frequency, inductor and capacitor parameters. The other listed factors used to describe quality depend on the whole system including feedback control.

The ratio of the change in input supply voltage to the change of converter output voltage describes how much the input voltage variation affects the converter output. Unstable supply voltage, fluctuation in power grid or passive diode rectifier without sufficient ripple filter can greatly disturb the DC input voltage. When the discussed ratio is high, the disturbance do not impact much the converter output voltage. This ratio can be expressed for a specific single frequency or as a function for frequency range. In the literature one can find the term Power Supply Rejection Ratio (PSRR) [55], which is expressed in decibels and defined as follows

$$\mathrm{PSRR} = 20 \log_{10} \frac{\Delta V_{\mathrm{in}}}{\Delta V_{\mathrm{out}}}. \tag{2.33}$$

The next factor is related to a transient response, when set-point changes or disturbance occurs. The basic properties of step response are illustrated in Fig. 2.17. Properly designed controller responses to a transient quickly, with small overshoot and ringing. However, it is not easy to achieve low overshoot for the oscillatory character of the plant. The fastest response that contains neither overshoot nor ringing is associated with critical damping. Various controllers for fixed plant and the same test conditions can be compared against overshoot or settling time. Percent overshoot is defined as

$$\mathrm{PO} = \frac{\mathrm{peak}\, V_{\mathrm{out}} - V_{\mathrm{out}}(\infty)}{V_{\mathrm{out}}(\infty)} 100\%. \tag{2.34}$$

Settling time is defined as a the time required by the closed loop system output value to approach the final value (steady state) within some defined margin [54]. Both, overshoot and settling time depend on damping ratio of the system (commonly denoted by ζ). For power electronic converter applications it is usually preferred to exhibit no overshoot at the cost of larger settling time. This decay property can be achieved for overdamped system, when $\zeta > 1$.

The steady state error is a difference between demanded output voltage (or current) and its actual value in steady state

$$e_{\mathrm{ss}} = \lim_{t \to \infty} e(t). \tag{2.35}$$

In case when steady-state error exceeds the specified (expected) error in feedback system, the zero-frequency gain of controller needs to be increased.

The last specified factor concerns behavior of the system during load current variation. From the controller perspective, load changes are threated as disturbances. Hence, the

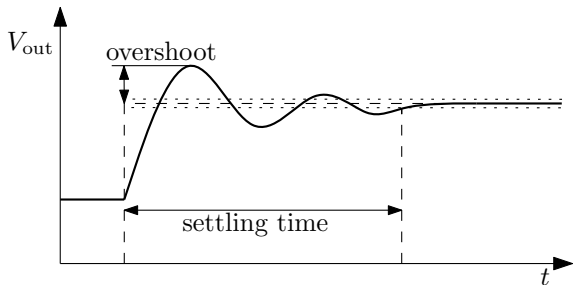


Figure 2.17: Transient response to a step excitation

analysis can be similar as in the case of set-point variations – including assessment of overshoot and settling time.

3

Digital Control Techniques for Power Converters

The digital feedback control system for power converter can be typically divided into the following function blocks arranged here in the order of signal flow:

1. Analog signal conditioning and analog-to-digital converter,
2. Digital filter,
3. Compensator,
4. Modulator.

The simplified block diagram of a basic control signal processing is shown in Fig. 3.1. Each block plays an important role in the performance of a control system. Analog to digital converter takes care of the proper representation of analog signal in digital memory. Digital filter suppresses undesired switching ripples and averages the signal. The feedback linear controller (or compensator, denoted in Fig. 3.1 by $G_{\mathrm{c}}(z)$) regulates the output of the power converter $\langle y[n] \rangle_{T_s}$ to track the reference input $u_{\mathrm{ref}}[n]$ in the presence of measurement noise, disturbances and uncertainty in process dynamics [6]. Modulator transforms the discrete signal into the binary space to drive gates of power switches. The plant (power converter) is denoted in the figure by $P(s)$.

In addition to control algorithm, there are many aspects that need to be considered before implementing controller in a digital manner, with the most important being [33]:

- sampling rate,

- analog-to-digital conversion,
- floating point or fixed point arithmetics,
- word length,
- memory requirements,
- computational delay,
- controller realization,
- anti-windup mechanism.

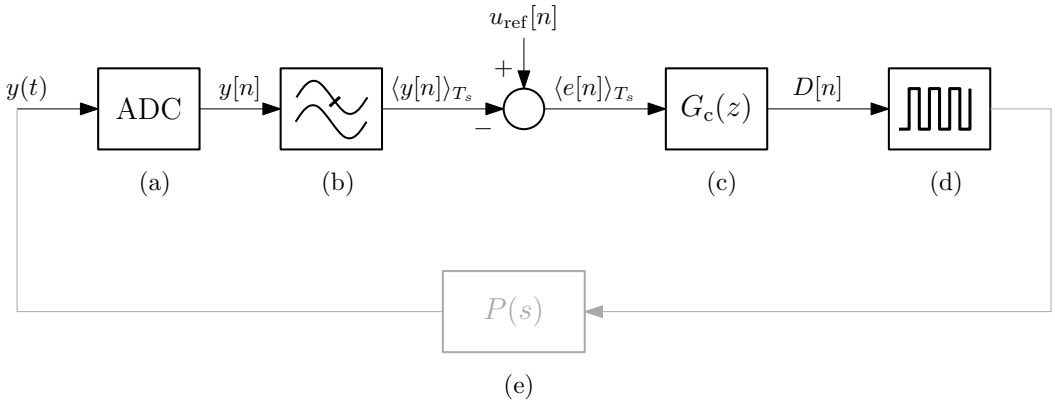


Figure 3.1: Block diagram of a digital control system for power converters, a – analog-to-digital converter, b – digital low-pass filter, c – digital controller, d – pulse width modulator, e – plant

In this chapter operation principles and realizations of all mentioned blocks are presented. However, only these methods and realizations were selected, which in Author's opinion give good results in terms of robustness and performance and are suitable for later practical implementation in a real-time control system. The selection of appropriate methods is critical for further realization and implementation of the control algorithm. The digital filter used for attenuation of the switching ripples in digital representation of voltage or current signals should be simple, easy to implement and suppress not only fundamental frequency of the switching ripples but also its harmonics. Therefore, the moving average filter was chosen for the purpose of this Thesis.

There are numerous approaches to compensator design, which could successfully realize the control of power converters. To limit the selection, only robust, linear, output feedback controllers are considered in this Thesis. Robustness in Author's opinion is one of the most critical requirement for power electronic converters. The specified load variation, converter parameters, input voltage or any other limited disturbances should never destabilize the system. The linear controllers are considered because they are most

established in the literature and offer powerful and flexible methods for system analysis. Other control schemes found in literature include hysteresis control, fuzzy logic, sliding mode, predictive control [14].

Although all the described components are realized in discrete manner, the analysis in all cases is done based on continuous-time prototypes. There are two classical methods for linear digital control system design. One is called indirect technique, where the continuous-time controller $G_c(s)$ is developed in s-domain using well-known classical methods. Then, the discrete-time digital controller in z-domain $G_c(z)$ can be obtained with one of discretization techniques. The second approach is direct technique, where the discrete model of digital controller $G_c(z)$ is derived directly in the z-domain [27, 49]. The illustration of these two design techniques is shown in Fig. 3.2.

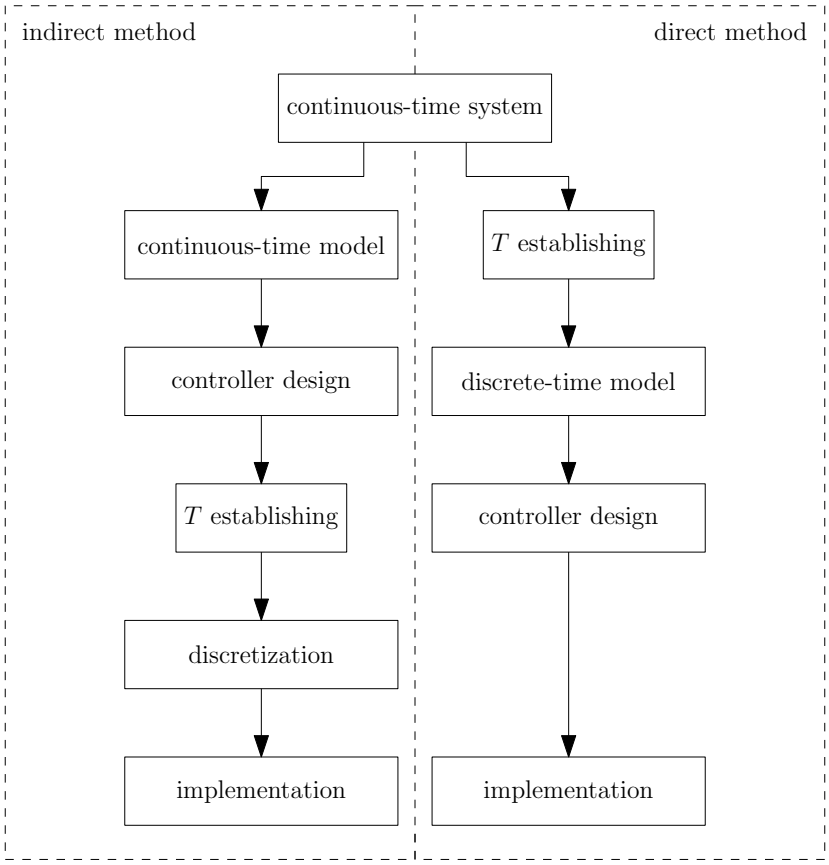


Figure 3.2: Design methods for digital control system [27]

The continuous-time control system is usually better to asses stability, robustness and performance, therefore the indirect method is preferred in this Thesis. However, there is one exception to this rule – in sec. 3.2 the digital realization of the filter is obtained by the direct method.

3.1 Analog-to-digital converter

The analog world of the process and the digital world of the controller is connected with Analog-to-Digital Converter (ADC). Nowadays, most of ADCs are integrated circuits with high resolution and sampling rate. However, it might be important to understand their operational principles and analyze their impact on the system performance. The ADC block in Fig. 3.1 includes not only analog-to-digital converter, but also all essential analog circuits like anti-aliasing filters, attenuators, amplifiers, overvoltage protection circuits, voltage level shifters and matching circuits.

The processed analog signal is subjected to quantization process and then to encoding of the quantized values. Number of quantization levels depends on the resolution of the converter (N). Finite resolution of the converter results in inaccurate digital representation of measurement (mapping ambiguity). This causes the quantization error. The quantization error can be treated as additional additive interfering signal and as such is called quantization noise. The quantization error expresses the difference between the analog input voltage and the reconstructed voltage of the digital representation [38]. The illustration of quantization error for 3-bits converter is shown in Fig. 3.3.

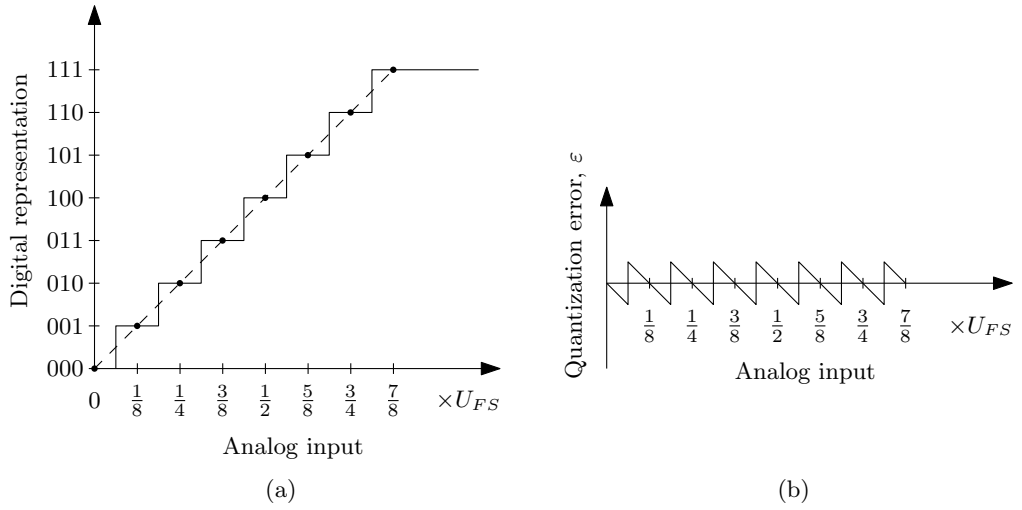


Figure 3.3: Comparison of the analog voltage to the digital representation (a) and quantization error voltage (b) (based on [38])

The average value of quantization noise ε is equal to 0 (as can be seen from Fig. 3.3b), while the RMS value is equal to

$$\varepsilon_{\mathrm{RMS}} = \sqrt{\frac{1}{U_{\mathrm{q}}} \int_{-\frac{U_{\mathrm{q}}}{2}}^{\frac{U_{\mathrm{q}}}{2}} \varepsilon^2 \, \mathrm{d}\varepsilon} = \frac{U_{\mathrm{q}}}{2\sqrt{3}}, \tag{3.1}$$

where U_{q} denotes the the quantum voltage level and is equivalent to the Least Significant Bit (LSB). U_{q} can be obtained by dividing full-scale voltage range U_{FS} by the number of quantization levels 2^N:

$$U_{\mathrm{q}} = \frac{U_{\mathrm{FS}}}{2^N} = 1 \text{ LSB}. \tag{3.2}$$

The Signal-to-Noise Ratio (SNR) can be used to compare the level of full-scale signal to the level of quantization noise. To be able to compare these values, the RMS value of the full-scale peak-to-peak input signal has to be calculated

$$\mathrm{SNR} = 20 \log \frac{U_{\mathrm{FS}}/2\sqrt{2}}{\varepsilon_{\mathrm{RMS}}} = 20 \log \frac{2^N U_{\mathrm{q}}/2\sqrt{2}}{U_{\mathrm{q}}/2\sqrt{3}} \approx 6.02N + 1.76 \text{ [dB]}. \tag{3.3}$$

The values of signal-to-noise ratio caused by quantization for a few most common resolutions for ideal ADC converters are collected in Tab. 3.1. Although the quantization error is not a simple process, it has approximately flat power spectral density and for the numerical simulation purposes it can be modeled as white Gaussian noise.

In practice, the noise in analog/digital conversion can come from more sources. For example, all ADC converters operate in respect to a reference voltage source, which can give varying potential and might drift over the temperature. Another source of error can be a sampling clock, which can introduce the phase noise. On the other hand, there are some well known techniques used to increase the accuracy of measurement (e.g. oversampling or averaging).

Table 3.1: Signal-to-quantization noise ratio for the most common ADC resolutions

resolution	SNR
8 bits	49.9 dB
12 bits	74.0 dB
14 bits	86.1 dB
16 bits	98.1 dB
18 bits	110.1 dB
24 bits	146.3 dB

Various architectures of Analog-to-Digital converters are present in the market and are distinguished by the accuracy, resolution, bandwidth, nonlinearities, cost etc. However, some of them may be not suitable for digital controller for power processing applications. The high bandwidth is required due to the high frequency of the switching signal, which exceeds tens or hundreds thousand operation per second. This eliminates integrating converters and most of Sigma-Delta converters. Moreover, transient states (including input voltage variations and load variations) can result in extremely fast responses which require low latency ADC topologies [63]. The resolution of ADC affects the accuracy of the output voltage in the steady state. The required resolution can be calculated based

on the specified output voltage accuracy ΔU_o and measuring range U_max

$$N = \log_2 \left(\frac{U_\mathrm{max}}{\Delta U_\mathrm{o}} \right). \tag{3.4}$$

For example, to achieve 0.1 V accuracy for range 0 V to 300 V, at least 12-bit ADC is needed.

Based on previous experience of the Author, Successive Approximation ADC converters (SAR) are an excellent choice for use in power conversion applications due to sufficient throughput, resolution, low latency and favorable dynamic properties.

3.2 Moving average digital filter

The passive output filters in power electronic converters smooth the square periodic waveform present on the output of semiconductor devices. Therefore, they attenuate unwanted frequencies and help to produce acceptable shape of output voltage and current. However, the limited size of passive elements and theirs parasitic properties makes perfect filtration impossible. The distorted waveforms come back through analog-to-digital converters into control system and limit the performance and precision of a feedback control.

Ripple is a phenomenon that occurs in all kind of switching-mode power converters. Properly designed passive filter attenuates ripple amplitude to an acceptable level, but cannot remove it completely. However, even small voltage fluctuations impact the accuracy of voltage and current measurements.

Signals of measured voltage and current can be decomposed into DC and ripple components (eq. 3.5),(eq. 3.6).

$$u(t) = U + u_\mathrm{ripple}(t) \tag{3.5}$$

$$i(t) = I + i_\mathrm{ripple}(t) \tag{3.6}$$

In properly designed converter, the amplitude of ripple voltage and current should not exceed the specified limit

$$\|u_\mathrm{ripple}\|_\infty \ll |U| \quad \|i_\mathrm{ripple}\|_\infty \ll |I|. \tag{3.7}$$

In switching converter applications, the ripple spectrum has its fundamental frequency, which is equal to the semiconductor switching frequency, and contains its higher harmonics. When the Nyquist frequency of the sampling systems is higher than the switching frequency, then the analog antialiassing filters can be supported by the digital

filtration of ripple components. Digital filter can be precisely tuned to remove switching frequency component. Moreover, it is possible to adopt the cut-off frequency to the varying switching frequency in case of complex modulator structure.

There are many digital filter realizations able to remove unwanted parts of the spectrum from the input signals. Because the unwanted frequency components are present in the upper range of spectrum, it is possible to apply low-pass digital filter. The moving average filter is a simple linear low-pass windowed FIR filter. Among the many types of digital low-pass filters, moving average filter was selected due to its following properties [21]:

- notches at the switching frequency and its harmonics,
- magnitude of -3 dB at half of the switching frequency.

To understand operation principles of the moving average filter, let us write once again the averaging operator (eq. 3.8). Using Laplace transform, the operator can be described in frequency domain by the following transfer function (eq. 3.9).

$$\langle x(t)\rangle_{T_\mathrm{s}} = \frac{1}{T_\mathrm{s}} \int_{t-T_\mathrm{s}}^{t} x(\tau)\mathrm{d}\tau, \tag{3.8}$$

$$G_\mathrm{av}(s) = \frac{1 - e^{-sT_\mathrm{s}}}{sT_\mathrm{s}}, \tag{3.9}$$

where $x(t)$ denotes the input signal. Fig. 3.4 presents the Bode plot of the continuous-time moving average filter. The graph has normalized value of a frequency variable f/f_s. One can see in the figure, that not only the switching frequency f_s is removed but all its harmonics: $2f_\mathrm{s}$, $3f_\mathrm{s}$, $(\dots)$ are eliminated as well.

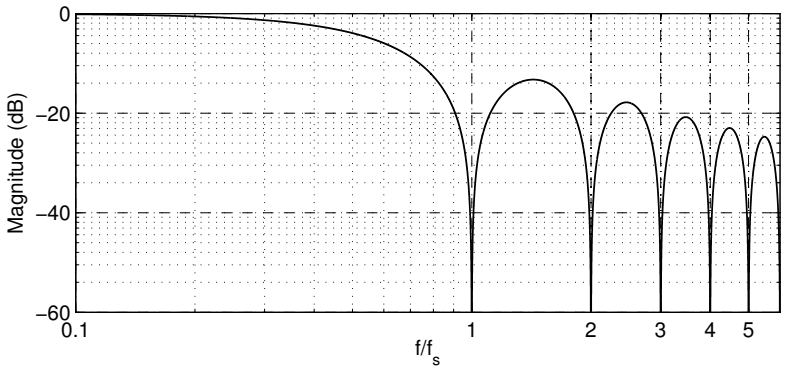


Figure 3.4: Magnitude of an averaging operator in the frequency domain

The equivalent of (eq. 3.9) system in discrete time domain can be obtained using Euler discretization scheme and written as follows.

$$\langle x[n]\rangle_{T_\mathrm{s}} = \frac{1}{N}\sum_{i=0}^{N-1} x[n-i], \tag{3.10}$$

where N denotes number of samples averaged during single switching period T_s.

This system represents a simple Finite Impulse Response (FIR) filter and can be easily implement in FPGA structure, by application of the algorithm based on non-recursive block diagram shown in Fig. 3.5. This implementation is often classified as a direct-form.

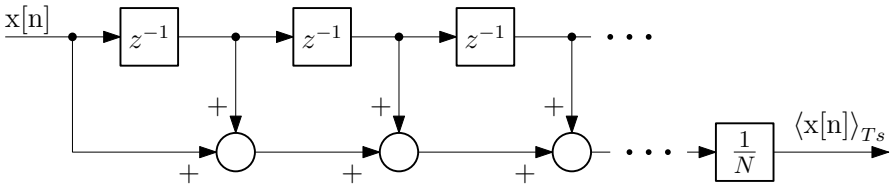


Figure 3.5: Digital realization of moving average filter

It is obvious that the discrete operator (eq. 3.10) for limited number of samples introduces inexactness of average value. To determine the level of inaccuracy between discrete and continuous average a relative mean error can be calculated

$$\delta = \left| \frac{\frac{1}{N-1}\sum_{i=0}^{N} x[n-i] - \frac{1}{T_\mathrm{s}}\int_{t-T_\mathrm{s}}^{t} x(\tau)\mathrm{d}\tau}{\frac{1}{T_\mathrm{s}}\int_{t-T_\mathrm{s}}^{t} x(\tau)\mathrm{d}\tau} \right|. \tag{3.11}$$

The inaccuracy depends on the number of samples N and on the shape of function $x(t)$. To estimate the value of δ as a particular example case, the inductor current waveform is chosen as the function $x(t)$. Inductor transient current has exponential character and on intervals can be described by $\exp(-t\frac{R}{L})$ function, however for very short switching time it can be approximated by triangular waveform, as it was shown previously in chapter 2. Fig. 3.6 shows the induction transient current against various duty cycle D. All waveforms (a), (b) and (c) in Fig. 3.6 have very wide spectrum. The Fourier decomposition of signals results in infinite number of harmonics above fundamental frequency f_s. The quasi-symmetrical waveform in Fig. 3.6b contains almost only odd harmonics, where the "sawtooth" waveforms Fig. 3.6b contains both odd and even harmonics.

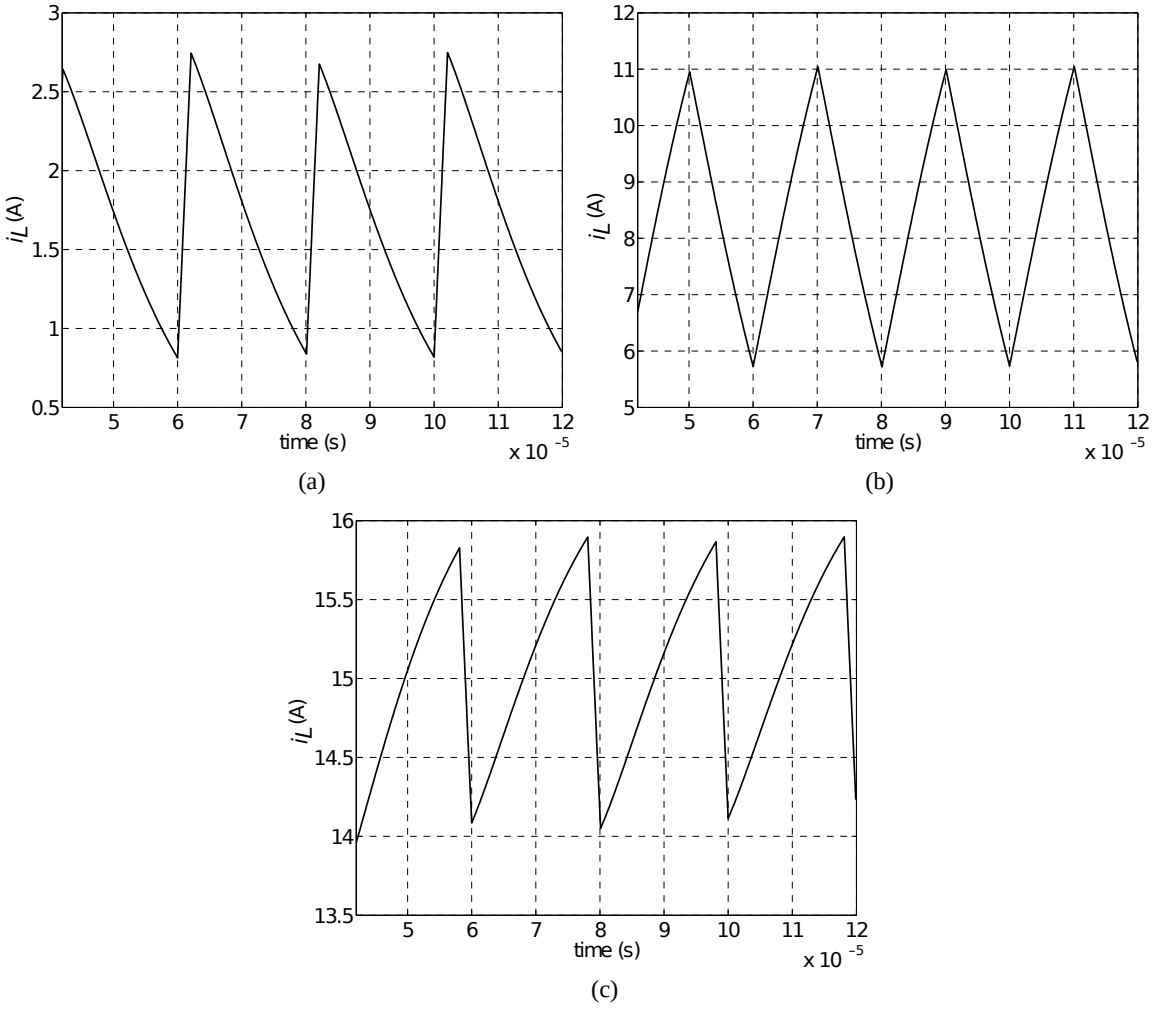


Figure 3.6: Transient inductor current waveform in time domain for various duty cycle values, (a) D=0.1, (b) D=0.5, (c) D=0.9

Let us assume that the signal is sampled at rate N times higher than the fundamental frequency f_s. Thus, the filter window spans a single switching period. The Nyquist–Shannon sampling theorem assumption is met for reconstructing sine wave signal of fundamental frequency f_s, when N is greater than 2. The choice of buffer length N in discrete average function depends on the expected accuracy of mean calculation. Because of an asymmetrical shape of inductor current waveform in time domain for high and low duty cycles D, the relative error of the discrete average operator depends also on D. The relative square error of the discrete averaging operator against duty cycle for buffers of length 2, 3, 4 and 5 was analyzed by the Author and presented in Fig. 3.7. Obviously, the average function can help not only in filtering of current waveform, but also other signals needed to be processed for switching converters control. As an exam-

ple, Fig. 3.8 shows the performance of continuous-time moving average filtration for buck converter output voltage signal. The presented signal voltage is a result of simulation study.

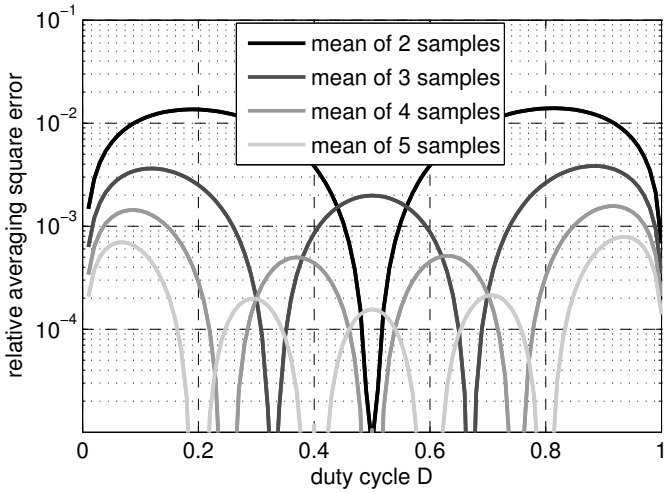


Figure 3.7: The relative error of discrete average operator for various number of samples against duty cycle

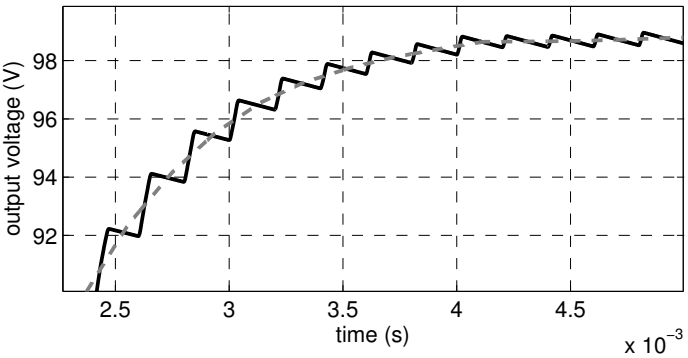


Figure 3.8: The magnified step response of buck-converter output voltage (solid line) and its averaged component (dashed line)

3.3 Compensator – robust control strategy

The most important property, that ensures the proper operation of the dynamical system, is stability. Furthermore, it is expected that the system remains stable despite a reduced order of the model, uncertain model parameters or disturbances.

To ensure power converter performance for unknown or uncertain load parameters and for varying input voltage conditions, the controller has to be designed in a certain manner. The controller which can oppose against parameter variations is described as robust. Robustness against variations of process dynamics is one of the most important factors in the design of control system [5].

It is known that even if the plant transfer function $P(s)$ has no right half-plane poles, closing the feedback loop may make the system unstable. Moreover, even stable closed-loop system may exhibit undesirable properties like overshoot (exceeding the set point value) or ringing (oscillation about the set point value) [21]. Reliable control system provides not only robust performance and ensures stability under varying operating conditions, but also helps to avoid unfavorable behaviors.

Classical stability analysis takes into account stability margins. Two basic stability criteria may help to measure the robustness against process variation: a gain and phase margin [6]. The phase margin ϕ_m (eq. 3.12) defines the difference between the phase angle of open-loop system for gain crossover frequency (ω_gm) and -180° angle. The phase margin specify the maximal additional phase lag, before the closed-loop system loses stability.

$$\phi_\mathrm{m} = 180^\circ - \arg\left(G_\mathrm{C}(j\omega)P(j\omega)\right)|_{\omega=\omega_\mathrm{gm}}. \tag{3.12}$$

The gain margin g_m (eq. 3.13) expresses the value of magnitude (suppression) of open-loop system in phase crossover frequency (ω_pm). The gain margin might help to assess how much the controller gain can be increased, before the closed-loop system loses stability. Gain and phase margins are illustrated on Bode plot in Fig. 3.9.

$$g_\mathrm{m} = -20\log\left(\,|G_\mathrm{C}(j\omega)P(j\omega)|_{\omega=\omega_\mathrm{pm}}\,\right). \tag{3.13}$$

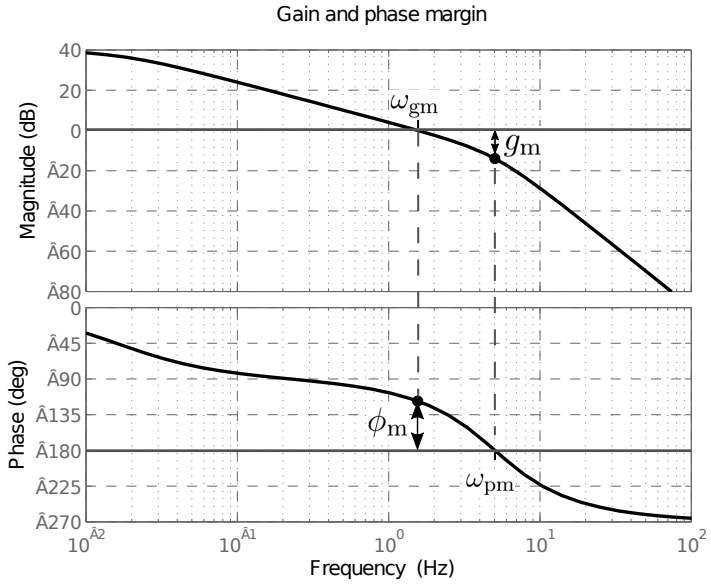


Figure 3.9: Gain and phase margin illustrated on the Bode plot

Both, phase and gain margin refer directly to the Nyquist stability criterion and express the relation between the Nyquist curve and critical point (-1, 0). Despite the gain and margins are still commonly used robustness measures in practical applications [7], the relationship between the stability margins and stability robustness is indirect. They offer the characterization of robustness only by changes in phase angle and magnitude of the nominal Nyquist plot [53]. Unfortunately, the unmodeled dynamics can affect also the shape of the Nyquist plot. In consequence, the modern control design techniques are very often based on H_∞-synthesis or μ-synthesis, where the closed-loop transfer function is subject to optimization.

In power electronic converters, the proper design of robust control systems is challenging. Many switching converters exhibit nonlinear properties, are non-minimum phase, have uncertain parameters and are fed by saturated control signal. [4].

The most important properties of the control system comprise the stability, disturbance rejection and transient response. Therefore, these basic factors should be taken into account with particular attention, when controller properties are specified.

The analysis included in this section relate only to blocks $G_{\mathrm{c}}(z)$ (or $G_{\mathrm{c}}(s)$ for continuous time analysis) and $P(s)$ in Fig. 3.1. In fact, the dynamics of analog and digital filters affect the stability and behavior of the closed loop system. To simplify the derivation, they have been intentionally omitted in the models. However, the complete model

including filter dynamics was taken into account for simulation studies and design of the compensator.

3.3.1 Unmodeled dynamics

When it comes to creating a mathematical model, one tries to accurately describe the physical system dynamics. However, a model is always just an approximation of the system behavior. Very often, for simplicity a model is linearized or considered as linear with neglected nonlinearities. This causes a discrepancy between the model and the real system dynamics. The reduced-order models and system parameter variations are other factors that make the differences. There is a risk that the model discrepancy adversely affects the stability of the system or its performance [28]. For this reasons, introducing the uncertainty models in the system is a very important task and can be useful in the design process of the robust controller and stability analysis.

In many applications it is not possible to consider complete dynamic model of a plant. For example, in electronic circuit design it is very rare to model real-world resistor as a dynamic system. However, at high frequency even resistor is not pure resistance and exhibits some parasitic properties like inductance and capacitance, which in fact complicates the system. The proper uncertainty analysis can be very useful in the robust controller design.

The basic representations of unstructured dynamic uncertainties depending on the location of perturbations are shown in Fig. 3.10. In this case, the considered model is Multiple Input and Multiple Output (MIMO). The additive uncertainty representation in Fig. 3.10a can be useful in characterization of absolute error between nominal model and actual dynamics [28]. It can be described with the combination of nominal plant $P_0(s)$ and unknown transfer function matrix $\Delta(s)$. The dynamics perturbations can be expressed as follows

$$P(s) = P_0(s) + \Delta_{\mathrm{a}}(s), \tag{3.14}$$

where $P(s)$ denotes perturbed system dynamics and $\Delta_{\mathrm{a}}(s)$ represents an unmodeled dynamics. The most common uncertainity model is multiplicative perturbation

$$P(s) = P_0(s)\left(I + \Delta_{\mathrm{s}}(s)\right), \tag{3.15}$$

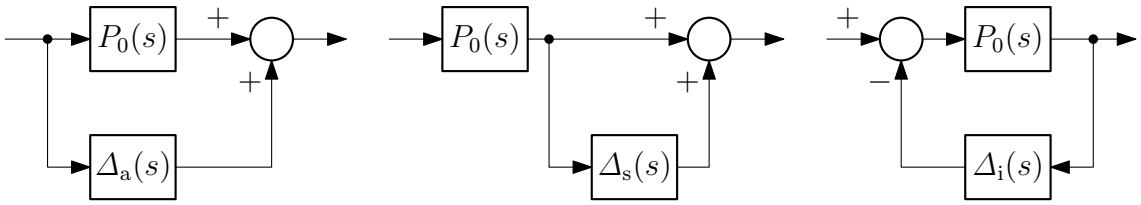
where $\Delta_{\mathrm{s}}(s)$ is a variable stable transfer function, which has bounded magnitude satisfying condition

$$\|\Delta_{\mathrm{s}}(j\omega)\|_\infty = \sup_{\omega\in\mathbb{R}} \sigma_{\max}\left(\Delta_{\mathrm{s}}(j\omega)\right) \leq 1, \tag{3.16}$$

where $\|\cdot\|_\infty$ denotes L_∞ norm and $\sigma_{\max}(\cdot)$ denotes the largest singular value of matrix. Such a perturbation $\Delta_{\mathrm{s}}(s)$ is said to be allowable [15]. The L_∞ norm is further discussed in 3.3.5 and can be considered at this point as a generalization of the Bode amplitude peak response for MIMO systems.

Another uncertainty model is an inverse additive perturbation

$$P^{-1}(s) = P_0^{-1}(s) + \Delta_{\mathrm{i}}(s). \tag{3.17}$$



(a) (b) (c)

Figure 3.10: Three representations od unmodeled dynamics in linear systems. a – additive perturbation; b – output multiplicative perturbation; c – inverse additive perturbation

3.3.2 Parametric uncertainties

Besides the representations of unmodeled or neglected system dynamics, it can be very suitable to consider the parameter perturbations of an identified dynamic model. The inaccurate description of the model in terms of parametric variations might have an impact on the system stability. In fact, the physical parameters of the real system are never exactly known. Therefore, there is necessity to determine the stability properties not only for nominal system, but also for the whole family of systems varied by parameters set.

The universal method for representation of uncertain system as linear is desirable for further analysis. One can split the system into two blocks, where all known and fixed parameters are put together in a linear, time-invariant plant $\mathbf{M}$, while all uncertain and varying parameters form a perturbation matrix Δ [29]. The matrix Δ

$$\Delta = \begin{bmatrix} \delta_1 & & & \\ & \delta_2 & & \\ & & \ddots & \\ & & & \delta_n \end{bmatrix} \tag{3.18}$$

represents complex or real uncertainties, usually concentrated on the main diagonal [40]. Connections between $\mathbf{M}$ and Δ blocks are shown in Fig. 3.11. This approach is called Linear Fractional Transformation (LFT)n. Signals w and z represent exogenous inputs and exogenous outputs of the generalized plant model $\mathbf{M}$ respectively, while signals p and

q are considered as output and input signals of the perturbation block Δ. When $\Delta \equiv 0$, it means that plant $\mathbf{M}$ has nominal transfer function. The LFT is a direct generalization of state-space realizations and is very useful for effective operation on uncertain system.

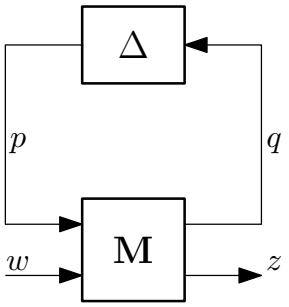


Figure 3.11: Linear Fractional Representation of uncertain model

One can write the following state equation to describe the model illustrated in Fig. 3.11 [36]

$$\begin{array}{lcl} \dot{x}(t) & = & \mathbf{A}x(t) + \mathbf{B_p}p(t) + \mathbf{B_w}w(t), \\ q(t) & = & \mathbf{C_q}x(t) + \mathbf{D_{qp}}p(t) + \mathbf{D_{qw}}w(t), \\ z(t) & = & \mathbf{C_z}x(t) + \mathbf{D_{zp}}p(t) + \mathbf{D_{zw}}w(t), \\ p(t) & = & \Delta q(t), \\ \|\Delta\|_\infty & \leq & 1. \end{array} \tag{3.19}$$

Both, parametric uncertainties and dynamic uncertainties can be modeled with LFT. Let us define a block Δ as a diagonal matrix corresponding to parameter variations. To express the parametric uncertainty as Δ, the LFT is used.

Definition 3.1. *Let* $\mathbf{M}$ *be a partitioned matrix*

$$\mathbf{M} = \begin{bmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{bmatrix}.$$

The upper Linear Fractional Transformation of $\mathbf{M}$ *and* Δ *can be formally defined as*

$$\mathcal{F}_u(\mathbf{M}, \Delta) = M_{22} + M_{21}\Delta(I - M_{11}\Delta)^{-1}M_{12}, \tag{3.20}$$

provided that the inverse $(I - M_{11}\Delta)^{-1}$ *exists [11].*

Buck converter example

Let us consider the buck converter, described previously in sec. 2.2. Now, the model will be extended by uncertain load resistance R_o, inductance L, copper losses R_L and

capacitance C. The electrical circuit is shown in Fig. 3.12. To express variations, the nominal parameters $\bar{L}$ and $\bar{R}_{\mathrm{L}}$ are multiplied by $(1{+}0.2\delta_{\mathrm{L}})$ and $(1{+}0.2\delta_{\mathrm{R_L}})$, respectively, while the nominal parameters $\bar{C}$ and $\bar{R}_{\mathrm{o}}$ are multiplied by $(1{+}0.5\delta_{\mathrm{C}})$ and $(1{+}0.5\delta_{\mathrm{R_o}})$, respectively where $\delta_{(\cdot)}$ is assumed to be unknown value, but normalized in the range of $[-1, 1]$. It means, that in this example the inductance and resistance of inductor can differ from the nominal values maximally by $\pm 20\%$, while the capacitance and load resistance can differ from the nominal values maximally by by $\pm 50\%$ (for example when the additional capacitor is connected to the output by user or additional load is added).

$$\begin{array}{lcl} R_{\mathrm{o}} & = & \bar{R}_{\mathrm{o}}(1+0.5\delta_{\mathrm{R_o}}), \\ C & = & \bar{C}(1+0.5\delta_{\mathrm{C}}), \\ R_{\mathrm{L}} & = & \bar{R}_{\mathrm{L}}(1+0.2\delta_{\mathrm{R_L}}), \\ L & = & \bar{L}(1+0.2\delta_{\mathrm{L}}). \end{array} \tag{3.21}$$

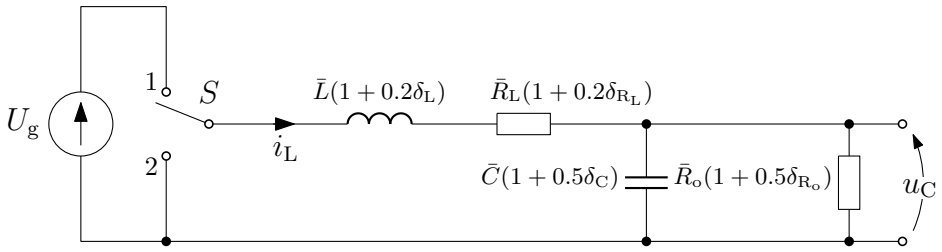


Figure 3.12: Buck converter circuit with uncertain L, R_{L}, C and R_{o} parameters

Hence, the state equations take the following form

$$\begin{cases} \dfrac{\mathrm{d}\langle i_{\mathrm{L}}(t)\rangle_{T_{\mathrm{s}}}}{\mathrm{d}t} = \dfrac{1}{\bar{L}(1+0.2\delta_{\mathrm{L}})}\big(D\,U_{\mathrm{g}} - \langle i_{\mathrm{L}}(t)\rangle_{T_{\mathrm{s}}}(\bar{R}_{\mathrm{L}}(1+0.2\delta_{\mathrm{RL}})) - \langle u_{\mathrm{C}}(t)\rangle_{T_{\mathrm{s}}}\big) \\ \dfrac{\mathrm{d}\langle u_{\mathrm{C}}(t)\rangle_{T_{\mathrm{s}}}}{\mathrm{d}t} = \dfrac{1}{\bar{C}(1+0.5\delta_{\mathrm{C}})}\left(\langle i_{\mathrm{L}}(t)\rangle_{T_{\mathrm{s}}} - \dfrac{\langle u_{\mathrm{C}}(t)\rangle_{T_{\mathrm{s}}}}{\bar{R}_{\mathrm{o}}(1+0.5\delta_{\mathrm{R_o}})}\right) \end{cases}. \tag{3.22}$$

The above system can be illustrated with a block diagram shown in Fig. 3.13.

One can observe that the inversed parameter $\frac{1}{L}$ can be represented as an LFT form:

$$\frac{1}{L} = \frac{1}{\bar{L}(1+0.2\delta_{\mathrm{L}})} = \frac{1}{\bar{L}} - \frac{0.2}{\bar{L}}\delta_{\mathrm{L}}(1+0.2\delta_{\mathrm{L}})^{-1} = \mathcal{F}_u(M_L, \delta_{\mathrm{L}}).$$

Expressions $1/C$ and $1/R_{\mathrm{o}}$ can be dealt with in the same way. Resistance R_{L} may be expressed as follows

$$R_{\mathrm{L}} = \bar{R}_{\mathrm{L}} + 0.2\bar{R}_{\mathrm{L}}\delta_{\mathrm{R_L}}(1 - 0\cdot\delta_{\mathrm{R_L}})^{-1}\cdot 1 = \mathcal{F}_u(M_{\mathrm{R_L}}, \delta_{\mathrm{R_L}}).$$

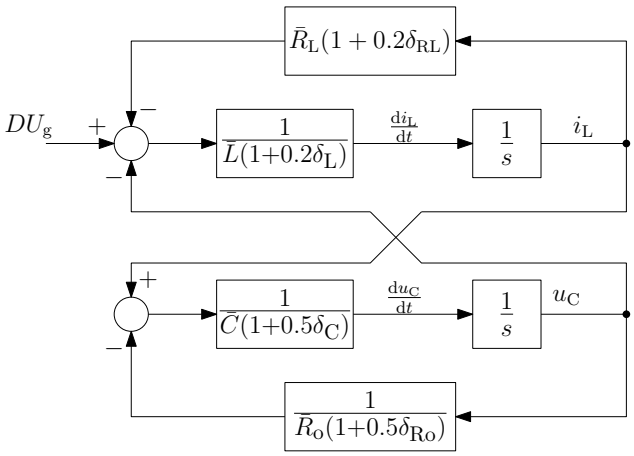


Figure 3.13: Buck converter block diagram with uncertain parameters

Hence, the following matrices are obtained

$$M_{\mathrm{L}} = \begin{bmatrix} -0.2 & 1 \\ -\frac{0.2}{\bar{L}} & \frac{1}{\bar{L}} \end{bmatrix},$$

$$M_{\mathrm{R_L}} = \begin{bmatrix} 0 & 0.2\bar{R}_{\mathrm{L}} \\ 1 & \bar{R}_{\mathrm{L}} \end{bmatrix},$$

$$M_{\mathrm{C}} = \begin{bmatrix} -0.5 & 1 \\ -\frac{0.5}{\bar{C}} & \frac{1}{\bar{C}} \end{bmatrix},$$

$$M_{\mathrm{R_o}} = \begin{bmatrix} -0.5 & \frac{1}{\bar{R}_{\mathrm{o}}} \\ -0.5 & \frac{1}{\bar{R}_{\mathrm{o}}} \end{bmatrix}.$$

Now the block diagram in Fig. 3.13 can be rearranged into a form shown in Fig. 3.14.

Let us define vector p composed of the signals coming out from the perturbation blocks δ_{L}, δ_{RL}, δ_{C}, δ_{Ro} [28]. Signals q_1, q_2, q_3 and q_4 can be considered as artificial outputs depend on $\mathrm{d}i_{\mathrm{L}}/\mathrm{d}t$, i_{L}, $\mathrm{d}u_{\mathrm{C}}/\mathrm{d}t$, u_{C}, respectively.

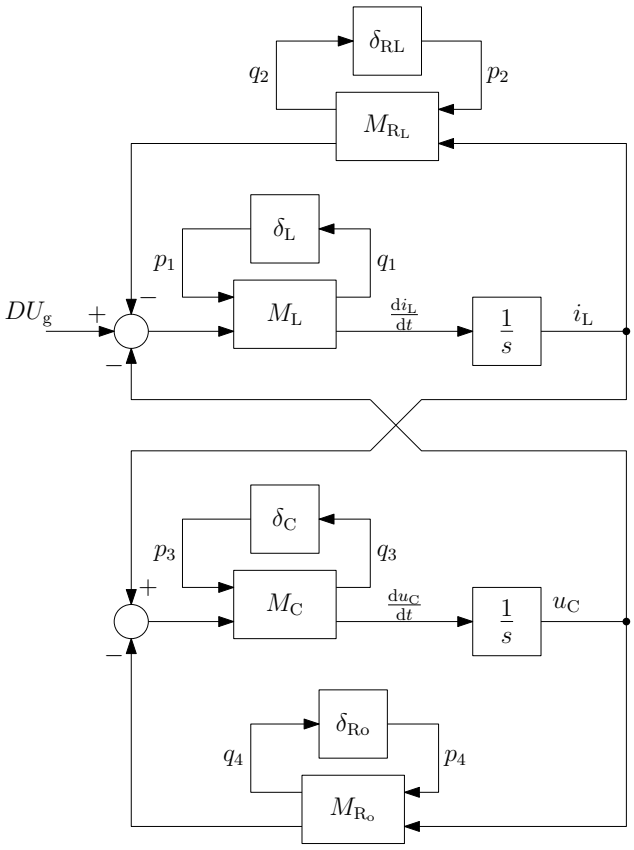


Figure 3.14: Rearranged block diagram with uncertain parameters

$$
\begin{array}{lcl}
\frac{\mathrm{d}i_{\mathrm{L}}}{\mathrm{d}t} & = & \frac{1}{L}\left[D\,U_{\mathrm{g}} - i_{\mathrm{L}}\bar{R}_{\mathrm{L}} - u_{\mathrm{C}} - 0.2p_1 - p_2\right], \\
\frac{\mathrm{d}u_{\mathrm{C}}}{\mathrm{d}t} & = & \frac{1}{C}\left[i_{\mathrm{L}} - \frac{u_{\mathrm{C}}}{\bar{R}_{\mathrm{o}}} - 0.5p_3 + 0.5p_4\right], \\
q_1 & = & D\,U_{\mathrm{g}} - i_{\mathrm{L}}\bar{R}_{\mathrm{L}} - u_{\mathrm{C}} - 0.2p_1 - p_2, \\
q_2 & = & 0.2\bar{R}_{\mathrm{L}}i_{\mathrm{L}} \\
q_3 & = & i_{\mathrm{L}} - \frac{u_{\mathrm{C}}}{\bar{R}_{\mathrm{o}}} - 0.5p_3 + 0.5p_4, \\
q_4 & = & \frac{u_{\mathrm{C}}}{\bar{R}_{\mathrm{o}}} - 0.5p_4 \\
y & = & u_{\mathrm{C}}, \\
p_1 & = & \delta_{\mathrm{L}}q_1, \\
p_2 & = & \delta_{\mathrm{RL}}q_2, \\
p_3 & = & \delta_{\mathrm{C}}q_3, \\
p_4 & = & \delta_{\mathrm{Ro}}q_4.
\end{array}
\tag{3.23}
$$

In state space representation, equations (eq. 3.23) look as follows

$$
\begin{aligned}
\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_\mathrm{L} \\ u_\mathrm{C} \end{bmatrix} &= \begin{bmatrix} -\frac{\bar{R}_\mathrm{L}}{L} & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{C\bar{R}_\mathrm{o}} \end{bmatrix}\begin{bmatrix} i_\mathrm{L} \\ u_\mathrm{C} \end{bmatrix} + \begin{bmatrix} -\frac{0.2}{L} & -\frac{1}{L} & 0 & 0 \\ 0 & 0 & -\frac{0.5}{C} & \frac{0.5}{C} \end{bmatrix}\begin{bmatrix} p_1 \\ p_2 \\ p_3 \\ p_4 \end{bmatrix} + \begin{bmatrix} \frac{U_\mathrm{g}}{L} \\ 0 \end{bmatrix} D, \\
\begin{bmatrix} q_1 \\ q_2 \\ q_3 \\ q_4 \end{bmatrix} &= \begin{bmatrix} -\bar{R}_\mathrm{L} & -1 \\ 0.2\bar{R}_\mathrm{L} & 0 \\ 1 & -\frac{1}{\bar{R}_\mathrm{o}} \\ 0 & \frac{1}{\bar{R}_\mathrm{o}} \end{bmatrix}\begin{bmatrix} i_\mathrm{L} \\ u_\mathrm{C} \end{bmatrix} + \begin{bmatrix} -0.2 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & -0.5 & -1 \\ 0 & 0 & 0 & -0.5 \end{bmatrix}\begin{bmatrix} p_1 \\ p_2 \\ p_3 \\ p_4 \end{bmatrix} + \begin{bmatrix} U_\mathrm{g} \\ 0 \\ 0 \\ 0 \end{bmatrix} D, \\
y &= \begin{bmatrix} 0 & 1 \end{bmatrix}\begin{bmatrix} i_\mathrm{L} \\ u_\mathrm{C} \end{bmatrix}, \\
\begin{bmatrix} p_1 \\ p_2 \\ p_3 \\ p_4 \end{bmatrix} &= \begin{bmatrix} \delta_\mathrm{L} & 0 & 0 & 0 \\ 0 & \delta_\mathrm{RL} & 0 & 0 \\ 0 & 0 & \delta_\mathrm{C} & 0 \\ 0 & 0 & 0 & \delta_\mathrm{Ro} \end{bmatrix}\begin{bmatrix} q_1 \\ q_2 \\ q_3 \\ q_4 \end{bmatrix}.
\end{aligned}
\tag{3.24}
$$

Now one can express the above system with LFT. The output vector is composed of state variable derivatives $\mathrm{d}i_\mathrm{L}/\mathrm{d}t$ and $\mathrm{d}u_\mathrm{C}/\mathrm{d}t$, while the input vector contains state variables and the duty cycle D.

$$
\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix} i_\mathrm{L} \\ u_\mathrm{C} \end{bmatrix} = \mathcal{F}_u(\mathbf{M}, \Delta)\begin{bmatrix} i_\mathrm{L} \\ u_\mathrm{C} \\ D \end{bmatrix}, \tag{3.25}
$$

where

$$
\mathbf{M} = \left[\begin{array}{cccc:cc:c}
-0.2 & -1 & 0 & 0 & -R_\mathrm{L} & -1 & U_\mathrm{g} \\
0 & 0 & 0 & 0 & 0.2R_\mathrm{L} & 0 & 0 \\
0 & 0 & -0.5 & -1 & 1 & -\frac{1}{R_\mathrm{o}} & 0 \\
0 & 0 & 0 & -0.5 & 0 & \frac{1}{R_\mathrm{o}} & 0 \\
\hdashline
-\frac{0.2}{L} & -\frac{1}{L} & 0 & 0 & -\frac{R_\mathrm{L}}{L} & -\frac{1}{L} & \frac{U_\mathrm{g}}{L} \\
0 & 0 & -\frac{0.5}{C} & -\frac{0.5}{C} & \frac{1}{C} & -\frac{1}{CR_\mathrm{o}} & 0
\end{array}\right], \quad
\Delta = \begin{bmatrix} \delta_\mathrm{L} & 0 & 0 & 0 \\ 0 & \delta_\mathrm{RL} & 0 & 0 \\ 0 & 0 & \delta_\mathrm{C} & 0 \\ 0 & 0 & 0 & \delta_\mathrm{Ro} \end{bmatrix}.
\tag{3.26}
$$

Fig. 3.15 illustrates the above equations. The uncertain coefficients in the state-space model are now characterized by an upper LFT realization with a diagonal uncertainty matrix Δ.

The influence of parametric uncertainties on frequency response, where duty cycle D is an input signal and output voltage u_C is an output signal, is shown in Fig. 3.16. The graph was drawn using common MATLAB *bode* function. Before that, the parametric uncertainty was defined using *ureal* function, which create real parameter with nominal value and variability set.

Now, let us consider the nominal plant $P_0(s)$ and the perturbed plant transfer func-

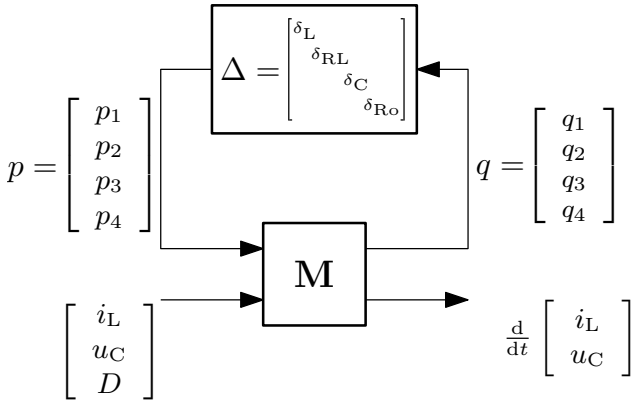


Figure 3.15: Linear Fractional Transformation of the system described by (eq. 3.24)

tion $P(s)$ represented by multiplicative perturbation model

$$P(s) = (1 + \Delta \cdot W_3(s))P_0(s), \tag{3.27}$$

where $W_3(s)$ is a fixed, stable transfer function (usually rational) called uncertainty weighting function [15]. Rewriting the above equation

$$\frac{P(s)}{P_0(s)} - 1 = \Delta \cdot W_3(s). \tag{3.28}$$

Recalling that the perturbation function satisfies the condition $||\Delta||_\infty \leq 1$ the following inequality holds

$$\left| \frac{P(j\omega)}{P_0(j\omega)} - 1 \right| \leq |W_3(j\omega)| \qquad \forall \omega \in \mathbb{R} \tag{3.29}$$

Hence, the magnitude of weighting function $|W_3(j\omega)|$ provides the uncertainty profile [15].

Weighting function for uncertain system described with state equation (eq. 3.24) can be obtained directly using (eq. 3.28). The left-hand side of (eq. 3.28) is illustrated in Fig. 3.17 as a family of amplitude responses. A simple function which is an upper bound of the magnitude plot for all frequencies for this example can be proposed as follows

$$W_3(s) = \frac{3.33s}{s + 16600}. \tag{3.30}$$

The magnitude response of this function is presented in Fig. 3.17 as a bold solid line.

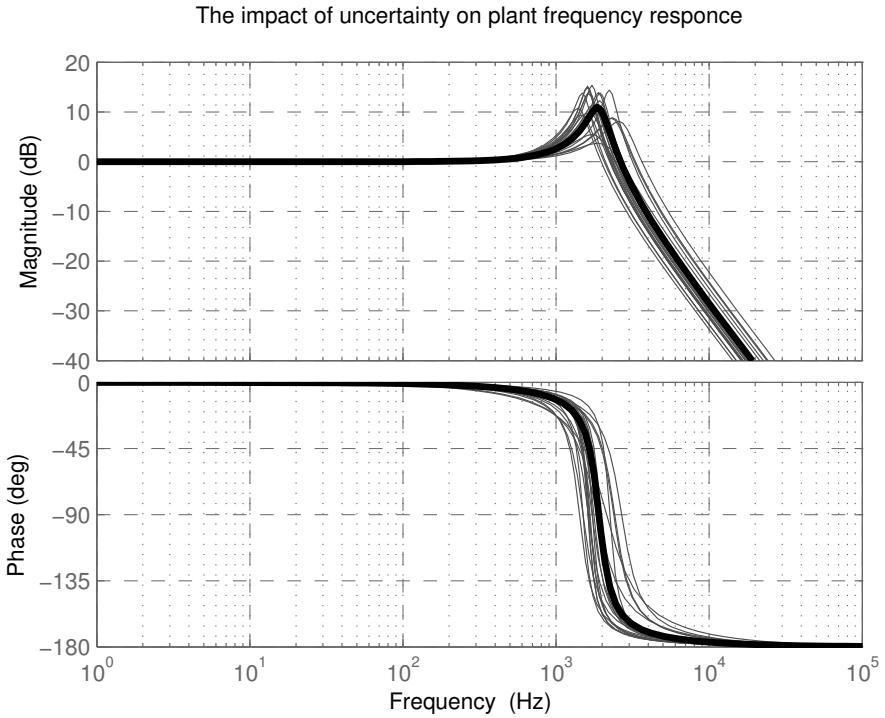


Figure 3.16: The impact of plant model uncertainties on a frequency response (a black thick line refers to the nominal plant)

3.3.3 Robust control design

Let us investigate how the external signals: the reference signal r, the external disturbance d and the measurement noise n influence the output signals u, v, y. The analyzed control loop is presented in Fig. 3.18, where the controller is described with two transfer functions: set point prefilter $F(s)$ and feedback $G_{\mathrm{C}}(s)$. The plant model is denoted by $P(s)$. This kind of control system is one of few closed loop systems with two degrees of freedom. The relationships are collected in (eq. 3.31).

$$\begin{bmatrix} \hat{u} \\ \hat{v} \\ \hat{y} \end{bmatrix} = \begin{bmatrix} \frac{G_{\mathrm{C}}(s)F(s)}{1+P(s)G_{\mathrm{C}}(s)} & \frac{-P(s)G_{\mathrm{C}}(s)}{1+P(s)G_{\mathrm{C}}(s)} & \frac{-G_{\mathrm{C}}(s)}{1+P(s)G_{\mathrm{C}}(s)} \\ \frac{P(s)G_{\mathrm{C}}(s)F(s)}{1+P(s)G_{\mathrm{C}}(s)} & \frac{P(s)}{1+P(s)G_{\mathrm{C}}(s)} & \frac{-P(s)G_{\mathrm{C}}(s)}{1+P(s)G_{\mathrm{C}}(s)} \\ \frac{P(s)G_{\mathrm{C}}(s)F(s)}{1+P(s)G_{\mathrm{C}}(s)} & \frac{P(s)}{1+P(s)G_{\mathrm{C}}(s)} & \frac{1}{1+P(s)G_{\mathrm{C}}(s)} \end{bmatrix} \begin{bmatrix} \hat{r} \\ \hat{d} \\ \hat{n} \end{bmatrix}^{\mathrm{T}} . \tag{3.31}$$

One can notice that some transfer functions occur repeatedly. Hence, for system with two degrees of freedom, 6 unique transfer functions can be written down to characterize the system properties and they are known as a "Gang of Six" [6]. Analogically, the system

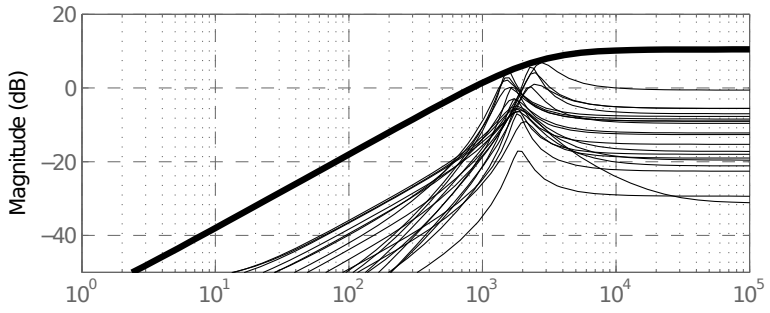


Figure 3.17: The magnitude plot of left-hand side of equation (eq. 3.28) and Bode magnitude characteristics of proposed W_3 transfer function (bold line)

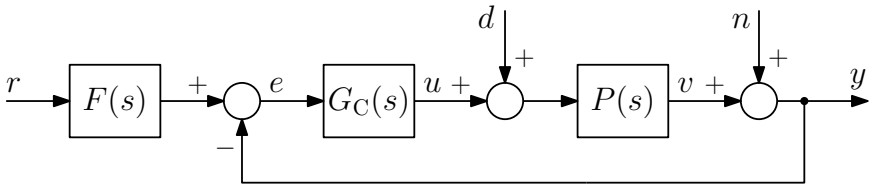


Figure 3.18: Block diagram of a control system of two degrees of freedom

without set point prefilter block $F(s)$ (Fig. 3.19) can be characterized by 4 basic unique transfer functions and they are known as a "Gang of Four" [6]

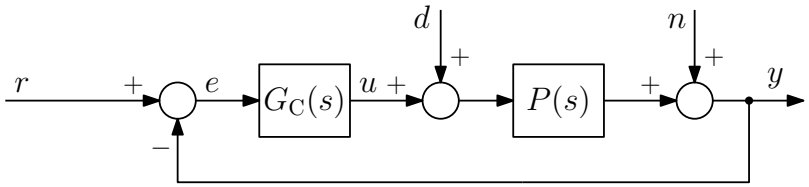


Figure 3.19: Block diagram of a control system of one degree of freedom

$$\begin{bmatrix} \hat{u} \\ \hat{y} \end{bmatrix} = \begin{bmatrix} \frac{G_{\mathrm{C}}(s)}{1+P(s)G_{\mathrm{C}}(s)} & \frac{-P(s)G_{\mathrm{C}}(s)}{1+P(s)G_{\mathrm{C}}(s)} & \frac{-G_{\mathrm{C}}(s)}{1+P(s)G_{\mathrm{C}}(s)} \\ \frac{P(s)G_{\mathrm{C}}(s)}{1+P(s)G_{\mathrm{C}}(s)} & \frac{P(s)}{1+P(s)G_{\mathrm{C}}(s)} & \frac{1}{1+P(s)G_{\mathrm{C}}(s)} \end{bmatrix} \begin{bmatrix} \hat{r} \\ \hat{d} \\ \hat{n} \end{bmatrix}^{\mathrm{T}}. \tag{3.32}$$

Two of them are given special attention, since they are used for compensator synthesis:

$$S(s) = \frac{\hat{e}(s)}{\hat{r}(s)} = \frac{\hat{y}(s)}{\hat{n}(s)} = \frac{1}{1 + P(s)G_{\mathrm{C}}(s)}, \tag{3.33}$$

$$T(s) = \frac{\hat{y}(s)}{\hat{r}(s)} = \frac{P(s)G_{\mathrm{C}}(s)}{1 + P(s)G_{\mathrm{C}}(s)}. \tag{3.34}$$

The first transfer function is called sensitivity function $S(s)$ while the second one is termed complementary sensitivity function $T(s)$. In literature [59] one can find that the another two transfer functions from "Gang of Four" are called: the input disturbance sensitivity function $(\hat{y}(s)/\hat{d}(s))$ and the control sensitivity function $(\hat{u}(s)/\hat{r}(s))$. The input disturbance sensitivity function can be also considered as a product of $S(s)G_{\mathrm{C}}(s)$, while the control sensitivity function as a product of $S(s)P(s)$. Closed loop system is internally stable if and only if all four transfer functions from (eq. 3.32) are stable.

The complementary sensitivity function plays an important role in the measurement of disturbance rejection properties. When high disturbance rejection characteristic is required ($y(t) \simeq r(t)$), $T(s)$ should assume magnitude close to 1 for certain frequencies. Moreover, good tracking property is also indicated by $T(s)$ values close to 1. Both goals seem to be achieved simultaneously.

The control sensitivity transfer function $G_{\mathrm{C}}(s)S(s)$ describes how $n(t)$ influences $u(t)$. It can be shown that for high frequencies, where plant gain usually drops, the noise induced component of control signal is considerably amplified. It may result in unacceptably high amplitude of $u(t)$. An important property of sensitivity function is reflecting, how the variation of the process influences the closed loop properties

$$\frac{\mathrm{d}T(s)/T(s)}{\mathrm{d}P(s)/P(s)} = \frac{PG_{\mathrm{C}}}{T(1 + PG_{\mathrm{C}})^2} = S(s). \tag{3.35}$$

Since the sum of sensitivity function and complementary sensitivity function equals 1,

$$S(s) + T(s) = 1 \tag{3.36}$$

it would be desirable to keep sensitivity function low for broad spectrum. Unfortunately, there are some constraints on the sensitivity function. The integral Bode's formula for loop transfer function without poles in the right half plane and pole excess at least 2

$$\int_0^\infty \log|S(j\omega)|\mathrm{d}\omega = 0 \tag{3.37}$$

shows that if the magnitude of sensitivity function is made smaller for selected frequencies, it must increase for other frequencies [6].

One can notice that, good tracking properties and disturbance rejection have to be traded off against suppression of measurement noise n.

One possible approach to solve the above problem is to minimize the norm of each sensitivity function only for a selected frequency range. Since the sensitivity function $S(s)$ represents the influence of noise and disturbances, it would be enough to limit its norm for low frequencies only. The complementary sensitivity function $T(s)$ represents the ability of setpoint-tracking property, hence its norm has to equal 1 for lower frequencies in order to reduce the magnitude of the error.

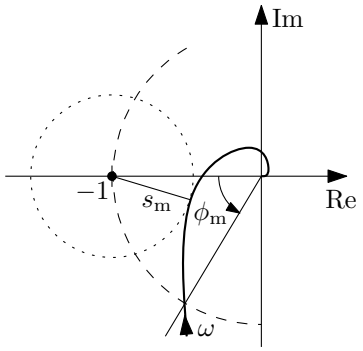


Figure 3.20: Nyquist plot with marked phase margin ϕ_m and a critical point $(-1,0)$. The shortest distance between the critical point and a Nyquist curve is the robustness measure s_m

The maximum magnitude of sensitivity function over all frequency range can be used as another robustness measure, except gain and phase margin. Let us introduce the sensitivity margin s_m, which can be expressed as the inversion of maximum magnitude of sensitivity function

$$s_\mathrm{m} = \frac{1}{\|S(j\omega)\|_\infty} = 1/\sup_{\omega\in\mathbb{R}} |S(j\omega)|. \tag{3.38}$$

The sensitivity measure has a straightforward interpretation in the Nyquist plot (Fig. 3.20).

The complementary sensitivity function can be used to measure allowable process variation. Let us assume, that the nominal process P_0 is perturbed without causing instability to $P_0+\Delta P$. The loop function changes from $\mathcal{L}_0 = P_0 G_\mathrm{C}$ to $\mathcal{L}_1 = G_\mathrm{C}(P_0+\Delta P)$, as it is illustrated in Fig. 3.21. If the difference between $\mathcal{L}_1$ and $\mathcal{L}_0$ is lower than the distance between the critical point $(-1,0)$, than the sufficient condition for stability under perturbation is met.

Theorem 3.1. *Robust stability theorem* [46]. *Assume that a particular controller $G_\mathrm{C}(s)$ stabilizes the nominal model $P_0(s)$, and all models $P(s)$ have the same number of the closed right half-plane poles. Then all models $P(s)$ are feedback loop stable with controller $G_\mathrm{C}(s)$ if and only if the complementary sensitivity function $T(s)$ satisfies the following bound*

$$\frac{|\Delta P(j\omega)|}{|P_0(j\omega)|} < \frac{1}{|T(j\omega)|}, \qquad \forall\omega \in \mathbb{R} \tag{3.39}$$

■

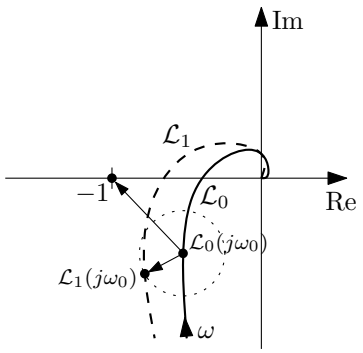


Figure 3.21: Geometric interpretation of robust stability theorem

Quotient $\Delta P(s)/P_0(s)$ can be described as a product $W_3(s)\Delta(s)$, where $W_3(s)$ represents the profile of uncertainty and $||\Delta(j\omega)||_\infty \leq 1$.

Hence, if supremum of $|T(j\omega)W_3(j\omega)|$ for all $\omega \in \mathbb{R}$ is less than 1, the controller $G_\mathrm{C}(s)$ internally stabilizes the perturbed plant $P(s)$.

The inequality means that the critical point $(-1,0)$ lies outside the disk of center located in $P_0(j\omega)G_\mathrm{C}(j\omega)$ and radius of $|W_3(j\omega)P_0(j\omega)G_\mathrm{C}(j\omega)|$ for every frequency $\omega \in \mathbb{R}$. This can be illustrated in the Nyquist plot in Fig. 3.22, where $\mathcal{L}_l(j\omega) = P_0(j\omega)G_\mathrm{C}(j\omega)$ is the loop function. The geometric interpretation refers directly to the Nyquist stability criterion assuming that the open loop system is stable, when the Nyquist contour given by $\Omega = \{\mathcal{L}(j\omega) : -\infty < \omega < \infty\} \subset \mathbb{C}$ has no net encirclements of the critical point $(-1,0)$ [6].

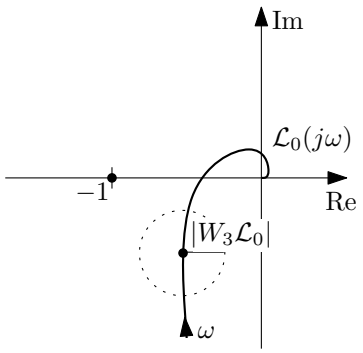


Figure 3.22: Illustration of robust stability (based on [15])

3.3.4 Lead-lag compensator

A classical approach to compensator design for power processing systems is based on realization of a desired transfer function in analog technique, usually by means of operational amplifiers and RC filters. A lead-lag compensator design is based on achieving desired open-loop transfer function by introducing poles and zeros in $G_{\mathrm{C}}(s)$.

One can specify the elementary transfer functions: real left half-plane pole and real left half-plane zero (eq. 3.40), real right half-plane zero (eq. 3.41), inverted real left half-plane pole (eq. 3.42) and inverted real left half-plane zero (eq. 3.43). Right half-plane pole transfer function is not listed below, since it is unstable and unusable for the purpose of controller design. In all cases below, the cut-off frequency (frequency where the magnitude is equal to ± 3 dB) is denoted by ω_0. Frequency responses of each transfer function are shown in Fig. 3.23, Fig. 3.24 and Fig. 3.25

$$G_{\mathrm{LP}}(s) = \frac{1}{1 + \frac{1}{\omega_0}s}, \qquad G_{\mathrm{LZ}}(s) = 1 + \frac{1}{\omega_0}s, \tag{3.40}$$

$$G_{\mathrm{RZ}}(s) = 1 - \frac{1}{\omega_0}s, \tag{3.41}$$

$$G_{\mathrm{LPI}}(s) = \frac{1}{1 + \frac{\omega_0}{s}} = \frac{\frac{1}{\omega_0}s}{1 + \frac{1}{\omega_0}s}, \tag{3.42}$$

$$G_{\mathrm{LZI}}(s) = 1 + \frac{\omega_0}{s} = \frac{1 + \frac{1}{\omega_0}s}{\frac{1}{\omega_0}s}. \tag{3.43}$$

The elementary transfer function can be used to build various, more sophisticated compensator variants. Lead compensator is used in order to decrease phase lag for certain frequencies, so in result it improves the phase margin ϕ_{m}. Lead compensator introduces left half-plane pole-zero pair. The value of a cut-off frequency for single zero is usually chosen as lower than a gain crossover frequency. The value of a single pole cut-off frequency is much higher than a gain crossover frequency, to realize real-differentiation action.

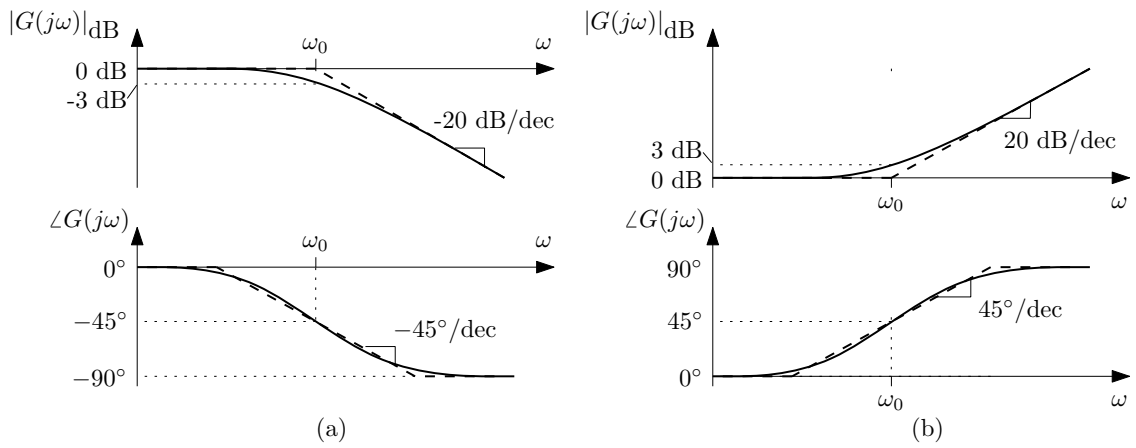


Figure 3.23: Bode characteristics (magnitude and phase) of real left half-plane pole (a), and real left half-plane zero (b) transfer functions

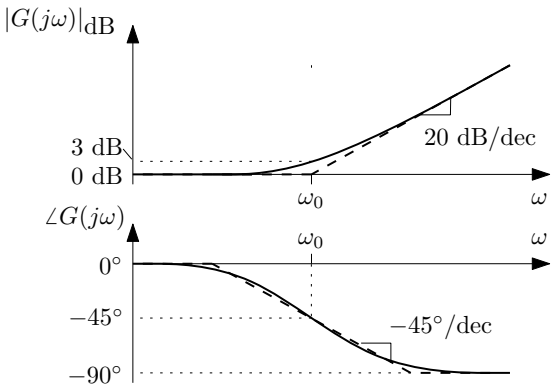


Figure 3.24: Bode characteristics (magnitude and phase) of real right half-plane zero transfer functions

Lag compensator is responsible mainly for increasing low-frequency loop gain [21]. As a consequence of lag action, the steady-state error is reduced and control performance is improved. Lag compensator transfer function has a left half-plane zero and left half-plane pole, where the pole corner frequency is lower than zero corner frequency. Lead and lag compensator actions are often combined together. In that case, to obtain high DC-gain and at the same time not worsen the phase margin, it is recommended to choose the value of the lag compensator inverted pole cut-off frequency at least one decade lower than the lead compensator zero cut-off frequency.

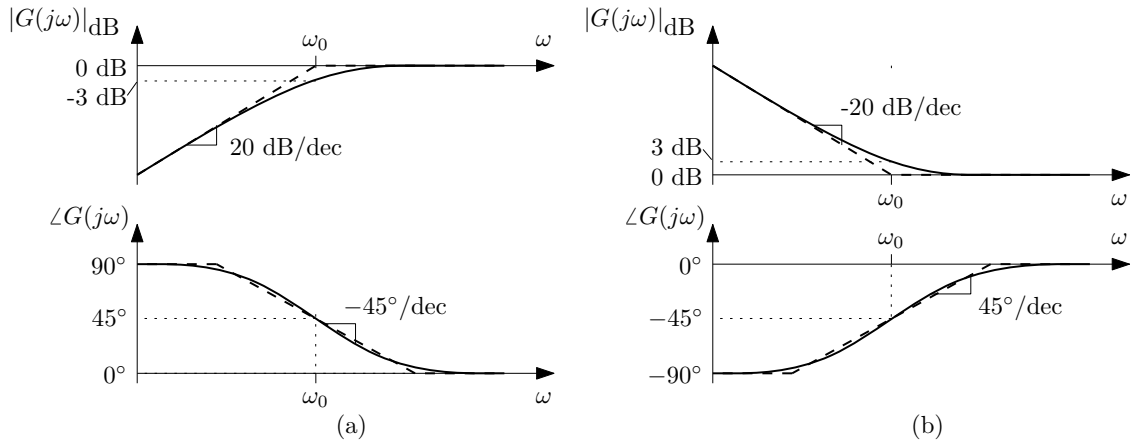


Figure 3.25: Bode characteristics (magnitude and phase) of inverted left half-plane pole (a), and inverted left half-plane zero (b) transfer functions

An example transfer function of combination of lead and lag compensator is given in (eq. 3.44), where ω_{z1} and ω_{z2} denote zeros cut-off frequencies and ω_{p} denotes pole cut-off frequency. A lead-lag compensator can be considered a part of a Proportional-Integral-Derivative controller (PID) loop. It has two zeros at $-\omega_{\mathrm{z1}}$ and $-\omega_{\mathrm{z2}}$ frequencies and two poles at 0 and $-\omega_{\mathrm{p}}$. The former zero frequency is a parameter of lag compensation (PI action), while the latter zero frequency is a parameter of lead compensation. The frequency response of the lead-lag controller is presented in Fig. 3.27. Properly designed lead-lag compensator can make the system robust and allows to meet the specified requirements regarding phase and gain margin [9].

$$G_{\mathrm{C}}(s) = G_{\mathrm{C0}} \frac{\left(1+\frac{\omega_{\mathrm{z1}}}{s}\right)\left(1+\frac{s}{\omega_{\mathrm{z2}}}\right)}{\left(1+\frac{s}{\omega_{\mathrm{p}}}\right)} = G_{\mathrm{C0}} \frac{\frac{1}{\omega_{\mathrm{z2}}}s^2 + \left(1+\frac{\omega_{\mathrm{z1}}}{\omega_{\mathrm{z2}}}\right)s + \omega_{\mathrm{z1}}}{\frac{1}{\omega_{\mathrm{p}}}s^2 + s}, \tag{3.44}$$

The transfer function of the lead-lag controller can be designed and verified with a help of MATLAB environment, as it is presented in the example listing 3.1.

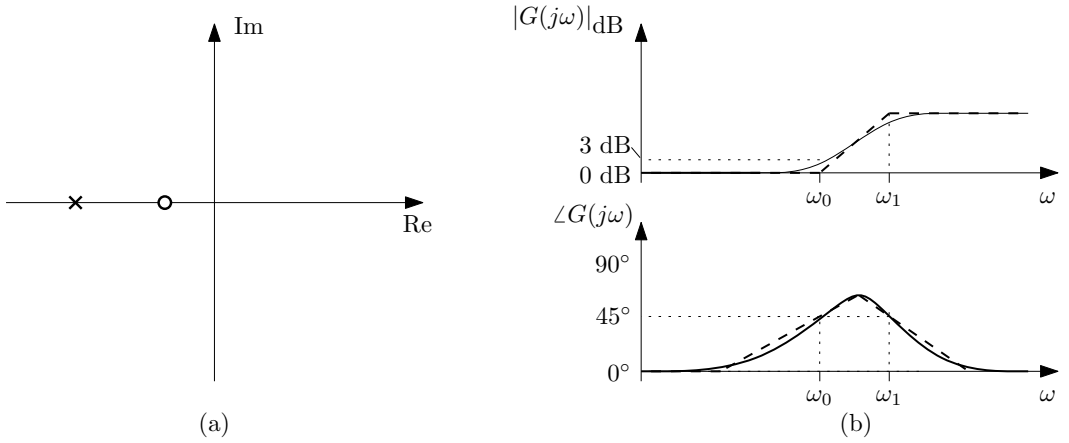


Figure 3.26: Zero and pole location of lead compensator on a complex plane (a) and Bode characteristics (magnitude and phase) (b)

Listing 3.1: Matlab source code for computing lead-lag controller

```
%% Lead compensator
%%
%% f_z = 3 kHz = 18850 rad/s
%% f_p = 40 kHz = 251330 rad/s
%%
%%                    s/f_z + 1
%% G_lead = GC0 * -------------
%%                    s/f_p + 1
%%
GC0 = 0.4;
T1=GC0 * tf([1/18850 1],[1/251330 1]);

%% Lag compensator
%%
%% f_L = 352 Hz = 2217 rad/s
%%
%%             s + f_l
%% G_lag = -----------
%%                s
%%
T2=tf([1 2703],[1 0]);

C_lead_lag = T1*T2;
```

The presented compensator can help to obtaining a robust system. The methods presented previously in section 3.3.3 can help to asses the closed-loop robust stability and robust performance. Usually, controller design is an iterative process – when the system specification and assumptions are not met, the designer has to keep retuning

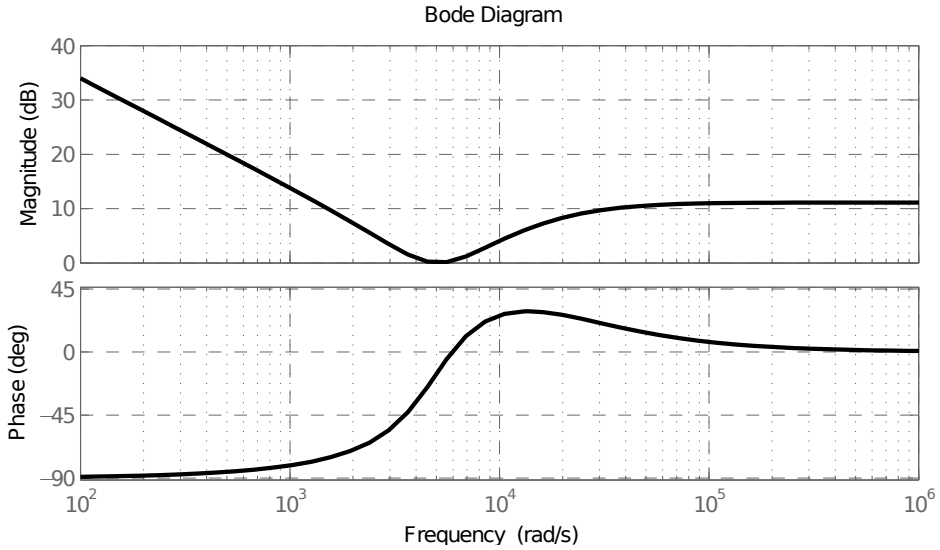


Figure 3.27: Bode characteristics (magnitude and phase) of the lead-lag compensator

controller parameters until satisfactory results are achieved.

3.3.5 $\mathcal{H}_\infty$ controller

The $\mathcal{H}_\infty$ is a method of controller synthesis based on a mathematical optimization problem. The $\mathcal{H}_\infty$ control approach leads to linear compensator with higher order compared to second-order lead-lag system (depending on the dimension of the plant and weighting functions structure). Nevertheless, the high computational effort necessary for digital implementation of high-order system is not challenging for modern computing machines, in particular based on parallel computing. Furthermore, it is worth to implement high-order compensator to approximate the theoretical best controller [39].

The $\mathcal{H}_\infty$ optimal controller design concerns the worst-case error signal, that can occurs on systems input, by minimizing L_∞ norm. For MIMO system the norm can be expressed as

$$\|H(j\omega)\|_\infty = \sup_{\omega\in\mathbb{R}} \sigma_{\max}\left(|H(j\omega)|\right). \tag{3.45}$$

Let us define the L_∞ norm of the weighted sensitivity function $S(s)$ [46]

$$\|W_1(s)S(s)\|_\infty = \sup_{\omega\in\mathbb{R}} |W_1(j\omega)S(j\omega)|. \tag{3.46}$$

The performance specification (a measure of goodness of tracking) can be described by the following inequality

$$\|W_1(s)S(s)\|_\infty \leq 1. \tag{3.47}$$

For Single Input and Single Output (SISO) system this has an interesting graphical interpretation visualized in Fig. 3.28, which says that every corresponding point of open loop function on the Nyquist plot for frequency ω lies outside the disc of center at point $-1+0j$ and radius $|W_1(j\omega)|$.

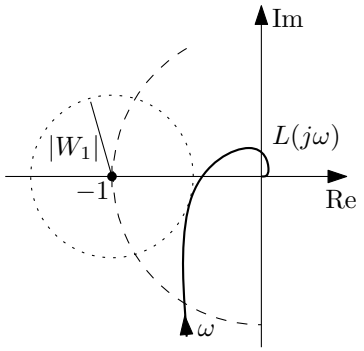


Figure 3.28: Illustration of performance specification (based on [15])

Selecting appropriate weighting function $W_1(j\omega)$ might lead to synthesis of the controller $G_C(j\omega)$ which make magnitude of the sensitivity function $S(j\omega)$ low for certain frequencies. However, to get robust controller, the objective function has to be enriched by another component, which makes magnitude of the complementary sensitivity function $T(j\omega)$ low for another frequency range. Recalling the robust stability theorem (eq. 3.39), complementary sensitivity function has to be small in the frequency range, where the uncertainty is large [46]

$$\frac{|\Delta P(j\omega)|}{|P_0(j\omega)|} < \frac{1}{|T(j\omega)|}, \quad \forall\omega \in \mathbb{R} \tag{3.48}$$

Let us consider the perturbed plant transfer function $P(s) = (1 + \Delta(s)W_3(s))P_0(s)$. Here $P_0(s)$ is related to a nominal plant transfer function and $W_3(s)$ is a fixed stable weighting transfer function. $\Delta(s)$ is a variable stable transfer function satisfying the condition $\|\Delta(s)\|_\infty \leq 1$ [15]. The above condition can be rewritten to the following equation

$$\frac{P(s)}{P_0(s)} - 1 = \Delta(s)W_3(s). \tag{3.49}$$

Because $\|\Delta(s)\|_\infty \leq 1$, one can write the inequality

$$\left|\frac{P(s)}{P_0(s)} - 1\right| \leq |W_3(s)|, \tag{3.50}$$

where $W_3(s)$ provides the profile of uncertainty. Hence

$$\|W_3(s)T(s)\|_\infty < 1. \tag{3.51}$$

It is important, that good tracking property of low frequency signal requires the module of complementary sensitivity function for certain frequency range to be equal or close to 1 [36].

As it was already written, the sum of sensitivity function and complementary sensitivity function is equal to 1. Hence, a tradeoff between robust stability and nominal performance arises [46]:

$$|W_1(j\omega)S(j\omega)| + |W_3(j\omega)T(j\omega)| < 1 \quad \forall\omega \in \mathbb{R}. \tag{3.52}$$

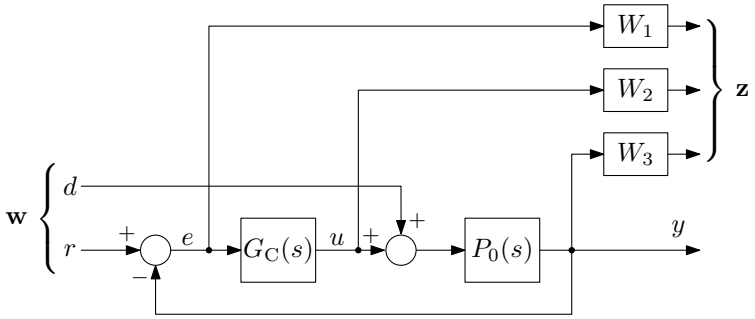


Figure 3.29: Block diagram of the closed-loop system with weighting functions W_1, W_2 and W_3, where W_1 is penalizing the error signal, W_2 is penalizing the control signal and W_3 is penalizing the output signal [56]

To formulate optimization problem, the weighting functions have to be known. One can determine weighting functions by taking into account the following rules. When the following criteria are met:

- the module of $W_1(s)$ is greater than 1 for low frequency range,
- the module of $W_1(s)$ and $S(s)$ product is less than 1 for whole frequency range,
- $W_1(s)$ is proper and stable,

then the module of $S(s)$ is less than 1 for low frequency range.

When the following criteria are met:

- the module of $W_3(s)$ is greater than 1 for high frequency range,
- the module of $W_3(s)$ and $T(s)$ product is less than 1 for whole frequency range,
- $W_3(s)$ is proper and stable,

then the module of $T(s)$ is less than 1 for high frequency range. Example of weighting functions W_1 and W_3 which satisfy above requirements is shown in Fig. 3.31. One can also consider complementing the system with weighting function W_2 to limit the maximum magnitude of control sensitivity function $G_{\mathrm{C}}(s)S(s)$.

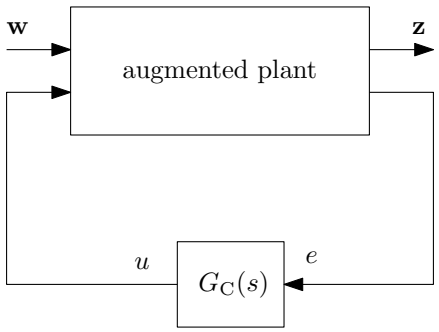


Figure 3.30: Augmented plant block diagram commonly used for $\mathcal{H}_\infty$ controller synthesis using optimization

In (eq. 3.47) weighting function W_1 is multiplied by $S(s)$, while in (eq. 3.51) weighting function W_3 is multiplied by $T(s)$. $S(s)$ corresponds to G_{er} transfer function relating r to e, while $T(s)$ equals G_{yr} and describes a relation between r and y:

$$\hat{e} = G_{er}\hat{r}, \qquad \hat{y} = G_{yr}\hat{r}. \tag{3.53}$$

Let us suppose that for a given ω $|\hat{r}(\omega)| = 1$. Then, one can substitute $|W_1 S(s)|$ for $|W_1\hat{e}|$ and $|W_3 T(s)|$ for $|W_3\hat{y}|$. That explains introduction of W_1 and W_3 blocks into the closed loop system block diagram shown in Fig. 3.29. The SISO system presented in Fig. 3.29 can be transformed into standard closed-loop form for structured $\mathcal{H}_\infty$ synthesis, shown in Fig. 3.30. Signals e and u denote error value and control signal respectively, $\mathbf{w}$ is the exogenous vector signal, that represents in this case the reference signal r and disturbance signal d, while $\mathbf{z}$ is a vector signal that combines outputs from blocks W_1, W_2 and W_3. The vector $\mathbf{z}$ is a "virtual" output, that is used only for controller design. The augmented plant is described by the following equations

$$\begin{aligned} \dot{x} &= \mathbf{A}x + \mathbf{B_w}\mathbf{w} + \mathbf{B_u}u, \\ \mathbf{z} &= \mathbf{C_z}x + \mathbf{D_{zw}}\mathbf{w} + \mathbf{D_{zu}}u, \\ yu &= \mathbf{C_y}x + \mathbf{D_{yw}}\mathbf{w} + \mathbf{D_{yu}}u. \end{aligned} \tag{3.54}$$

The controller $G_{\mathrm{C}}(s)$ can be described by the linear time-invariant state-space system as well

$$\begin{aligned} \dot{x}_k &= \mathbf{A_k}x_k + \mathbf{B_k}e, \\ u &= \mathbf{C_k}x_k + \mathbf{D_k}e. \end{aligned} \tag{3.55}$$

The optimization problem is based on selecting the controller $G_C(s)$ among all controllers which make the closed loop system stable for certain plant $P(s)$, which minimizes the norm of transfer function between signals w and z.

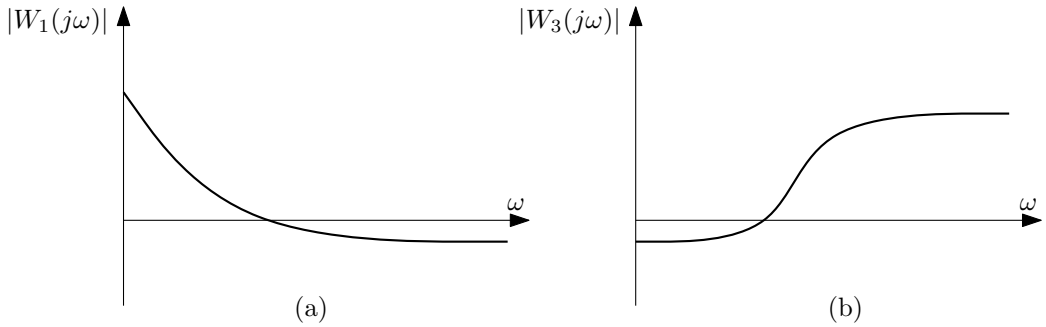


Figure 3.31: Proposition of W_1 (a) and W_3 (b) weighting function modules, which satisfy the conditions from 3.3.5

To find the optimal controller $K(s)$ for a particular system for given weighting functions, one can solve the algebraic Riccati equation, for example by using MATLAB *hinfsyn* function, as it is shown in example in listing 3.2.

Listing 3.2: Matlab source code for computing $\mathcal{H}_\infty$ controller

```
%% plant augmentation for use in weighted mixed-sensitivity
%% where W1(s) is penalizing the error signal,
%% W2(s) is penalizing the control signal
%% and W3(s) is penalizing the output signal
H_sys=augw(P_continuous,W1,W2,W3);
%% function that computes a stabilizing H_infinity
%% optinal controller C_hinf
[C_hinf,clp,gam,info] = hinfsyn(H_sys,1,1,'GMAX',1.3,'GMIN',0.8);
```

3.3.6 Linear control for saturated input plant

Designing the control systems in previous sections, the Author was concentrated on the class of Linear Time-Invariant system (LTI). This class of controllers was selected intentionally. The LTI control systems can be designed using closed-loop convex analysis. They follow the principle of superposition (linearity and homogeneity) and have only one isolated equilibrium point or complete subspace as an equilibrium set. Moreover, the performance of linear controllers can be validated using tools such as Bode plot analysis, Nyquist plot analysis or many others well-established methods. LTI controller can be discretized and implement in digital processing system.

Although many aspects of control systems can be described using linear theory, some nonlinearities cannot be omitted in practice [5]. One of the particular type of nonlinearities are constraints. The linear control system has a form

$$\begin{aligned} \frac{\mathrm{d}x}{\mathrm{d}t} &= f(x,e), \\ u &= h(x,e), \end{aligned} \tag{3.56}$$

where $x \in \mathbb{R}^n$, $e \in \mathbb{R}^p$ and $u \in \mathbb{R}^q$. However, the control of PWM power converter assumes that the control signal (duty cycle) is limited, since $D \in [0,1]$. For a power converters that operate over a wide range of voltage or current, it is possible that the control value reaches the lower or upper limit. In that case the feedback loop is broken and the converter runs in open loop as long as control value remains saturated [6].

When the control system dynamics includes integration action, the state variable corresponding to integrator may continue to grow up until the system quits the saturation condition. Then, this "pumped" state variable begins to decrease which can take some time and results in a large transient. This effect is often called integrator windup. The method of eliminating integrator windup effect is called anti-windup technique. The problem of actuator saturation control is complex and addressed by many research works (see [34], [31]). One of the possible solution applicable for state space realization of LTI controller system is presented in this section.

Let us consider the model of a state space controller with an input error signal denoted by $e(t)$ and a saturated control output denoted by $u(t)$

$$\begin{aligned} \dot{x} &= \mathbf{A}x + \mathbf{B}e, \\ u &= \mathrm{sat}(\mathbf{C}x + \mathbf{D}e), \end{aligned} \tag{3.57}$$

where $\mathbf{A} \in \mathbb{R}^{n\times n}$, $\mathbf{B} \in \mathbb{R}^{n\times p}$, $\mathbf{C} \in \mathbb{R}^{q\times n}$ and $\mathbf{D} \in \mathbb{R}^{q\times p}$. The state space system can be enhanced by feedback loop that reduces state derivative in case when the output is saturated, as it is shown in Fig. 3.32.

$$\begin{aligned} \dot{x} &= \mathbf{A}x + \mathbf{B}e + \mathbf{K}(u - \mathbf{C}x - \mathbf{D}e), \\ u &= \mathrm{sat}(\mathbf{C}x + \mathbf{D}e), \end{aligned} \tag{3.58}$$

where $u \in \Omega \subset \mathbb{R}^q$. Matrix $\mathbf{K} \in \mathbb{R}^{n\times q}$ should be chosen such a way that the matrix $(\mathbf{A} - \mathbf{KC})$ has desired, stable eigenvalues.

$$\mathrm{Re}(\lambda) < 0 \quad \forall\lambda : \det\left(\mathbf{A} - \mathbf{KC} - \lambda\mathbf{I}\right) = 0. \tag{3.59}$$

Hence, the above realization can prevent integration windup when the actuator is saturated.

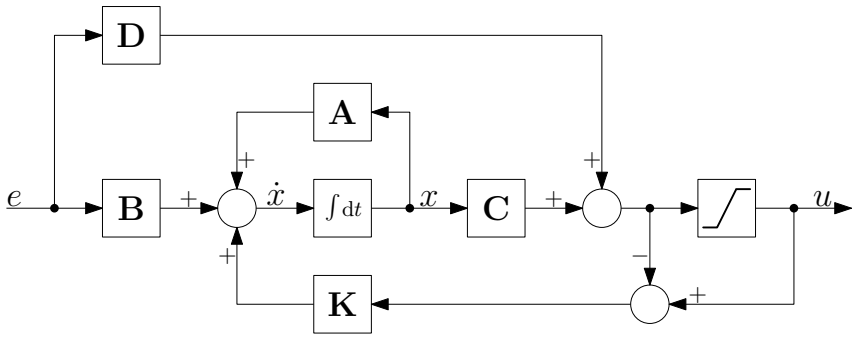


Figure 3.32: State space realization with anti-windup loop

3.3.7 Summary

The previous section gave an introduction to the topic of the robust linear controller design for power electronic systems. Two methods of control were proposed: lead-lag compensator and $\mathcal{H}_\infty$ controller.

It has been shown that robust lead-lag compensator can be easily synthesized using first-order elementary components. As a result, second-order differential linear system can be used for compensation, which can be then implemented either in analog or digital technology. However, due to simplicity, lead-lag compensator does not give control designer much freedom in shaping the loop transfer function. There are many variations and modification of classical PID controller. One of them, which gain a lot of interest in recent years, is called Fractional-Order PID (FOPID) and is based on non-integer calculus (see i.e. [16, 17]). This approach can help in obtaining robustness or iso-damping property, but on the other hand can complicate the realization due to the fact that fractional order system has infinite dimension and does not reflect semigroup property.

The second method of robust controller design discussed in the section is $\mathcal{H}_\infty$ compensator. Its performance and robustness greatly depends on designed weighting functions $W_1(s)$, $W_2(s)$ and $W_3(s)$. Moreover, the order of controller also depends on the orders of weighting functions and increases with them.

Two methods of controller design described in this section: Lead-lag and $\mathcal{H}_\infty$ will be realized, implemented and verified in the next chapter.

3.4 Modulator

The digital control system operates on physical value numerical representations, which are discrete in time and quantized in amplitude signal. However, the power stage of electronic converter switches between two binary states only. The power transistors are driven by binary (two-level) signal. The purpose of modulator is to generate a binary waveform called carrier signal, that carry the low-frequency information signal. All kind of modulation schemes for switching-mode power converters are designed to generate a pulse sequence, results in an average value equal to a present value of the target reference signal [30]. In this section two different modulation strategies are compared with respect to harmonic distortion, number of commutations and spectrum.

So far many variations of the conventional pulse-width modulators have been developed, for example sigma–delta digital pulsewidth modulator [48, 37] or a delta modulator [12, 13]. The latter approach is particularly interesting due to low complexity and high effective resolution without the need for a high frequency clock. In this section, the delta modulator is compared with conventional PWM technique.

The choice of appropriate modulation scheme as well as an adequate switching frequency is important and can result in reduction of converters switching losses, improvement of the power quality and potential reduction of electromagnetic interference due to spread-spectrum effects.

3.4.1 Pulse-width modulator

The PWM is a principal and well-known technique of driving switching-mode power converters. This modulation strategy varies the duty cycle of a constant frequency square wave to achieve the expected current or voltage average value. Let us define logic signal $\gamma(t)$, which is periodic and takes only two values: 1 or 0. The fundamental concept of PWM is based on the volt-second balance conservation – the integral of the voltage waveform over time [30]. This principle refers to current converters as well.

As it was introduced in (eq. 3.8), the average value $\langle\gamma\rangle_{T_\mathrm{s}}$ is equal to

$$\langle\gamma\rangle_{T_\mathrm{s}} = \frac{1}{T_\mathrm{s}} \int_{t-T_\mathrm{s}}^{t} \gamma(\tau)\mathrm{d}\tau. \tag{3.60}$$

The duty cycle D is defined as a fraction of the switching period T_s when the signal $\gamma(t)$ is equal to 1. Hence, the value of the pulse wave $\gamma(t)$ is equal to 1 for $kT_\mathrm{s} < t \leq kT_\mathrm{s} + D\,T_\mathrm{s}$ and $\gamma(t)$ equals to 0 for $kT_\mathrm{s} + D\,T_\mathrm{s} < t \leq (k+1)T_\mathrm{s}$ for $k \in \mathbb{N}$. The integral from (eq. 3.60) can be split into two subintegrals (eq. 3.61). From (eq. 3.61) follows the expected result, that the average value of the signal $\gamma(t)$ is equal to the duty cycle D.

$$\langle\gamma\rangle_{T_\mathrm{s}} = \frac{1}{T_\mathrm{s}}\left(\int_{t-T_\mathrm{s}}^{t-DT_\mathrm{s}} \gamma(\tau)\mathrm{d}\tau + \int_{t-DT_\mathrm{s}}^{t} \gamma(\tau)\mathrm{d}\tau\right) = \frac{1}{T_\mathrm{s}}\int_{t-DT_\mathrm{s}}^{t} \mathrm{d}\tau = D \tag{3.61}$$

The simplest realization of pulse-width modulation is based on comparison of a low-frequency target waveform (control signal) against high-frequency carrier waveform. In Fig. 3.33 a sawtooth wave for a carrier signal realization is employed as an example.

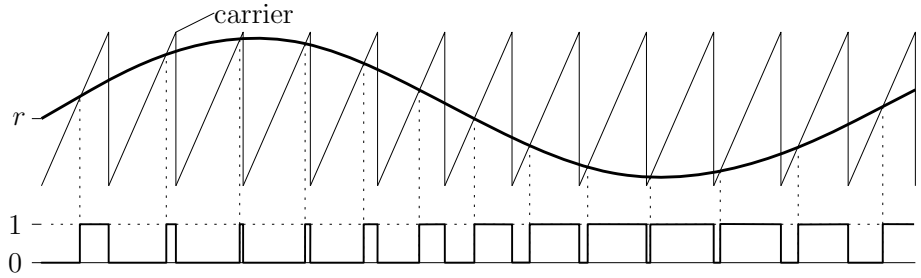


Figure 3.33: PWM waveform (bottom) generated from comparison of low frequency envelope signal with high frequency carrier signal (sawtooth)

3.4.2 Delta modulator

Delta modulation is another technique of producing binary (two-level) waveform that alternates between two discrete states. In contrast to the conventional PWM, the Delta modulation is asynchronous. It means that it does not have a constant switching frequency f_s (switching period T_s) and depends on actual value of the input signal as well as the internal state.

The delta modulator generates the pulse waveform of two states, similarly as in classical PWM case: $\Psi \in \{0, 1\}$. This modulator operates in a closed-loop: the filtered signal $p(t) = g_\mathrm{LP}(t) * \Psi(t)$ is subtracted from the reference signal $D(t)$ and compared within the upper and lower boundary levels ($f * g$ denotes a convolution of functions f and g). In control theory this technique is also known as bang-bang control. Fig. 3.34 presents the block diagram of delta modulator.

When the $D(t) - p(t)$ signal is rising and reaches the threshold $+h$, the output signal Ψ switches from 0 to 1. Analogically, when the $D(t) - p(t)$ signal is decreasing and crosses the $-h$ point, then the output signal Ψ switches from 1 to 0. This action is illustrated in Fig. 3.35.

The generated pulse signal $\Psi(t)$ changes the state in time instants, when one of the following conditions is satisfied:

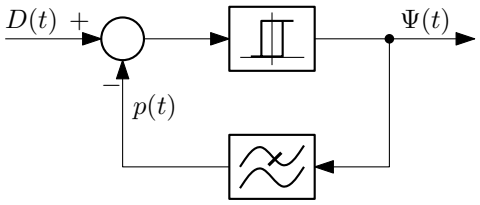


Figure 3.34: The delta modulator closed-loop block diagram

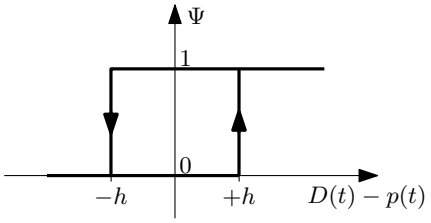


Figure 3.35: Delta loop

$$\begin{aligned} \Psi(t) &= 0 \qquad \text{if } \; D(t) - p(t) \leq -h \; \wedge \; \Psi(t^-) = 1 \\ \Psi(t) &= 1 \qquad \text{if } \; D(t) - p(t) \geq h \; \wedge \; \Psi(t^-) = 0 \end{aligned} \tag{3.62}$$

where h denotes half of the hysteretic band and t^- denotes the time instant immediately preceding the switching event. The operation principles are demonstrated in Fig. 3.36.

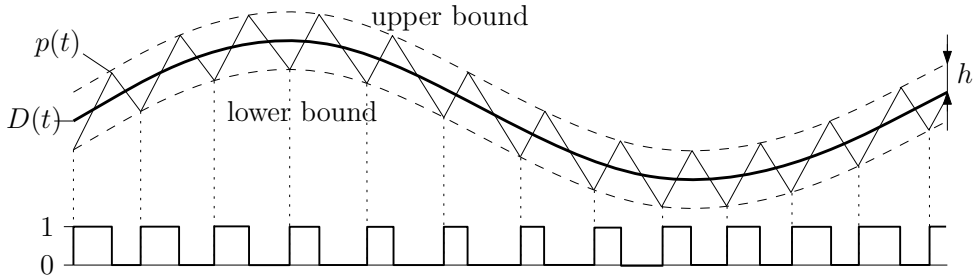


Figure 3.36: The delta modulator waveform

Let us design the filter block in Fig. 3.34 as a basic continuous-time first-order low-pass filter of unity DC gain. Then, the change of the filtered signal $p(t)$ in time domain can be written as follows

$$\frac{\mathrm{d}p}{\mathrm{d}t} = \frac{\Psi - p}{\tau_{\mathrm{LP}}}, \tag{3.63}$$

From the evolution of hysteretic curve in Fig. 3.36 one can employ the approximation of the derivative and formulate the following relationships

$$\begin{cases} \frac{2h}{T_+} \approx \frac{\mathrm{d}p(t)}{\mathrm{d}t} - \frac{\mathrm{d}D(t)}{\mathrm{d}t} \\ -\frac{2h}{T_-} \approx \frac{\mathrm{d}p(t)}{\mathrm{d}t} - \frac{\mathrm{d}D(t)}{\mathrm{d}t} \end{cases}, \tag{3.64}$$

where periods T_+ and T_- refer to periods of time when the generated signal $\Psi(t)$ is equal to 1 and 0, respectively.

Hence, applying the filter derivative equation (eq. 3.63) for relationships (eq. 3.64) the two periods T_- and T_+ can be approximated with

$$\begin{cases} T_+ \approx \frac{2h\tau_{\mathrm{LP}}}{1 - D(t) - \tau_{\mathrm{LP}}\frac{\mathrm{d}D(t)}{\mathrm{d}t}} \\ T_- \approx \frac{2h\tau_{\mathrm{LP}}}{D(t) + \tau_{\mathrm{LP}}\frac{\mathrm{d}D(t)}{\mathrm{d}t}} \end{cases}. \tag{3.65}$$

It is interesting, how each of the T_1 and T_2 periods depend on $D(t)$ signal and its variation. The sum of two periods T_1 and T_2 lead us to calculate the variable switching period T_s

$$T_\mathrm{s} = T_+ + T_- = \frac{2h\tau_{\mathrm{LP}}}{D - D^2 + \tau_{\mathrm{LP}}\frac{\mathrm{d}D}{\mathrm{d}t}\left(1 - 2D - \tau_{\mathrm{LP}}\frac{\mathrm{d}D}{\mathrm{d}t}\right)}. \tag{3.66}$$

When the signal $D(t)$ is constant ($\frac{\mathrm{d}D}{\mathrm{d}t} = 0$) for a single switching period, equation (eq. 3.66) can be simplified to

$$T_\mathrm{s} = T_+ + T_- = \frac{2h\tau_{\mathrm{LP}}}{D - D^2}. \tag{3.67}$$

Now, it can be seen that analogically to PWM modulation, the average value of $\Psi(t)$ depends only on $D(t)$, provided that $\frac{\mathrm{d}D}{\mathrm{d}t} = 0$,

$$\langle\Psi\rangle_{T_\mathrm{s}} = \int_{t-T_\mathrm{s}(t)}^{t} \Psi(t)\mathrm{d}\tau = \frac{T_+}{T_\mathrm{s}} = \frac{2h\tau_{\mathrm{LP}}}{1-D}\frac{D(1-D)}{2h\tau} = D. \tag{3.68}$$

Because the switching frequency for delta modulator is not constant and varies based on actual filtered signal $p(t)$ (as well as the reference signal D(t)), its spectrum in frequency domain will be spread, comparing to the conventional PWM technique [45]. This is the main advantage of this modulation technique, because the energy of electromagnetic interference for each frequency is lower. On the other hand, the widely-changing frequency might be the main disadvantage as well, due to problems in filtering of uncertain-frequency signal. Usually, the choice of which modulation technique is used depends on the particular application.

3.4.3 Summary

To highlight the differences between the conventional Pulse Width Modulation technique and the delta modulation, a computer simulation study was performed. Simulink model consisted of a reference signal – 50 Hz sine waveform, two analyzed modulators and a few tools for analysis: switchover counter, Total Harmonic Distortion (THD) meter, frequency meter and spectrum analyzer. The simulation horizon was set to 1 s, which equals to 50 full periods of the reference signal.

Table 3.2: The comparison of modulation techniques obtained with Simulink model

Modulator type	Number of switchovers	THD	Frequency band [kHz]
PWM	10000	0.02398	10
Delta	8900	0.02390	5.56 – 12.5

A switching frequency of conventional PWM was equal to $f_s = 10$ kHz, while delta modulation had a switching frequency in a range of 5.56 kHz to 12.5 kHz. As can be seen in Fig. 3.37, the spectrum of the former has high peaks in switching frequency and its harmonics, while the latter has slightly more uniform spectrum.

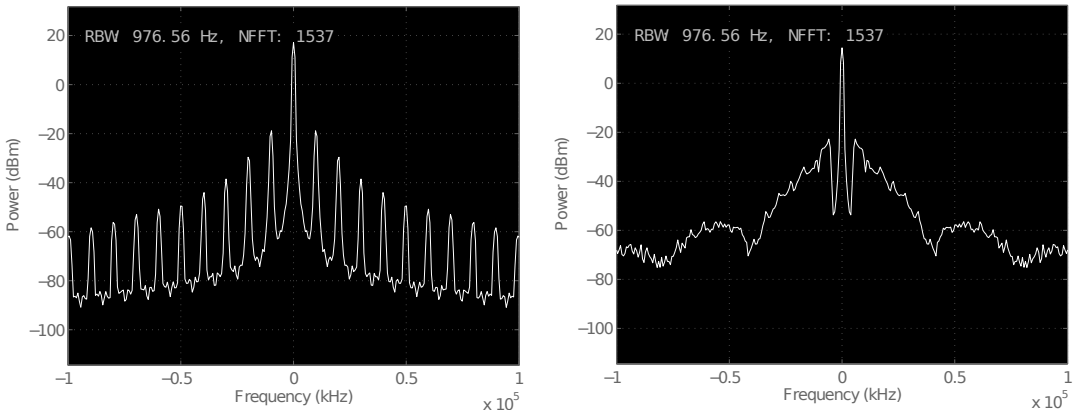


Figure 3.37: Comparison of power spectrum density between the classical PWM modulator (a) and the delta modulator (b). The classical PWM has a stationary spectrum, while the latter has time-varying spectrum and (b) presents only a snapshoot

The comparison of modulators is summarized in Tab. 3.2. One can notice that the number of switchovers is lower for delta modulator than for PWM, where this number is obviously equal to the switching frequency over 1 s. The switching frequency of PWM and parameters of delta modulation were selected in such a way that both systems generate similar distortions, quantified by THD factor. The majority of thermal power wasted

in semiconductor devices in switching converter applications depends on the number of switchovers, which is a good motivation to consider in practice the delta modulation. In spite of similar THD factor for both modulators, more uniform spectrum of delta modulation can make the sound of switching converter emitted by an inductor core due to magnetostriction less bothersome and produce more uniform spectrum of electromagnetic radiation.

4

Design and Verification of Digital Control System for Power Electronic Converter

Let us take into account the buck converter circuit, presented in Fig. 2.6. In practical realization, the dynamics of the circuit may be a little bit more complex than it was described in sec. 2.2, mainly due to additional components, e.g. a snubber. Real components exhibit parasitic effects – capacitor has certain inductance and dissipation factor, etc. The circuit diagram supplemented with the RC snubber is shown in Fig. 4.1.

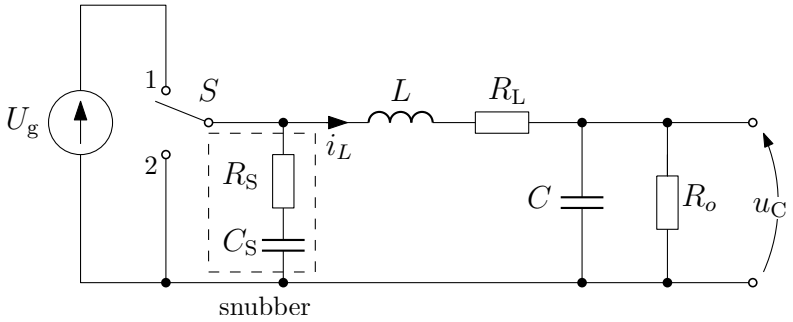


Figure 4.1: Buck converter power-stage circuit diagram with snubber

In this chapter, the numerical simulation model as well as physical model of the converter is described. The circuit presented in Fig. 4.1 was realized in practice, to validate the designed control system with a laboratory model.

4.1 Simulation model

The mathematical model of the converter is sufficient to design and analyze the control system. However, sometimes it is very convenient to take advantage of dedicated or universal simulation environment. This can accelerate the analysis, verify the analytical model and facilitate the parameters selection. Moreover, the simulation environment like MATLAB/Simulink can help in rapid prototyping of the control system by automated software source code generation utilities.

The Simulink software allows graphical programming and is intended for design and simulation of hybrid dynamical systems models. The Simscape toolbox belonging to Simulink library set consists of a comprehensive set of blocks for electric and electronic circuit modeling. They can be connected together with conventional Simulink blocks. Therefore, it is possible to design the control system in Simulink and verify it performance in Simscape subsystem.

The Author has implemented the buck converter model (see Fig. 4.1) in Simulink environment using Simscape toolbox. Its basic diagram is presented in Fig. 4.3. Simscape blocks can easily cooperate with common Simulink blocks, when electrical sensor blocks and physical signal converter blocks are used.

The nominal values of the key components are shown in Tab. 4.1. These values will be further used for laboratory model as well. The presented simulation model has one input signal corresponding to the duty cycle D and four measured values: supply voltage U_g, output voltage u_{C}, inductor current i_{L} and the output to input voltage ratio $\frac{u_{\mathrm{C}}}{U_{\mathrm{g}}}$ (Fig. 4.3). The model has two-level, hierarchical structure, where the converter is nested in the controller Simulink model. The simulation model is an approximation of the dynamics of a laboratory model (explained later in sec. 4.4), which allows validation of controller structures and its setting. This allows to reduce the risk of equipment damage by abnormal operation of the controller

Table 4.1: Nominal values of the system components

component	value	unit	description
L	1	mH	output filter inductor
R_{L}	0.105	Ω	inductor resistance
C	6.7	µF	output filter capacitor
C_{S}	100	pF	RC snubber capacitor
R_{S}	10	Ω	RC snubber resistor

The frequency response of the simulation model is presented in Fig. 4.2. The plot corresponds to the expected response of the second-order system, presented before in Fig. 2.11. For $R_{\mathrm{o}} = 43\ \Omega$, the resonant peak has magnitude of +10 dB and resonant frequency of about 1.9 kHz, which depends mostly on inductance L and capacitance C

according to a simplified equation (see also (eq. 2.21))

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{1}{(2R_oC)^2}} = 1924 \text{ Hz}. \tag{4.1}$$

The magnitude and phase responses end at 25 kHz, which is the Nyquist frequency of the discrete system for sampling frequency equal to 50 kHz. The analysis of accuracy

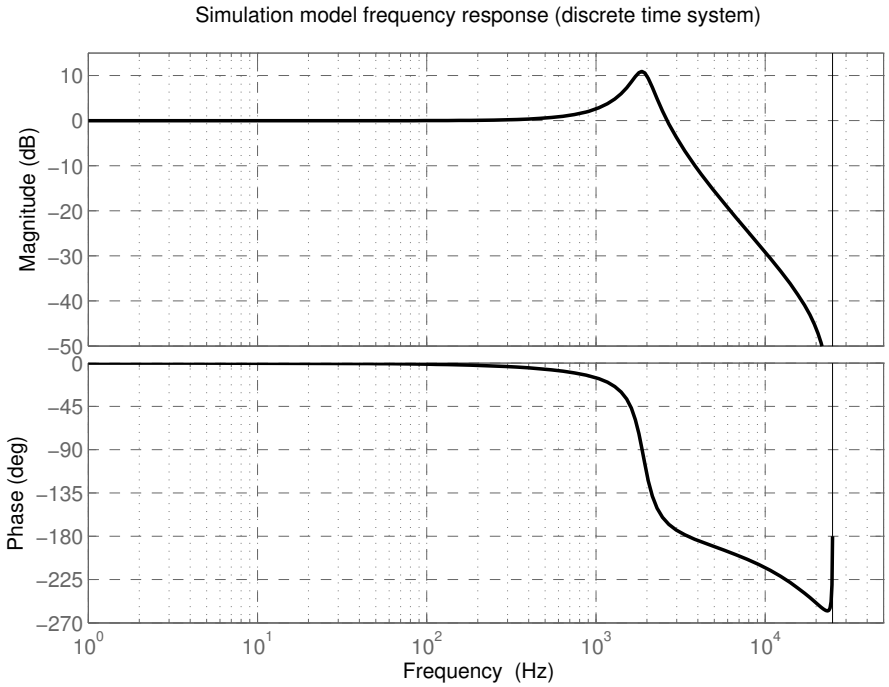


Figure 4.2: Frequency response of the discrete-time simulation model (sampling frequency at 50 kHz)

and comparison between simulation model and laboratory model is presented later in Fig. 4.16.

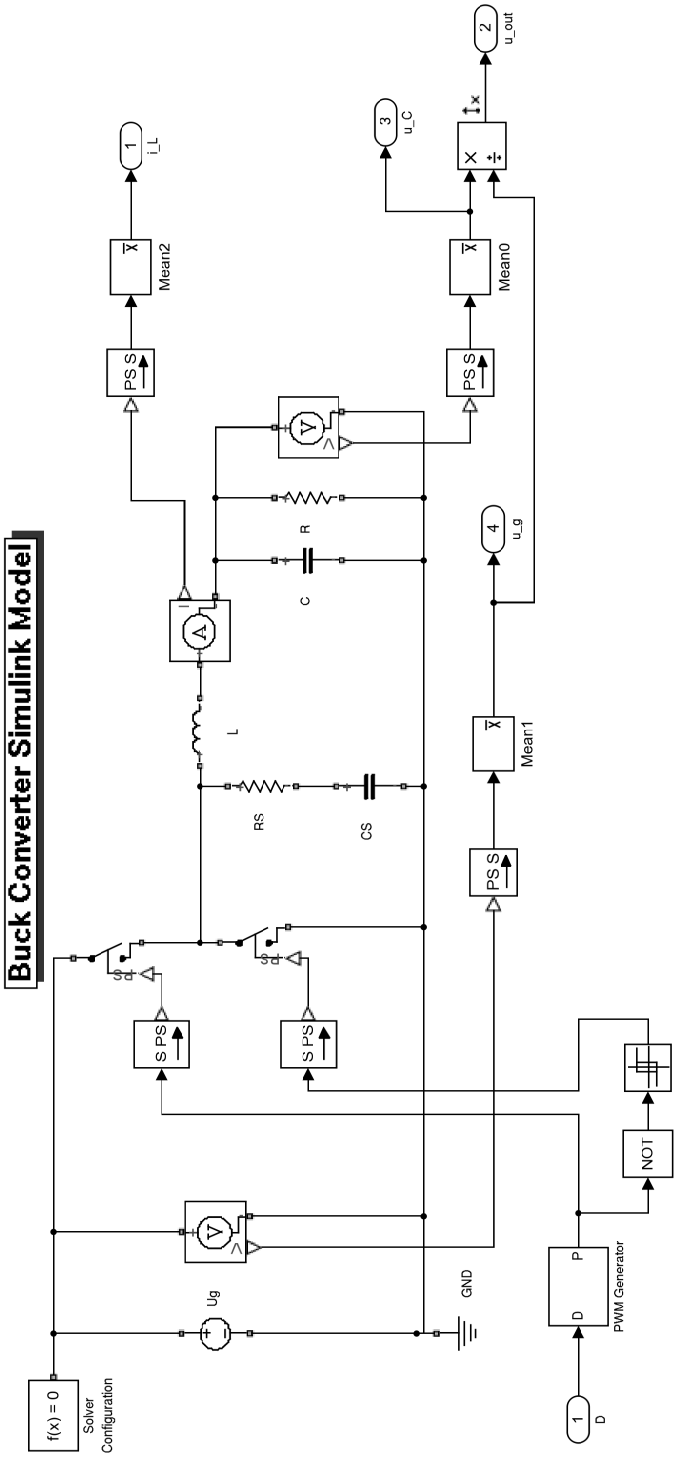


Figure 4.3: Simulink/Simscape diagram of the buck converter

4.2 Compensator design

4.2.1 Bandwidth

The design of power converter determines the switching frequency in order to meet a given specification, for example in terms of voltage and current ripples. Therefore, the sampling rate of analog signals should be equal or greater than switching frequency. The sampling rate does not need to be equal to the actuator frequency. Moreover, it is recommended for sampling rate to be an integer multiple of the switching frequency. This approach called "oversampling" can help in the digital filtering of the switching ripples in measured signal and therefore in avoiding aliasing effect. A digital control system with more than one source of clock signal is called multi-rate. Then, to decimate (reduce sampling rate), a band-limiting filter (decimator) is necessary, to avoid aliasing introduced in limited spectrum [2]. In the following case study, the moving average filter (proposed in sec. 3.2) is used.

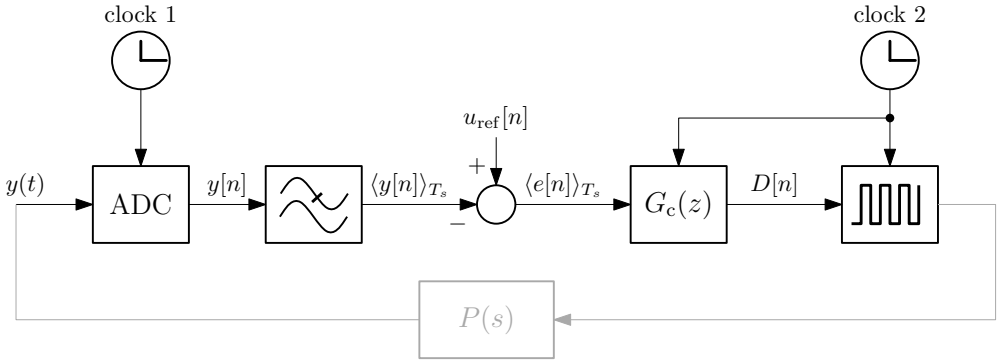


Figure 4.4: In multi-rate digital control system sampling rate of an analog-to-digital converter (clock 1) does not need to be equal to clock frequency of an actuator (clock 2)

Let us define the open-loop bandwidth as the frequency at which the loop gain is 0 dB. Above this frequency, the ratio of output to input signal amplitude is below 1, which means that system attenuates the signal. The digital signal processing theory restricts the bandwidth to the half of sampling rate, according to Nyquist-Shannon sampling theorem. However, this limitation is not sufficient for digital, discrete-time controllers for a continuous time plant. The proper selection of sampling rate or specifying bandwidth for fixed sampling rate is a fundamental problem. Some engineering recommendations suggest limiting the open-loop bandwidth to 10 to 20 times below sampling frequency, depending on a noise level in the feedback signal [27, 7]. This approach allows to neglect some delays in the control loop, including analog-to-digital conversion time, computer calculation time, modulator lag and other deterministic delays.

For the above reasons, the Author decided to establish the bandwidth of the control system to about 2 kHz which is 25 times lower frequency than actuator rate and 100

times lower frequency than sampling rate.

4.2.2 Controller specification and design

In order to make a fair comparison of controllers designed in various ways, it is necessary to establish common criteria to be met by each of them. The previous study highlighted the essence of robust control, so the following specification in Tab. 4.2 addresses the stability problem in the presence of uncertain plant model. The assumed target bandwidth is 2 kHz. Expected phase and gain margin are specified as 60° and 15 dB, respectively. The maximum magnitude of complementary sensitivity function $T(s)$ is expected to be below or equal to 1 (0 dB), while the maximum magnitude of sensitivity function $S(s)$ is expected to be below 1.5 (3.5 dB).

Table 4.2: Controller specification requirements – design assumption

property	value
mean steady state error	below 500 mV
bandwidth	below 2 kHz
phase margin	at least 60°
gain margin	at least 15 dB
$\|T(s)\|_\infty$	below or equal to 1
$\|S(s)\|_\infty$	below 1.5

Two previously described methods of linear control loop design allowed to achieve the robust controller of the converter: lead-lag compensator and $\mathcal{H}_\infty$ compensator. Defining a phase margin over 60° and a gain margin over 15 dB may be used to obtain a robust system. However, as it was written in 3.3.3, stability margin s_m is preferred to assess the robustness of the system. For the above specification, it is expected, that the stability margin should satisfy the following inequality

$$s_\mathrm{m} = \frac{1}{\|S(s)\|_\infty} > 0.66. \tag{4.2}$$

Three open-loop frequency responses of the system including response without compensator are presented in Bode plot (Fig. 4.5) and in Nyquist plot (Fig. 4.6). The sinusoidal excitation signal for analysis was in the range between 1 Hz and 100 kHz (some results have been already published in [19]).

From the Bode analysis it is possible to asses and verify if both controllers met the specification requirements from Tab. 4.2. The actual properties have been extracted and collected in Tab. 4.3. $\mathcal{H}_\infty$ controller has wider bandwidth and better phase margin than lead-lag compensator. The other properties are similar in both cases.

The following continuous-time linear system described in a state-space realization is used as a prototype for discrete implementation:

$$\begin{aligned} x(t) &= \mathbf{A}x(t) + \mathbf{B}e(t), \\ u(t) &= \mathbf{C}x(t) + \mathbf{D}e(t), \end{aligned} \tag{4.3}$$

where state matrices for lead-lag compensator are as follows

$$\begin{aligned} \mathbf{A_L} &= \begin{bmatrix} -251330 & 0 \\ 1 & 0 \end{bmatrix}, \qquad \mathbf{B_L} = \begin{bmatrix} 1 \\ 0 \end{bmatrix}, \\ \mathbf{C_L} &= \begin{bmatrix} -1.29\text{e}6 & 2.8532\text{e}8 \end{bmatrix}, \ \mathbf{D_L} = [5.599], \end{aligned} \tag{4.4}$$

and state matrices for $\mathcal{H}_\infty$ compensator are as follows

$$\begin{aligned} \mathbf{A_H} &= \begin{bmatrix} -7.54\text{e-}5 & 0 & 0 & 0 \\ 3.11\text{e}7 & -3.736\text{e}6 & -1.203\text{e}6 & -2.395\text{e}5 \\ 1.898\text{e}6 & 2.824\text{e}6 & -7.353\text{e}4 & -1.562\text{e}4 \\ 9.211\text{e-}37 & 0 & 1.515\text{e}5 & -5051 \end{bmatrix}, \qquad \mathbf{B_H} = \begin{bmatrix} 270.6 \\ 0 \\ 2.266\text{e-}18 \\ 2.806\text{e-}22 \end{bmatrix}, \\ \mathbf{C_H} &= \begin{bmatrix} 211 & 313.9 & -8.16 & -1.625 \end{bmatrix}, \ \mathbf{D_H} = [0]. \end{aligned} \tag{4.5}$$

Table 4.3: Actual properties of designed controllers

property	Lead-lag	$\mathcal{H}_\infty$
bandwidth	185 Hz	510 Hz
phase margin	70.59°	79.69°
gain margin	15.12 dB	15.11 dB
$\|T(s)\|_\infty$	0.99	0.99
$\|S(s)\|_\infty$	1.50	1.15

The preferred form of the system for realization in hardware is a state-space representation. But before a system can be implemented in hardware, the state space representation of continuous-time systems has to be discretized. Tustin approximation scheme is very often chosen for discretization in order to achieve similar magnitude and phase characteristics to the analog prototype. Infinite number of state space realizations ($\mathbf{\Phi}$, $\mathbf{\Gamma}$, $\mathbf{C}$ and $\mathbf{D}$) correspond to a discrete transfer function. Once the discrete system is obtained and verified, it can be evolved into realization that better fits for numerical implementation – called minimal realization (see [50, 25]). For the example below a balanced realization of equal controllability and observability Gramian for stable poles was chosen (called balanced realization, see [35]).

Let us describe the discrete-time linear system in state space representation

$$\begin{aligned} x[k+1] &= \mathbf{\Phi}x[k] + \mathbf{\Gamma}e[k], \\ u[k] &= \mathbf{C}x[k] + \mathbf{D}e[k], \end{aligned} \tag{4.6}$$

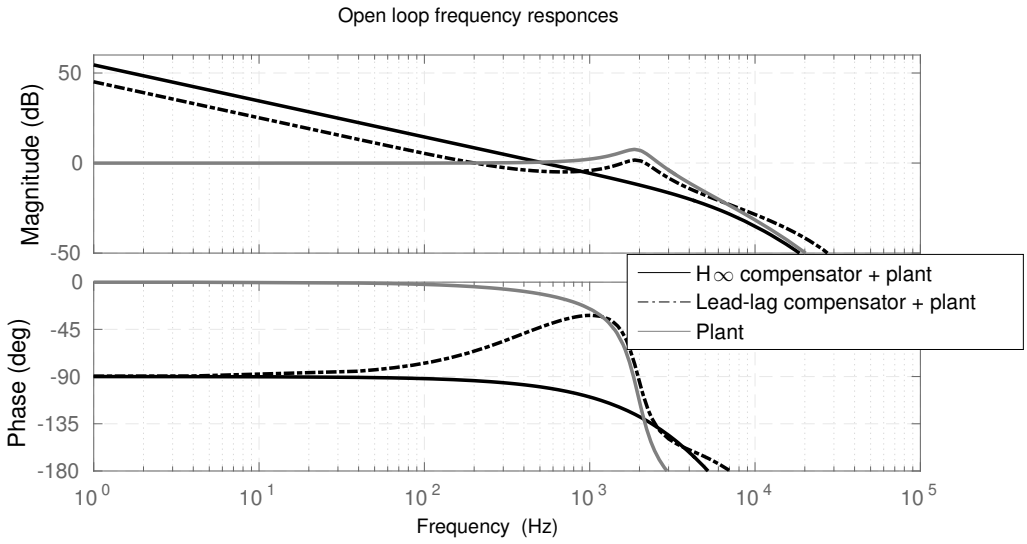


Figure 4.5: Bode plot of the continuous-time open-loop model with various robust control strategies

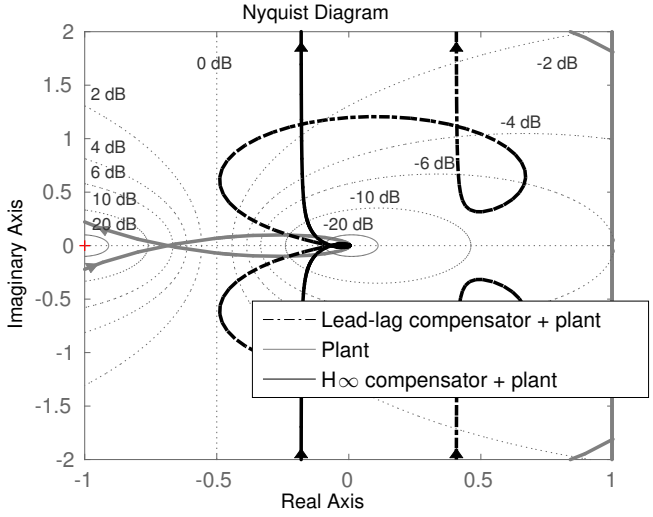


Figure 4.6: Nyquist plot of the continuous-time open-loop model with various robust control strategies

The discrete-time state space matrices of lead-lag compensator were derived

$$\begin{aligned} \mathbf{\Phi_L} &= \begin{bmatrix} 1 & 0 \\ 0 & -0.4307 \end{bmatrix}, \qquad \mathbf{\Gamma_L} = \begin{bmatrix} 1.977 \\ -1.445 \end{bmatrix}, \\ \mathbf{C_L} &= \begin{bmatrix} 0.01149 & 1.445 \end{bmatrix}, \ \mathbf{D_L} = [1.946], \end{aligned} \tag{4.7}$$

and poles, zeros and gain were calculated for the system (Tab. 4.4).

Table 4.4: Zeros and poles of discrete-time system for lead-lag compensator realization

Zeros	0.9474 0.6828
Poles	1 −0.4307
Gain	1.946

Similarly, the $\mathcal{H}_\infty$ compensator state space matrices can be written down

$$\mathbf{\Phi_H} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & -0.8759 & -0.2473 & -0.04661 \\ 0 & 0.2473 & 0.4997 & -0.1156 \\ 0 & 0.04661 & -0.1156 & -0.9572 \end{bmatrix}, \quad \mathbf{\Gamma_H} = \begin{bmatrix} 1.839 \\ 0.2912 \\ 0.5054 \\ 0.01623 \end{bmatrix}, \tag{4.8}$$

$$\mathbf{C_H} = \begin{bmatrix} 0.03635 & 0.2912 & -0.5054 & -0.01623 \end{bmatrix}, \ \mathbf{D_H} = [0.5668],$$

and zeros, poles and gain of the system are shown in Tab. 4.5.

Table 4.5: Zeros and poles of discrete-time system for $\mathcal{H}_\infty$ compensator realization

Zeros	$0.923\,165 + 0.22607j$ $0.923\,165 - 0.22607j$ −0.996 −1
Poles	0.999 99 0.464 96 −0.893 34 −0.904 89
Gain	0.5668

The quality of discrete-time system can be assessed by the comparison of its Bode characteristic to continuous-time prototype. Fig. 4.7 presents frequency responses of the lead-lag compensator realized in the continuous-time and discrete-time domains. Similarly, Fig. 4.8 presents frequency responses of the $\mathcal{H}_\infty$ compensator realized in the continuous-time and discrete-time domains. Because the responses of the systems are difficult to distinguish, an error between magnitude and phase characteristics of continuous and discrete time systems for both realizations is shown in Fig. 4.9. It can be seen from the plot, that the proposed discrete-time realizations have sufficient precision in terms of frequency characteristic mapping.

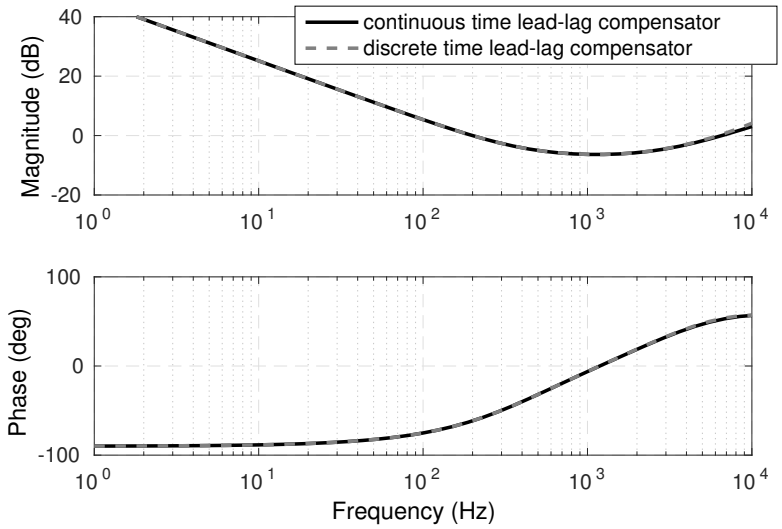


Figure 4.7: Bode characteristics of a continuous-time and a discrete-time realizations of lead-lag compensator

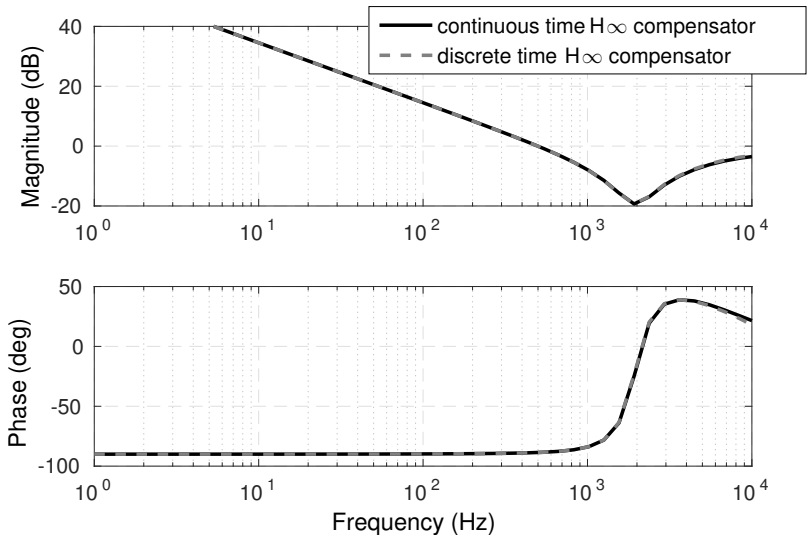


Figure 4.8: Bode characteristics of a continuous-time and a discrete-time realizations of $\mathcal{H}_\infty$ compensator

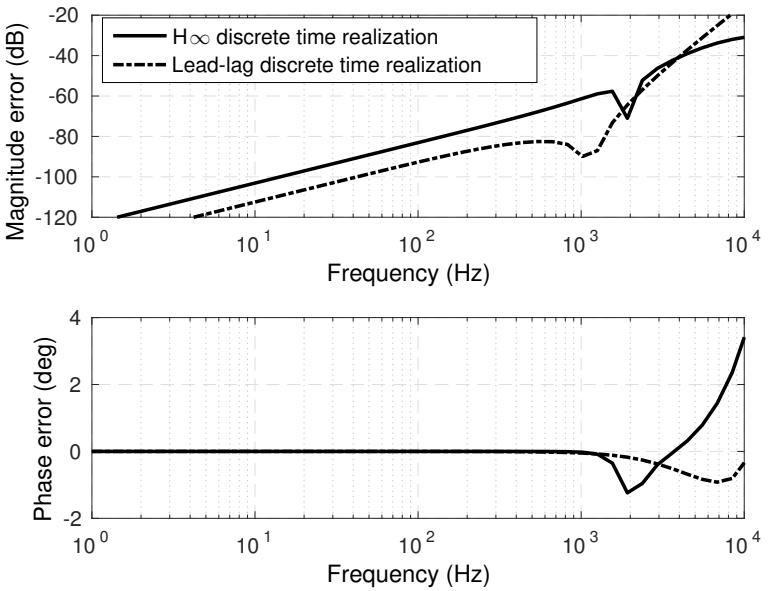


Figure 4.9: Absolute error of frequency responses for discrete-time realizations of $\mathcal{H}_\infty$ compensator and lead-lag compensator compared with the analog prototypes

4.3 Implementation

The implementation of selected control algorithm realizations and auxiliary functionalities (data acquisition, parameter updates etc.) was done in FPGA device. Reconfigurable devices are very suitable for demanding real-time signal processing and control applications with high sampling rate. In contrast to conventional computer, arithmetic and logic algorithms implemented in the FPGA are realized in hardware to allow parallel processing of complex expressions. The procedure of programming usually begins by problem definition. Then, the model of hardware design proposed for the posed problem can be basically obtained in two different ways. The first way is called behavioral model and refers to an approach based on functionality description. The second approach called structural model is focused towards design description by interconnection of basic hardware components. These two methods can also be combined – part of the system can be described structurally, while the rest behaviorally.

The efficient method of hardware design make use of Hardware Description Language (HDL). In the beginning, HDL was used only for describing the structure and behavior of logic circuits. With the development of digital technology, HDL began to be used also for the synthesis of digital systems. The most dominant HDL languages in electronic industry are VHDL and Verilog. The former was used by the Author for implementation

of low-level communication between FPGA device and peripherals like ADC or DAC. However, the majority of the logic description was done by the Author in Xilinx System Generator (XSG) – the higher level graphical interface hosted by MATLAB/Simulink environment. XSG tool constitutes the development platform with special Simulink library called Xilinx Blockset. The project designed in XSG can be simulated, evaluated and finally translated to VHDL or Verilog logic description.

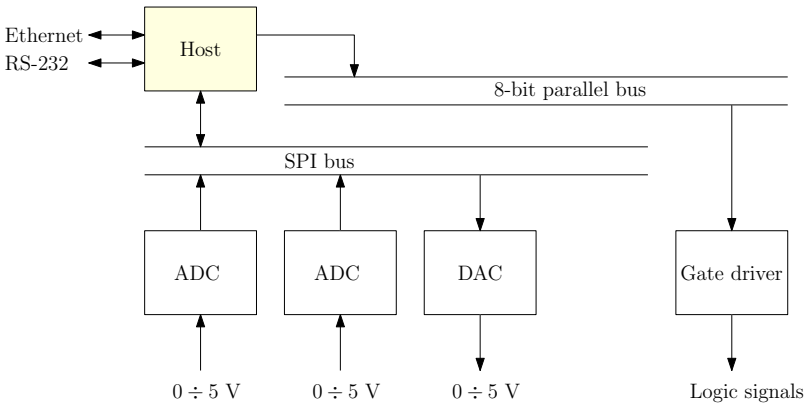


Figure 4.10: Simplified interconnection diagram of digital controller

A graphical representation of the top-level design flow diagram in the Xilinx System Generator for a proposed converter case study is shown in Fig. 4.13. Blocks called ADC and DAC are wrappers for behavioral description (called "Black box") for communication with peripherals, written directly in VHDL. Data exchange between host FPGA and peripherals is realized via synchronous protocol – Serial Peripheral Interface bus (SPI) (simplified interconnection diagram is shown in Fig. 4.10). To control SPI transmission, host device uses a control engine implemented as finite-state-machine in VHDL (illustrated in Fig. 4.11), while the corresponding source code is presented in listing 4.1.

Listing 4.1: A part of VHDL source code of SPI host controller

```
1  architecture Driver of spi_adc is
2    type MACHINE is (ready, execute);
3    signal STATE : MACHINE;
4    signal ASSERT_DATA : STD_LOGIC;
5    signal COUNTER : integer range 0 to 255;
6    signal CLK_TOGGLES : integer range 0 to 32;
7    signal LAST_RX_BIT : integer range 0 to 32;
8    signal RX_BUFF1 : STD_LOGIC_VECTOR(15 downto 0);
9    signal RX_BUFF2 : STD_LOGIC_VECTOR(15 downto 0);
10   signal RX_BUFF3 : STD_LOGIC_VECTOR(15 downto 0);
11   signal RX_BUFF4 : STD_LOGIC_VECTOR(15 downto 0);
12 begin
13   process (CLK, RST)
14   begin
15     if (RST = '1') then
```

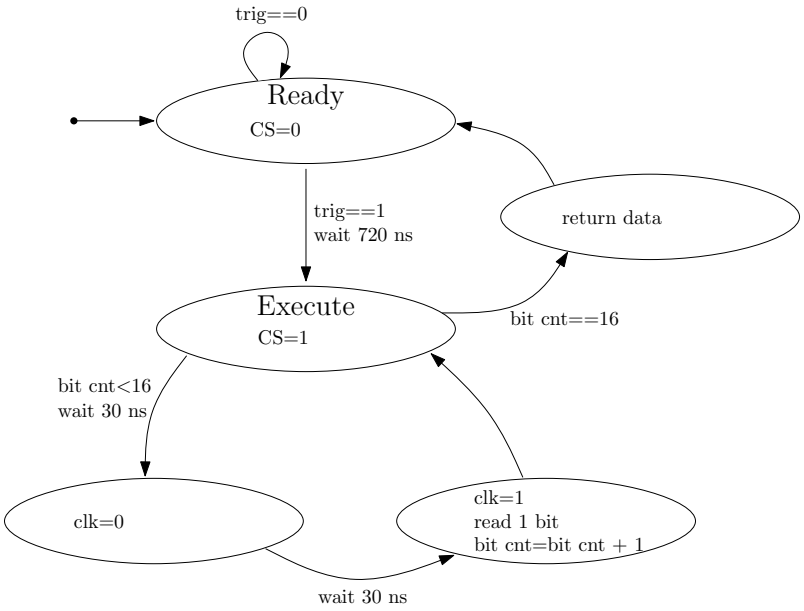


Figure 4.11: Simplified state transition diagram for SPI host controller

```
16        RX1 <= (others => '0');              -- clear output vectors
17        RX2 <= (others => '0');
18        RX3 <= (others => '0');
19        RX4 <= (others => '0');
20      STATE <= ready;
21
22      elsif (rising_edge(CLK)) then
23        case STATE is
24        when ready =>
25          BUSY <= '0';
26          CS <= '0';
27          if (TRIG = '1') then
28            BUSY <= '1';
29            SCLK <= '0';
30            CLK_TOGGLES <= 0;
31            COUNTER <= 72;                   -- wait 720 ns
32            ASSERT_DATA <= '1';
33            STATE <= execute;
34            LAST_RX_BIT <= 32;
35            CS <= '1';
36          else
37            STATE <= ready;
38          end if;
39        when execute =>
40          BUSY <= '1';
41          if(COUNTER = 0) then
42            COUNTER <= 6;                    -- wait 60 ns
43            ASSERT_DATA <= NOT ASSERT_DATA;
44            CLK_TOGGLES <= CLK_TOGGLES + 1;
```

```
45            if(CLK_TOGGLES <= 31 and BUSY = '1') then
46              SCLK <= not SCLK;
47            end if;
48            if (ASSERT_DATA = '0' and CLK_TOGGLES <= LAST_RX_BIT and
                  BUSY = '1') then
49              RX_BUFF1 <= RX_BUFF1(14 downto 0) & MAD1;
50              RX_BUFF2 <= RX_BUFF2(14 downto 0) & MAD2;
51              RX_BUFF3 <= RX_BUFF3(14 downto 0) & MAD3;
52              RX_BUFF4 <= RX_BUFF4(14 downto 0) & MAD4;
53            end if;
54
55            if (CLK_TOGGLES = LAST_RX_BIT) then
56              BUSY <= '0';
57              RX1 <= RX_BUFF1;
58              RX2 <= RX_BUFF2;
59              RX3 <= RX_BUFF3;
60              RX4 <= RX_BUFF4;
61              STATE <= ready;
62            else
63              STATE <= execute;
64            end if;
65          else
66            COUNTER <= COUNTER-1;          -- delay counter countdown
67            STATE <= execute;
68          end if;
69        end case;
70      end if;
71    end process;
72  end Driver;
```

A block called "To_EDK" realizes the functionality of signal acquisition in the fixed memory location. Precisely, it stores 16-bit vectors in First-In, First-Out (FIFO) buffers. Each buffer can hold up to 32768 values for further analysis.

The dynamical subsystem of the controller is implemented in a hierarchical block called “4th order system”. The lower layer of this block is depicted in Fig. 4.14 and contains the 4^{th} order state space realization of dynamical system implemented in floating-point arithmetic. The proposed implementation utilizes the basic blocks of addition and multiplication only (25 floating-point multipliers and 20 floating-point adders). All these mathematical operations are calculated in parallel and in this case study take only 500 ns. The most time-consuming single operation is a fixed-point division (between error signal and input voltage, located in Fig. 4.13 just before 4th order system) which takes 250 ns.

The hardware of designed controller is composed of functional modules, each of them is designed as a separate Printed Circuit Board (PCB). Peripheral boards – ADC, DAC and gate driver board meet standard Eurocard format, which can be plugged in subrack cassette. The front view of peripheral boards is presented in Appendix in Fig. A.5, Fig. A.6 and Fig. A.7. The assembled controller is shown in Fig. 4.12 [18].

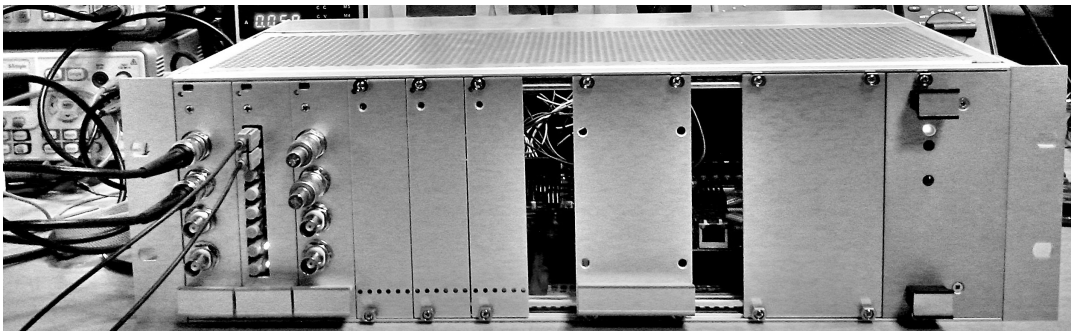


Figure 4.12: The front view of industry-ready FPGA-based real-time controller. The system can be extended with additional modules

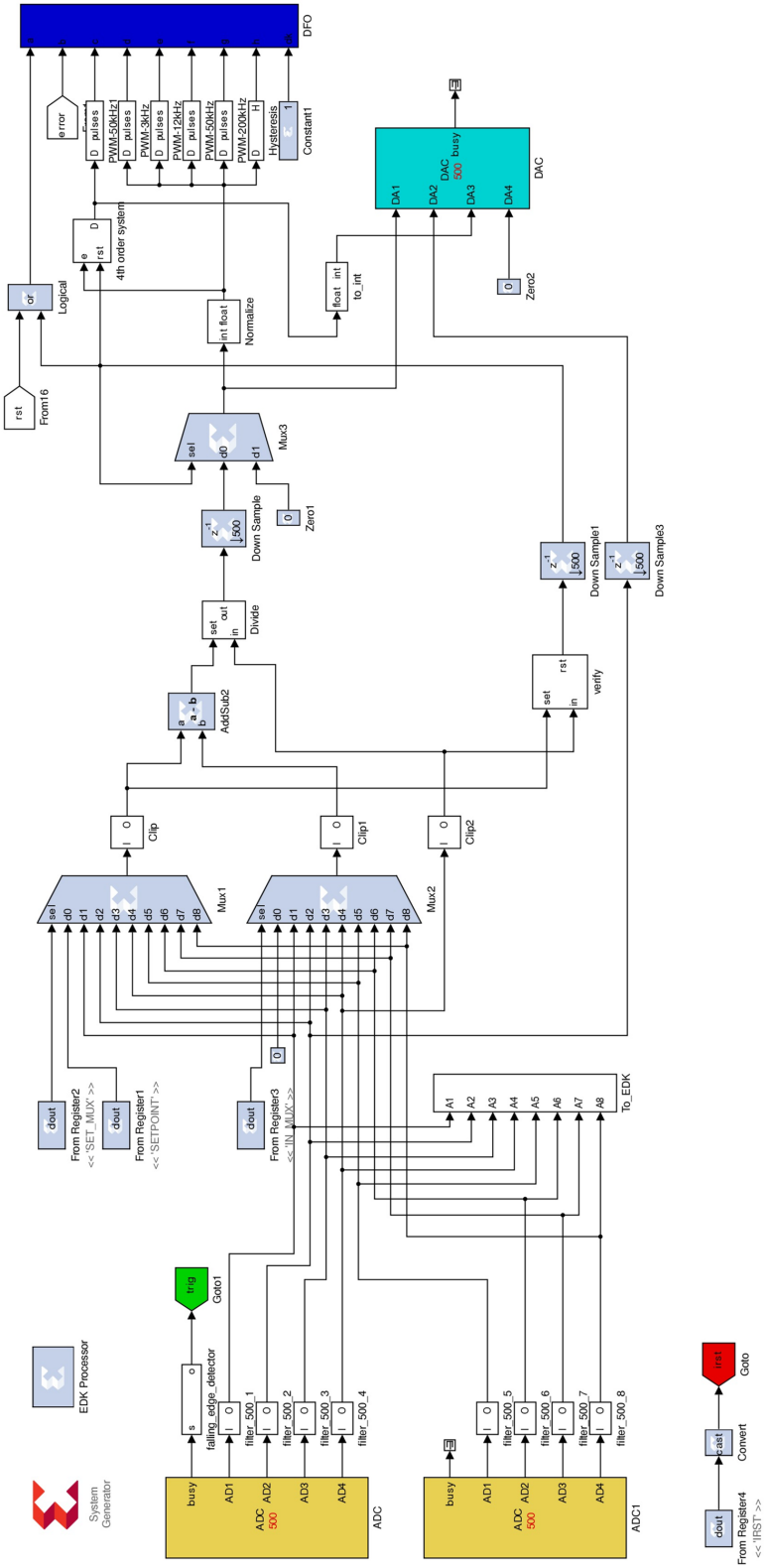


Figure 4.13: The top level of control system implementation dedicated for Xilinx FPGA device

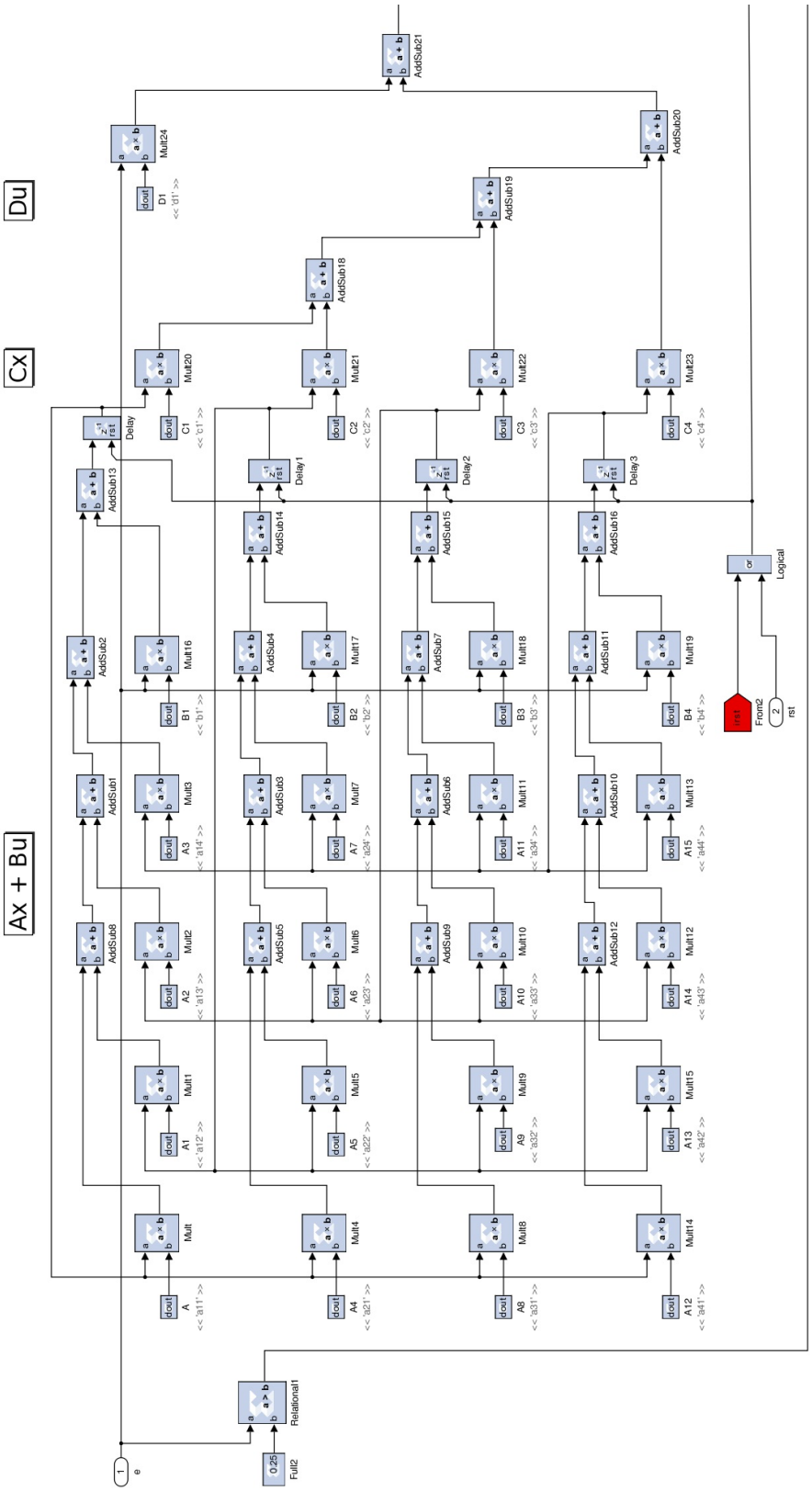


Figure 4.14: The implementation of state space system with floating-point arithmetic implemented for Xilinx FPGA device

4.4 Laboratory model

To validate the algorithms provided in this thesis, the laboratory model of the buck converter was designed and realized. The simplified circuit diagram of the buck converter power stage is identical as the one shown if Fig. 4.1 (a full complex diagram is presented in Appendix). The nominal values in simulation model are the same as the parameters of real components (Tab. 4.1). Both, MOSFET transistor and freewheeling diode are very fast semiconductor devices with breakdown voltage 1200 V and 650 V respectively. Inductor L has a core saturation characteristic presented in Fig. 4.15. Polypropylene capacitors C have tolerance of $\pm 5\%$.

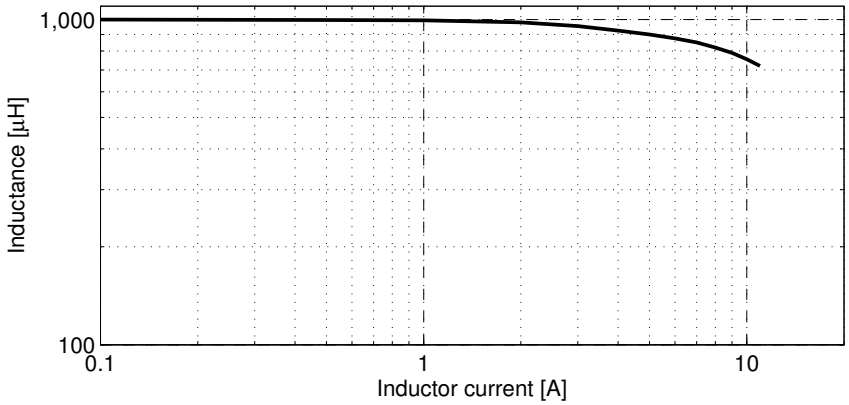


Figure 4.15: DC bias characteristic of "Feryster DEHF-42/1,00/11" inductor [24]. The magnetic permeability of the core decreases as the material approaches magnetic saturation, which reduces inductance

The frequency response of the laboratory model was identified and compared against the simulation model. The results are shown in Fig. 4.16. The solid black line represents physical model response, while the gray dashed line corresponds to mathematical model. Very close similarity of dynamic responses confirms the correctness of electronic circuit and accuracy against its mathematical model.

Both the simulation and the physical model took into account the supplementary dynamics of the moving average filter (comparing to the response in Fig. 4.2). Moreover, the time-delay introduced by a digital control system (analog-to-digital conversion time, computation time) was included in the plant model and can be observed on the phase characteristic for very high frequencies as an additional phase lag.

Another physical model verification was done based on a static plant characteristic. It is known that in general the averaged output voltage $\langle u_{\mathrm{C}} \rangle_{T_{\mathrm{s}}}$ should linearly depend on PWM duty cycle D (see sec. 2.2). The input-output characteristic of the physical model is shown in Fig. 4.17.

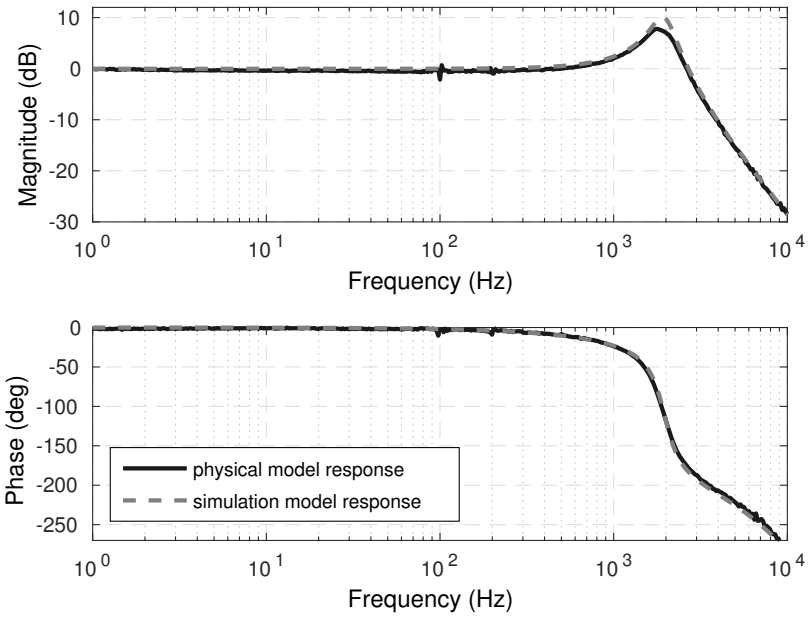


Figure 4.16: Frequency response of the laboratory model (solid line, switching frequency f_s=50 kHz) compared with the simulation model response (dashed line)

4.5 Laboratory test bench

To verify the performance of the designed laboratory model including all proposed control strategies, structures and settings, a dedicated test bench was prepared. The schematic diagram of a laboratory setup is shown in Fig. 4.18. The first transformer on the diagram (TR_1) is used to ensure galvanic isolation of the circuit from the power grid. This transformer has ratio 1:1, so it gives 230 V RMS, 50 Hz on the output. The transformer isolation is used to protect the circuit and the Author from electric shock and short circuits during experiments. Moreover, the isolation transformer helps to suppress electrical noise coming from the grid. Then the second transformer (autotransformer TR_2) is used to adjust the voltage in the 0–250 V range. A passive full bridge diode rectifier together with a capacitor C_g converts the AC to DC voltage for the buck converter. Passive rectifier is used purposely, to inject ripple at the DC bus. The amplitude of voltage ripple can be expressed by the equation

$$\Delta_{Ug} = \frac{i_g}{4 f_g C_g}. \tag{4.9}$$

For given condition the ripple frequency f_g is twice of the AC supply frequency, hence is equal to 100 Hz. For experimental purposes, the value of capacitor C_g was set to 400 µF. As an example, Fig. 4.19 presents the voltage ripple for input current i_g=2.3 A. For that

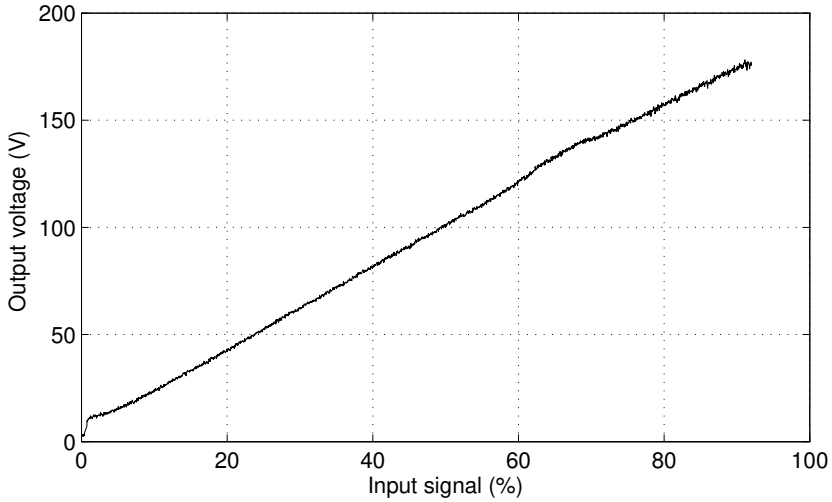


Figure 4.17: Static character of an open-loop system

case, the amplitude of voltage ripple equals about 26 V.

In practical application, the passive diode rectifiers are very common, so the Author wanted to determine how much the choice of control system strategy affects the PSRR. Moreover, the first thesis formulated in sec. 1.1 refers to the quality and reliability of energy supply. Therefore, the improvement of voltage quality needs to be proven. In many cases so large voltage ripple in DC output voltage as in presented example would be unacceptable. But in present case these ripples are purposely injected to the system and they are considered as disturbances. The intention was to verify the ability of active ripple voltage suppression by buck converter with fast feedback and feedforward responses. The property of input voltage disturbances suppression (PSRR) was discussed in sec. 2.4.

Finally, the experimental setup is composed of three load resistors R_0, R_1, R_2 of 43 Ω, 22 Ω and 22 Ω, respectively. Resistors R_1 and R_2 are connected via independent contractors and can be disconnected from the circuit at any time during test. The ability of changing the resistance of load allows to analyze the behavior of the system under changing load conditions. Photographs of the laboratory setup are presented in Fig. 4.20 and Fig. 4.21.

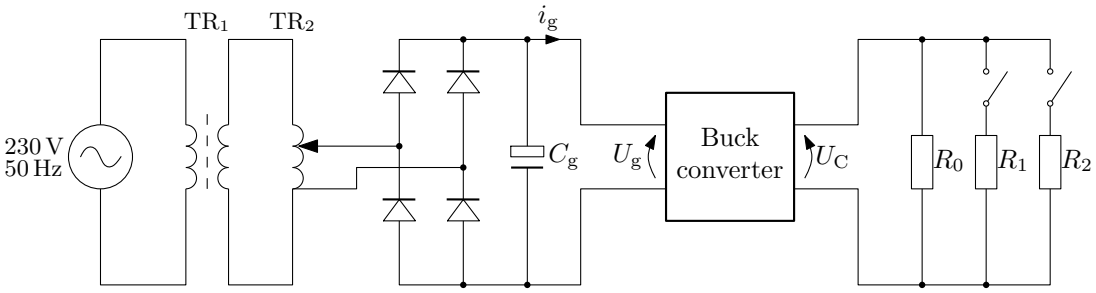


Figure 4.18: Laboratory test bench diagram

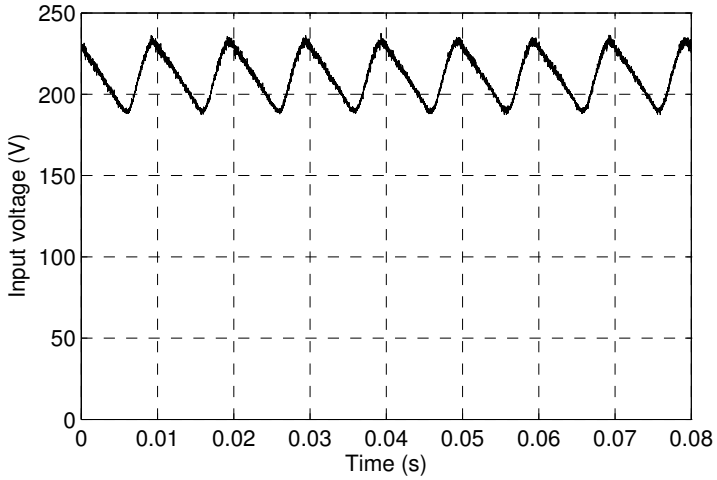


Figure 4.19: Input voltage ripples from full bridge diode rectifier for C_g=400 µF and i_g=2.3 A

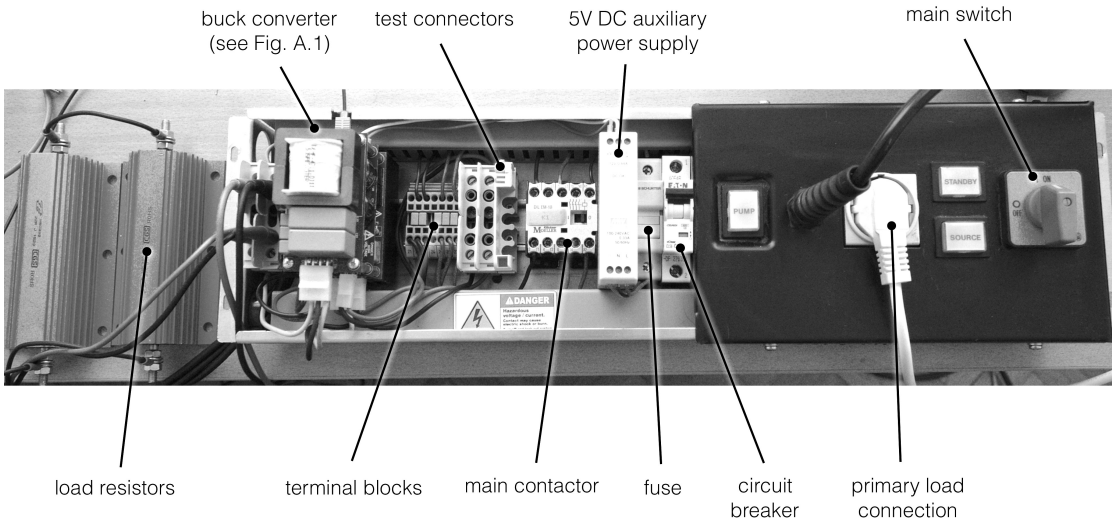


Figure 4.20: Buck converter embedded in a DIN TH-35 rail system

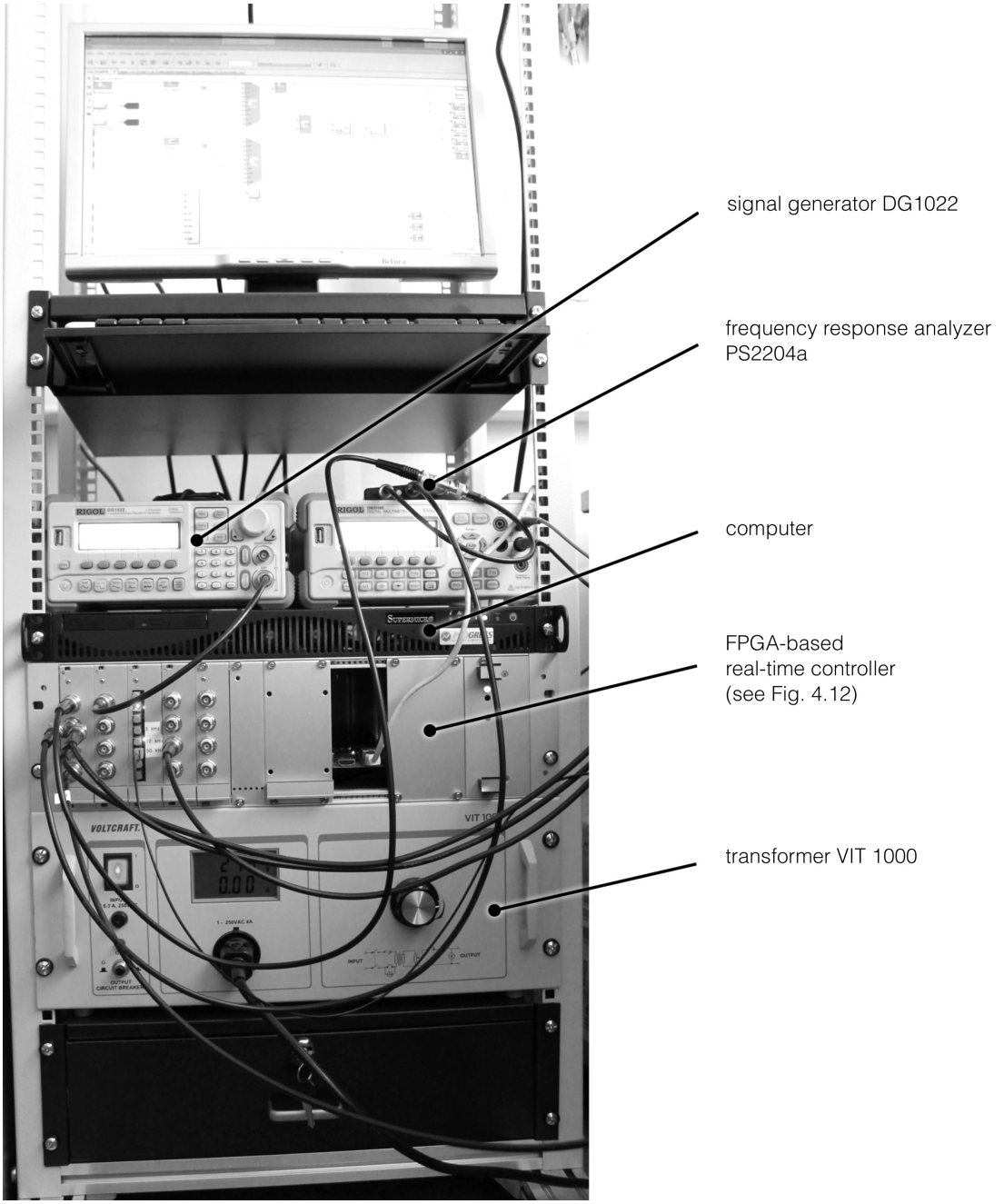


Figure 4.21: Laboratory test bench

4.6 Results

The test and verification scenario is designed to compare the synthesized and implemented digital control systems which meet the predefined specification requirements (see Tab. 4.2 and Tab. 4.3). The scenario includes the following test cases:

- closed loop frequency responses comparison,
- power supply rejection ratio for 50 Hz, 100 Hz and 200 Hz,
- closed loop step responses comparison,
- robustness to changes in load parameters.

Analysis of open-loop frequency response of the physical system can be impractical due to infinite or very high gain of a DC-component, which leads to saturation of the system. The Author decided to verify the frequency responses of the closed-loop system and compare it with the simulation model responses.

The analysis and evaluation of a control algorithm require an appropriate test bench. A schematic diagram of the measurement system is shown in Fig. 4.22. For the frequency response analysis, Picoscope PS2204a oscilloscope with spectrum analyzer and function generator was used. The internal wobulator logarithmically swept sinusoidal waveform from 1 Hz to 10 kHz. Based on acquired time series signals, the amplitude and phase of input and output signals were calculated and as a result, frequency responses from Fig. 4.23 and Fig. 4.24 were obtained. The reference DC component of set point value was equal to 75 V, while the amplitude of sinusoidal waveform component was equal to 20 V.

It can be seen from amplitude response, that $\mathcal{H}_\infty$ controller gives better results, which follows directly from the higher gain of an open-loop system for frequencies up to 1 kHz (see Fig. 4.5). The results confirm the correctness and accuracy of the simulation model.

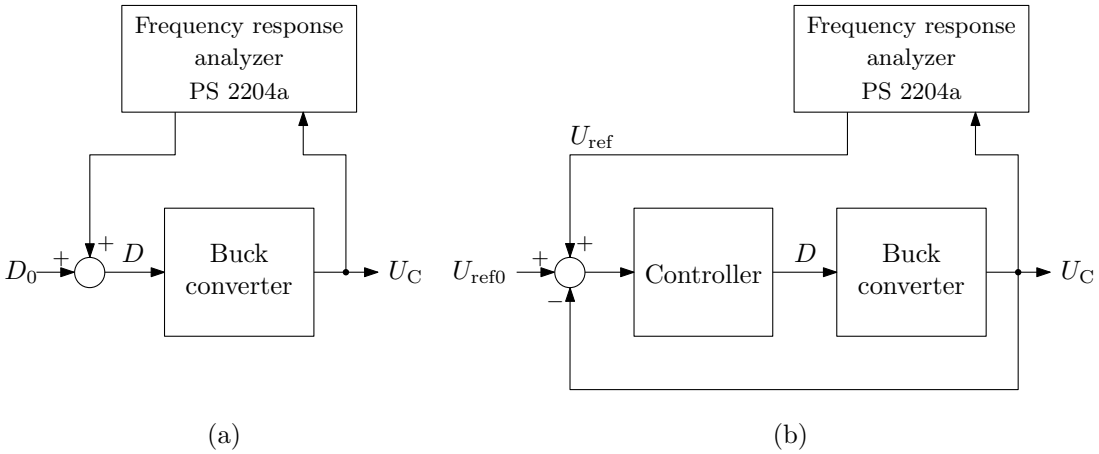


Figure 4.22: Frequency response analysis setup for a – open loop system, b – closed loop system

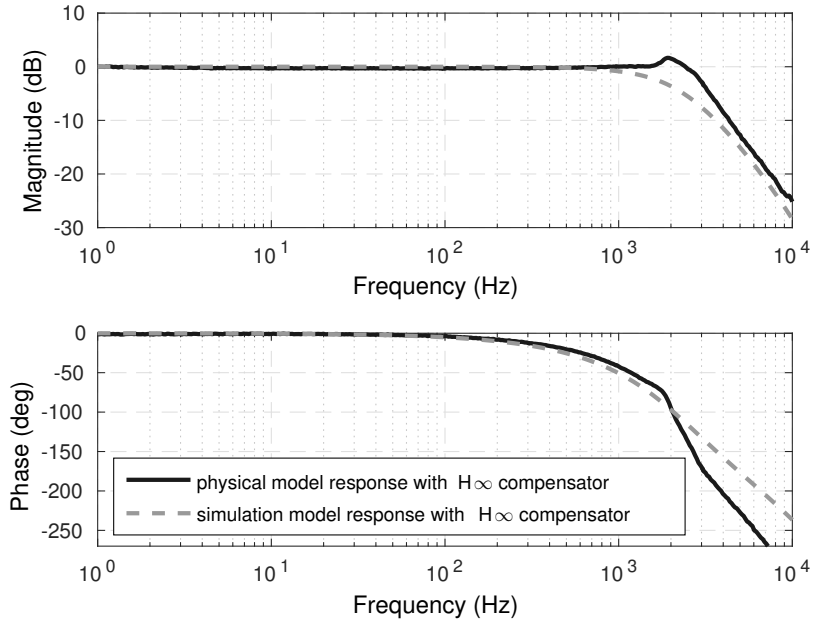


Figure 4.24: Frequency response of a closed-loop system with $\mathcal{H}_\infty$ compensator

The major quality factor for an output voltage in power electronic devices is the magnitude of unwanted frequency components. The amount of undesired signal components depend mostly on the quality of input voltage and the suppression of these components in closed-loop control system. For the purposes of experimental verification of the ability to attenuate unwanted signal components, the input voltage U_g has been intentionally

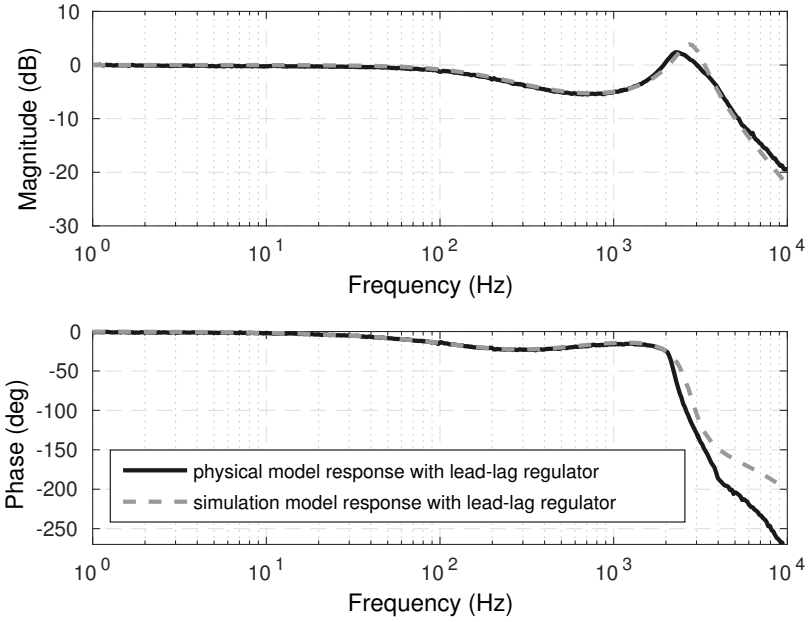


Figure 4.23: Frequency response of a closed-loop system with lead-lag compensator

distorted by 100 Hz ripples and its harmonics (mostly 200 Hz and 300 Hz). The results of attenuation for lead-lag controller and $\mathcal{H}_\infty$ controller are shown in Fig. 4.25 and Fig. 4.26, respectively. Fig. 4.27 presents filtered spectrum of both: $\mathcal{H}_\infty$ and lead-lag compensators.

The next test case was based on analysis of step response of the output voltage. During the test, the reference signal was switching between about 80 V and about 120 V. The test was done for the open loop system (only plant without controller) (Fig. 4.28), for the closed loop system with lead-lag compensator (Fig. 4.29) and for the system with $\mathcal{H}_\infty$ controller. (Fig. 4.29). The results of the experiment allowed to evaluate the settling time and overshoot value. Results are collected in Tab. 4.6.

The last test was conducted to evaluate robustness of the control system. Using experimental setup presented in Fig. 4.18, the value of load resistance was being rapidly changed between 20 Ω and 37 Ω. Evolution of voltage and current for the closed-loop system with lead-lag compensator and $\mathcal{H}_\infty$ controller are presented in Fig. 4.31 and Fig. 4.32, respectively.

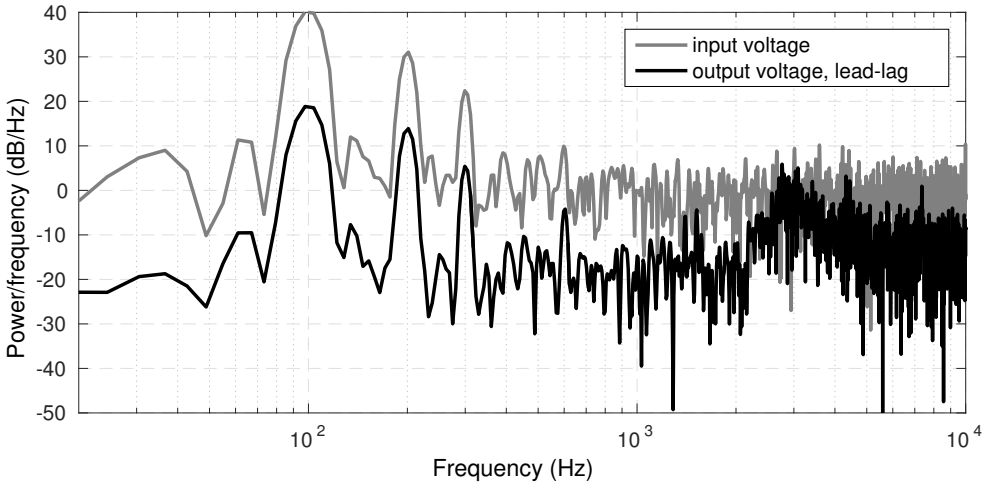


Figure 4.25: Power spectral density of an input and output voltage for buck converter driven by lead-lag controller

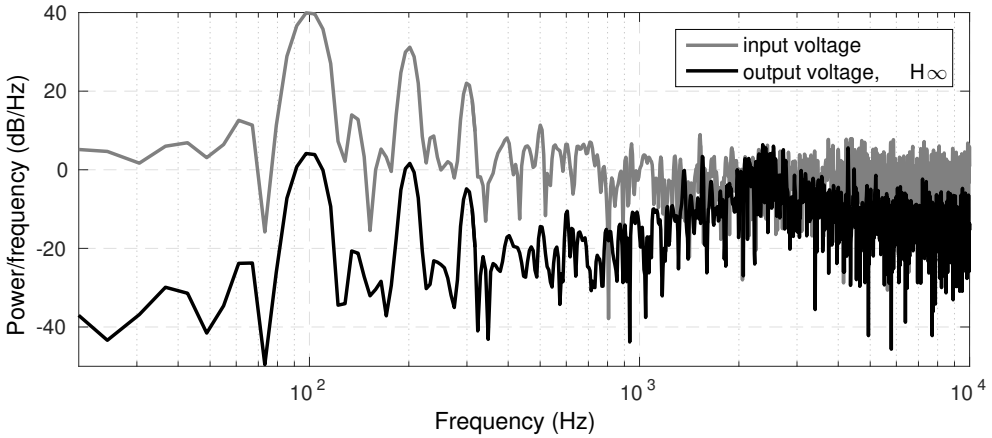


Figure 4.26: Power spectral density of an input and output voltage for buck converter driven by $\mathcal{H}_\infty$ controller

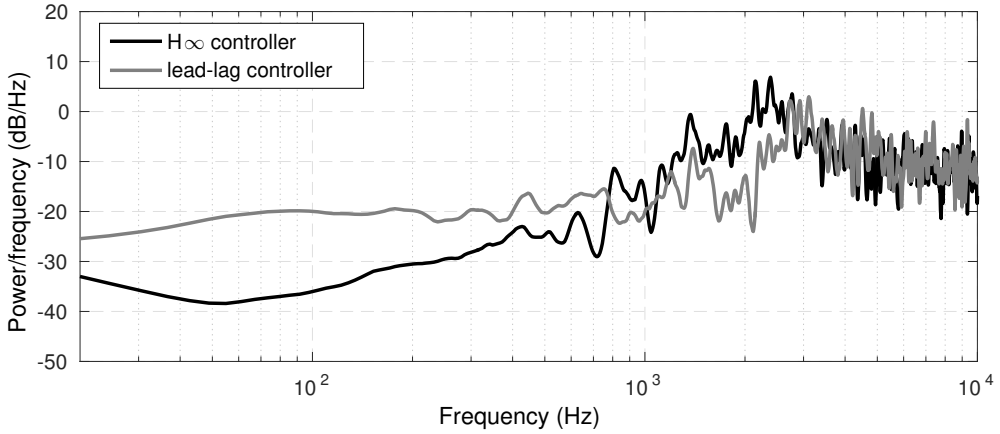


Figure 4.27: Power spectral density of power supply rejection ratio for $\mathcal{H}_\infty$ controller and lead-lag controller (averaged using mean filter of 10^{th} order)

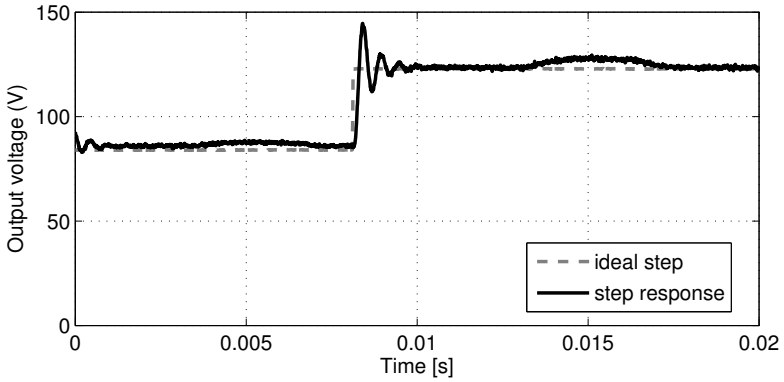


Figure 4.28: Experimental step output voltage response for the open loop system

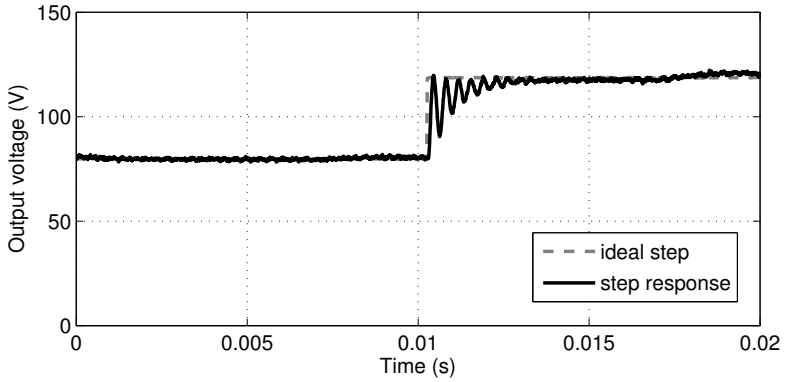


Figure 4.29: Experimental step output voltage response for the closed loop system with lead-lag compensator

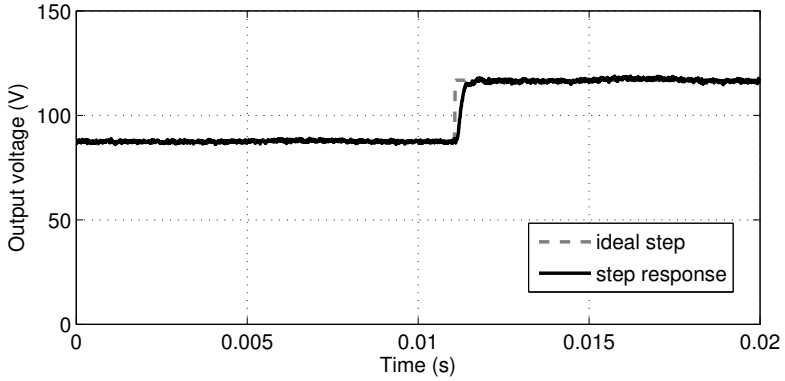


Figure 4.30: Experimental step output voltage response for the closed loop system with $\mathcal{H}_\infty$ compensator

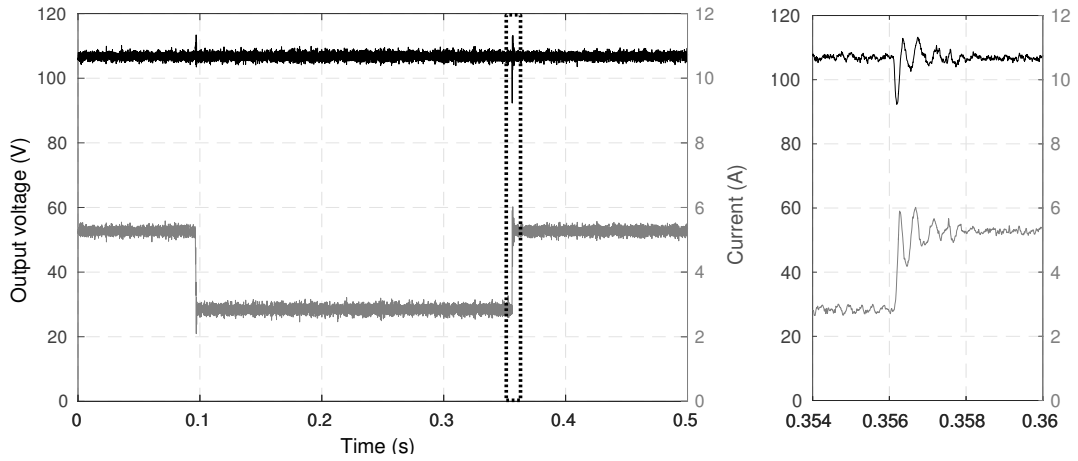


Figure 4.31: Experimental results of voltage and current response to load change from 2.8 A to 5.4 A for the closed loop system with lead-lag controller (on a right-hand side magnified sector)

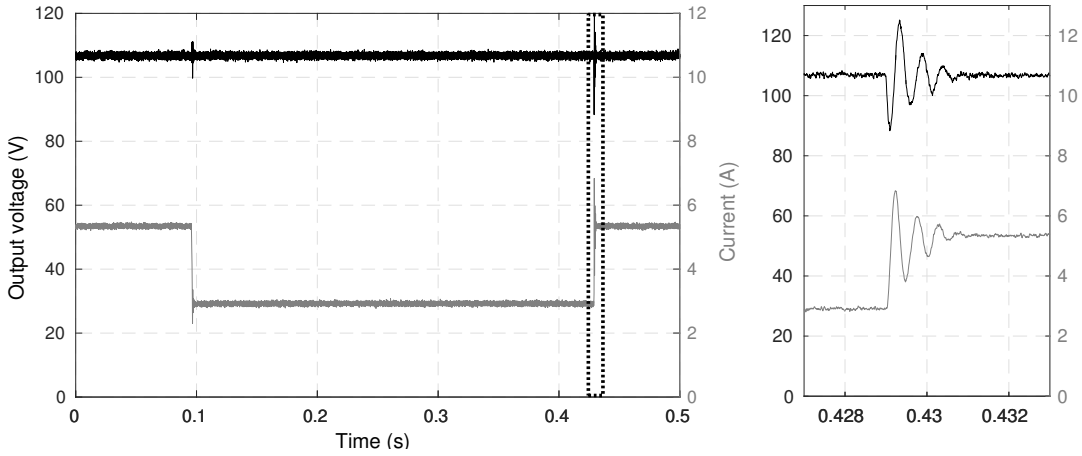


Figure 4.32: Experimental results of voltage and current response to load change from 2.8 A to 5.4 A for the closed loop system with $\mathcal{H}_\infty$ controller (on a right-hand side magnified sector)

Table 4.6: Result summary

Property	Lead-lag	$\mathcal{H}_\infty$
Mean steady state error	207 mV	49 mV
Settling time	3.2 ms	0.56 ms
Percent overshoot	0.7%	0%
PSRR @ 50 Hz	16 dB	45 dB
PSRR @ 100 Hz	21 dB	36 dB
PSRR @ 200 Hz	17 dB	30 dB

4.7 Summary

The case study of a buck converter system is universal, due to similarity of transfer functions to many other power converters (like inverter, DC motor chopper etc.). The experience earned during the experiments confirms that even complex controller structures (4th order system with feedforward loop from input supply voltage) working at very high sampling rate (50 kHz) can be effectively implemented in FPGA structure.

Identification of the physical buck converter confirms the excellent accuracy of the model proposed in chapter 2 for a wide frequency range. The spectra of input and output voltage signals obtained during experiments also confirm the proper operation of the moving average filter that is used to suppress the switching frequency and its harmonics.

The two different strategies of robust controller design were compared. As can be seen from frequency responses of the closed-loop system (Fig. 4.23 and Fig. 4.24), the $\mathcal{H}_\infty$ controller could make the amplitude response of considered system flat in very wide frequency range (up to 2 kHz). Above this frequency the roll-off of about 40 dB per decade occurs. The frequency response of the system with lead-lag compensator has plateau in 3^{rd} decade, which makes tracking property worse for this frequency range. The region, where the amplitude response of closed-loop systems drops is clearly visible in spectral plot Fig. 4.25 as well. $\mathcal{H}_\infty$ controller provides higher gain for low frequencies which make lower the steady-state error. It also gives higher suppression of 100 Hz component and higher harmonics and have better response for high frequency range. The step response of the system with $\mathcal{H}_\infty$ controller is without overshooting and ringing, comparing to the open-loop plant response and system with lead-lag compensator response.

Both analyzed control systems exhibit robustness property – the change in value of the load resistance did not destabilize the system. Moreover, the desired value of output voltage is restored very quickly. For both cases some overshoot in voltage and current can be seen (in Fig. 4.31 and Fig. 4.31), which may be caused by the saturation of the control signal.

Key values collected in Tab. 4.6 show a significant advantage of $\mathcal{H}_\infty$ controller over classical lead-lag approach. The suppression of disturbances introduced in the input voltage deserves a special attention. The $\mathcal{H}_\infty$ controller has higher PSRR ratio of 25 dB comparing to lead-lag compensator. These results encourage the use of this method in the design of control system for the purpose of power electronic converters.

5

Conclusions and Future Work

This thesis was devoted to a control system dedicated and adopted for power processing devices. It has been shown, that a well-designed controller ensures not only robustness to the varying parameters of the system, but can also improve the quality of energy supply and reduce unwanted components in low-frequency range. Methodology of digital realization of complex linear systems for very fast switching rate or commutation frequencies is in line with current trends. The Author believes that the verified practical results of this thesis can be valuable for industrial applications and might be implemented in commercial products. Moreover, some results have more general impact and can be extrapolated to different converter topologies if their dynamics can be described by the transfer function of similar structure.

Problem analysis described in this work required theoretical background in the area of control theory as well as deep understanding of electrotechnics and electronics. However, the main effort was placed on the practical realization of digital controller, implementation of the signal processing algorithms and their verification on power electronic converter. These steps were essential from the Author's perspective to confirm two theses proposed in sec. 1.1. The fist of the theses concerning the improvement of the quality and reliability of energy supply was proven by implementing $\mathcal{H}_\infty$ compensator in the FPGA-based dedicated controller. The results collected in Tab. 4.6 shows the improvement in quality – in particular in PSRR factor which describes the impact of the input voltage disturbances on the output voltage. The second thesis, concerning the implementation of complex control algorithm has been proven by the fact that the Author has implemented $4th$ order linear discrete compensator with the anti-windup algorithm in real-time FPGA

platform. The algorithm works at very high frequency of 50 kHz (analog-to-digital converters operate at 200 kHz, but decimator and moving average digital filter downsamples the signal to 50 kHz)

The Author considers the part of this work as the original achievement and scientific contribution. The most significant result concerns the realization of complex and advanced control system including hardware and software. The selected control algorithms have been developed on the basis of the model tests, simulations and experiments. The results presented in this thesis allow for a advantageous assessment of the potential of the proposed algorithms.

The Faculty of Electrical Engineering, Automatics, Computer Science and Biomedical Engineering, AGH University of Science and Technology conducts many innovative projects on energy conversion, monitoring and improving power quality. Most of them utilize power electronic inverters, DC/DC converters or another power processing devices. The most frequently chosen compensator used for particular control loops in these applications is analog or digital implementation of PI or PID controllers. Traditional controllers are simple, popular and well proven. The intention of the Author is to analyze in future the possible impact of replacing traditional digital control loops by the controller based on $\mathcal{H}_\infty$ theory. There is also an opportunity to use the $\mathcal{H}_\infty$ compensator in another applications, where linear control system is recommended and the improvement of control system may considerably affect the quality of the product.

Finally, the Author would like to continue his research on digital control systems for power electronic devices and evaluate another control strategies. The Author would like to analyze the applicability of the state observers (with a particular focus on exact state observer [20]). Another approach, which can allow obtaining good results and very fast response is predictive control. This method requires precise plant moder and is computationally expensive, but would be suitable for implementation in FPGA device [52].

Bibliography

[1] C. Albea. *Control Design for Electronic Power Converters*. PhD thesis, Institut National Polytechnique de Grenoble-INPG; Universidad de Sevilla, 2010.

[2] A. Antoniou. *Digital signal processing*. McGraw-Hill Toronto, Canada:, 2006.

[3] N. P. Aryan. *Design and Modeling of Inductors, Capacitors and Coplanar Waveguides at Tens of GHz Frequencies*. Springer, 2014.

[4] K. J. Åström, P. Albertos, M. Blanke, W. Schaufelberger, and A. Isidori. *Control of Complex Systems*. Springer-Verlag, 2001.

[5] K. J. Åström and T. Hägglund. *Advanced PID control*. ISA-The Instrumentation, Systems, and Automation Society; Research Triangle Park, NC 27709, 2006.

[6] K. J. Åström and R. M. Murray. *Feedback systems: an introduction for scientists and engineers*. Princeton University Press, 2010.

[7] K. J. Åström and B. Wittenmark. *Computer-Controlled Systems: Theory and Design*. Courier Corporation, 2011.

[8] J. Baranowski. Projektowanie obserwatora dla silnika szeregowego prądu stałego. *Automatyka/Akademia Górniczo-Hutnicza im. Stanisława Staszica w Krakowie*, 10(1):33–52, 2006.

[9] C. Basso. *Designing Control Loops for Linear and Switching Power Supplies: A Tutorial Guide*. Artech House, 2012.

[10] M. C. Brown. *Practical switching power supply design*. Elsevier, 2012.

[11] J. C. Cockburn and B. G. Morton. Linear fractional representations of uncertain systems. *Automatica*, 33(7):1263–1271, 1997.

[12] L. Corradini, A. Bjeletic, R. Zane, and D. Maksimovic. Fully digital hysteretic modulator for DC–DC switching converters. *Power Electronics, IEEE Transactions on*, 26(10):2969–2979, 2011.

[13] L. Corradini, E. Orietti, P. Mattavelli, and S. Saggini. Digital hysteretic voltage-mode control for DC–DC converters based on asynchronous sampling. *Power Electronics, IEEE Transactions on*, 24(1):201–211, 2009.

[14] P. Cortés, M. P. Kazmierkowski, R. M. Kennel, D. E. Quevedo, and J. Rodríguez. Predictive control in power electronics and drives. *Industrial Electronics, IEEE Transactions on*, 55(12):4312–4324, 2008.

[15] J. C. Doyle, B. A. Francis, and A. R. Tannenbaum. *Feedback control theory*. Courier Corporation, 2013.

[16] T. Dziwiński, W. Bauer, J. Baranowski, P. Piątek, and M. Zagórowska. Robust Non-integer Order Controller for Air Heater. In *Methods and Models in Automation and Robotics (MMAR), 2014 19th International Conference On*, pages 434–438. IEEE, 2014.

[17] T. Dziwiński, W. Bauer, J. Baranowski, P. Piątek, and M. Zagórowska. Robust Non-integer Order Controller for Air Heating Process Trainer. In *Advances in Modelling and Control of Non-integer-Order Systems*, pages 249–256. Springer, 2015.

[18] T. Dziwiński and K. Chmielowiec. High Performance FPGA-based Digital Real-time Controller for Electric Power Conversion Applications. In *IEEE Power and Energy Society General Meeting*. IEEE, 2014.

[19] T. Dziwiński, P. Piątek, W. Słowik, and J. Baranowski. On design of digital control systems for power electronic converters. In *The 39th Conference on Fundamentals of Electrotechnics and Circuit Theory*, pages 45–46. Institute of Electrical Engineering and Computer Science, Silesian University of Technology, 2016.

[20] T. Dziwiński and P. Włodarczyk. The application of the exact state estimation method in electric power systems. *Electrical Review*, 89(7):164–168, 2013.

[21] R. W. Erickson and D. Maksimovic. *Fundamentals of Power Electronics*. Springer, 2001.

[22] M. S. Fadali and A. Visioli. *Digital control engineering: analysis and design*. Academic Press, 2012.

[23] G. Feng, E. Meyer, and Y.-F. Liu. A new digital control algorithm to achieve optimal dynamic performance in DC-to-DC converters. *Power Electronics, IEEE Transactions on*, 22(4):1489–1498, 2007.

[24] Feryster. Dehf - hi-flux high current inductors. `http://www.feryster.pl/polski/pdf/dlawiki/dehf.pdf`. online, accessed in October 2015.

[25] L. Gang and M. Gevers. Optimal finite precision implementation of a state-estimate feedback controller. *Circuits and Systems, IEEE Transactions on*, 37(12):1487–1498, 1990.

[26] Google Inc., IEEE PELS. The Little Box Challenge. `https://www.littleboxchallenge.com`. online, accessed in September 2014.

[27] W. Grega. *Metody i algorytmy sterowania cyfrowego w układach scentralizowanych i rozproszonych*. Uczelniane Wydawnictwa Naukowo-Dydaktyczne AGH, 2004.

[28] D.-W. Gu, P. H. Petkov, and M. M. *Robust control design with MATLAB®*, volume 1. Springer Science & Business Media, 2005.

[29] G. Hardier, C. Roos, and C. Seren. Creating sparse rational approximations for linear fractional representations using surrogate modeling. In *3rd IFAC International Conference on Intelligent Control and Automation Science (2013 IFAC ICONS)*, 2013.

[30] D. G. Holmes and T. A. Lipo. *Pulse Width Modulation for Power Converters: Principles and Practice*, volume 18. John Wiley & Sons, 2003.

[31] T. Hu and Z. Lin. *Control systems with actuator saturation: analysis and design*. Springer Science & Business Media, 2001.

[32] G. C. Ioannidis and S. Manias. H∞ loop-shaping control schemes for the buck converter and their evaluation using μ-analysis. In *Electric Power Applications, IEE Proceedings-*, volume 146, pages 237–246. IET, 1999.

[33] R. Istepanian and J. F. Whidborne. *Digital controller implementation and fragility: A modern perspective*. Springer Science & Business Media, 2012.

[34] V. Kapila and K. Grigoriadis. *Actuator saturation control*. CRC Press, 2002.

[35] C. Kenney and G. Hewer. Necessary and sufficient conditions for balancing unstable systems. *Automatic Control, IEEE Transactions on*, 32(2):157–160, 1987.

[36] W. Koziński. *Projektowanie regulatorów: wybrane metody klasyczne i optymalizacyjne*. Oficyna Wydawnicza Politechniki Warszawskiej, 2004.

[37] Z. Lukić, N. Rahman, and A. Prodic. Multibit sigma–delta pwm digital controller IC for DC–DC converters operating at switching frequencies beyond 10 MHz. *Power Electronics, IEEE Transactions on*, 22(5):1693–1707, 2007.

[38] K. H. Lundberg. Analog-to-digital converter testing. `www.mit.edu/klund/A2Dtest.pdf`, 2002. online, accessed in October 2015.

[39] B. Lurie and P. Enright. *Classical feedback control: with MATLAB*. CRC Press, 2000.

[40] J.-F. Magni. Presentation of the linear fractional representation toolbox (lfrt). In *Computer Aided Control System Design, 2002. Proceedings. 2002 IEEE International Symposium on*, pages 248–253. IEEE, 2002.

[41] D. Maksimović, R. Zane, and R. Erickson. Impact of digital control in power electronics. In *Power Semiconductor Devices and ICs, 2004. Proceedings. ISPSD'04. The 16th International Symposium on*, pages 13–22. IEEE, 2004.

[42] D. Meeks. Loop stability analysis of voltage mode buck regulator with different output capacitor types – continuous and discontinuous modes. *Texas Instrument Application Report, SLVA301*, pages 1–36, 2008.

[43] S. Mehta and J. Chiasson. Nonlinear control of a series DC motor: theory and experiment. *Industrial Electronics, IEEE Transactions on*, 45(1):134–141, 1998.

[44] W. Mitkowski. *Stabilizacja systemów dynamicznych*. Wydawnictwo Naukowo-Techniczne, 1991.

[45] E. Monmasson. *Power Electronic Converters: PWM Strategies and Current Control Techniques*. John Wiley & Sons, 2013.

[46] M. Morari. *Robust Process Control*. Prentice Hall Inc., 1989.

[47] D. Morrison. Robert mammano: Lifetime achievement award recipient. *Power Electronics Technology*, 31(9):48–51, 2005.

[48] M. Norris, L. M. Platon, E. Alarcon, and D. Maksimovic. Quantization noise shaping in digital pwm converters. In *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, pages 127–133. IEEE, 2008.

[49] P. Paraskevopoulos. *Digital control systems*. Prentice Hall Upper Saddle River, 1996.

[50] P. Piątek. Wykorzystanie specjalizowanych architektur sprzętowych do realizacji krytycznych czasowo zadań sterowania – PhD Thesis, 2007.

[51] M. H. Rashid. *Power electronics handbook: devices, circuits and applications*. Academic press, 2010.

[52] V. Spinu, A. Oliveri, M. Lazar, and M. Storace. Fpga implementation of optimal and approximate model predictive control for a buck-boost dc-dc converter. In *Control Applications (CCA), 2012 IEEE International Conference on*, pages 1417–1423. IEEE, 2012.

[53] R. F. Stengel and C. I. Marrison. Reply by the authors to JJ Gribble. *Journal of Guidance, Control, and Dynamics*, 18(6):1468–1470, 1995.

[54] T.-T. Tay, I. Mareels, and J. B. Moore. *High performance control*. Springer Science & Business Media, 2012.

[55] J. C. Teel. Understanding power supply ripple rejection in linear regulators. *Analog Applications Journal*, 2005.

[56] The MathWorks, Inc. State-space or transfer function plant augmentation for use in weighted mixed-sensitivity H-infinity and H2 loopshaping design. `https://www.mathworks.com/help/robust/ref/augw.html`. online, accessed in October 2016.

[57] S. M. Trimberger. Three ages of FPGAs: A retrospective on the first thirty years of FPGA technology. *Proceedings of the IEEE*, 103(3):318–331, 2015.

[58] M. Veerachary. Robust digital voltage-mode controller for synchronous soft-switching boost converter. In *Power Electronics and Drive Systems (PEDS), 2011 IEEE Ninth International Conference on*, pages 1131–1136. IEEE, 2011.

[59] L. Wang, S. Chai, D. Yoo, L. Gan, and K. Ng. *PID and Predictive Control of Electrical Drives and Power Converters Using MATLAB/Simulink*. John Wiley & Sons, 2015.

[60] G. Weiss, Q.-C. Zhong, T. C. Green, and J. Liang. H repetitive control of dc-ac converters in microgrids. *Power Electronics, IEEE Transactions on*, 19(1):219–230, 2004.

[61] J. Whitaker. *The Electronics Handbook*. CRC Press, 2005.

[62] L. Yacoubi, K. Al-Haddad, L.-A. Dessaint, and F. Fnaiech. A DSP-based implementation of a nonlinear model reference adaptive control for a three-phase three-level NPC boost rectifier prototype. *Power Electronics, IEEE Transactions on*, 20(5):1084–1092, 2005.

[63] T. Zhou and J. Xu. Flash ADC with large conversion range for digital controller of high-frequency power converter. In *Communications, Circuits and Systems Proceedings, 2006 International Conference on*, volume 4, pages 2748–2751. IEEE, 2006.

List of Figures

List of Tables

Appendix

Buck converter – practical realization (Laboratory of Digital Control, Department of Automatics and Biomedical Engineering)

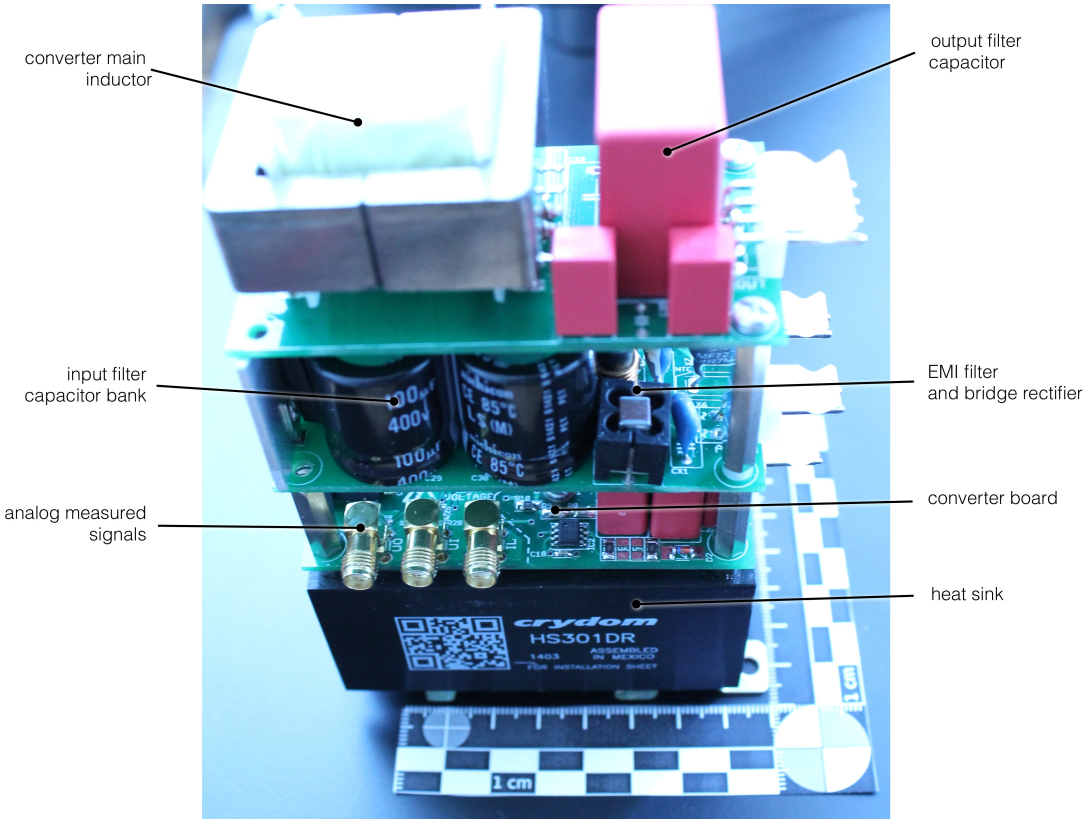


Figure A.1: Wiring diagram of the designed buck converter

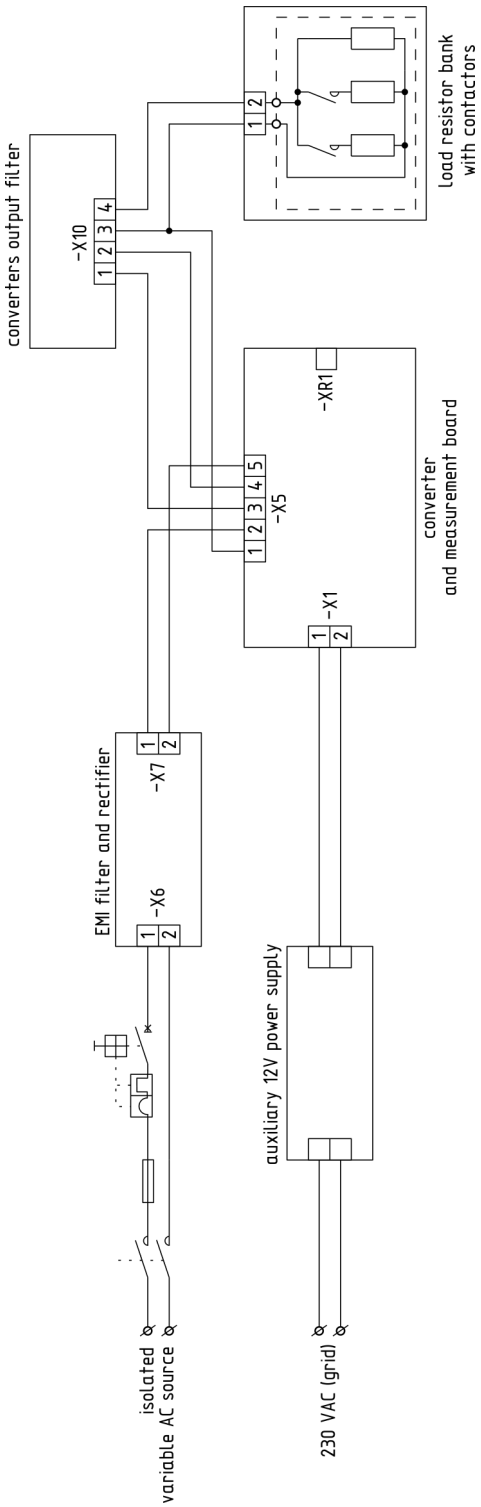


Figure A.2: Buck converter diagram designed for experiments conducted and described in this work (part 1)

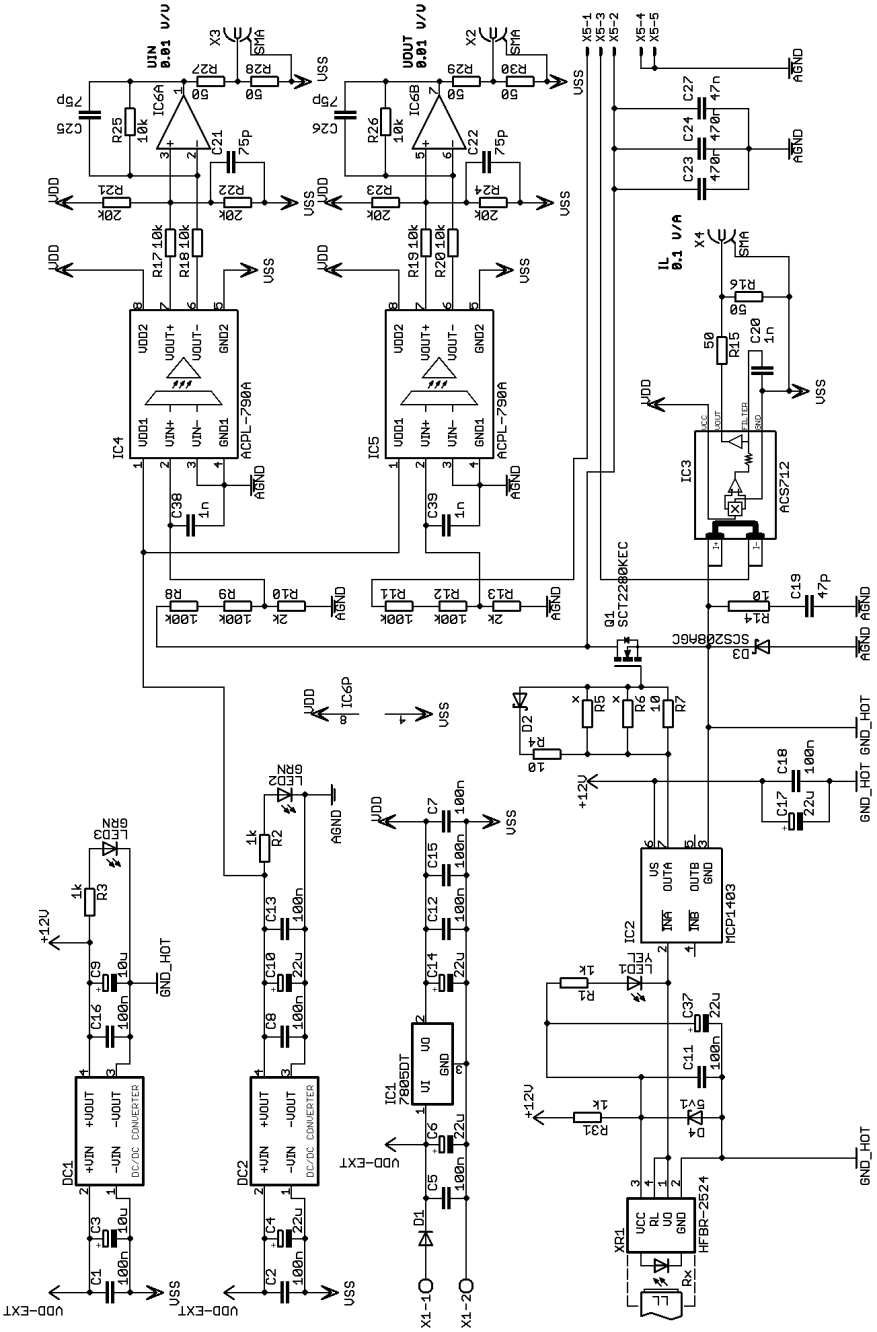


Figure A.3: Buck converter diagram designed for experiments conducted and described in this work (part 1)

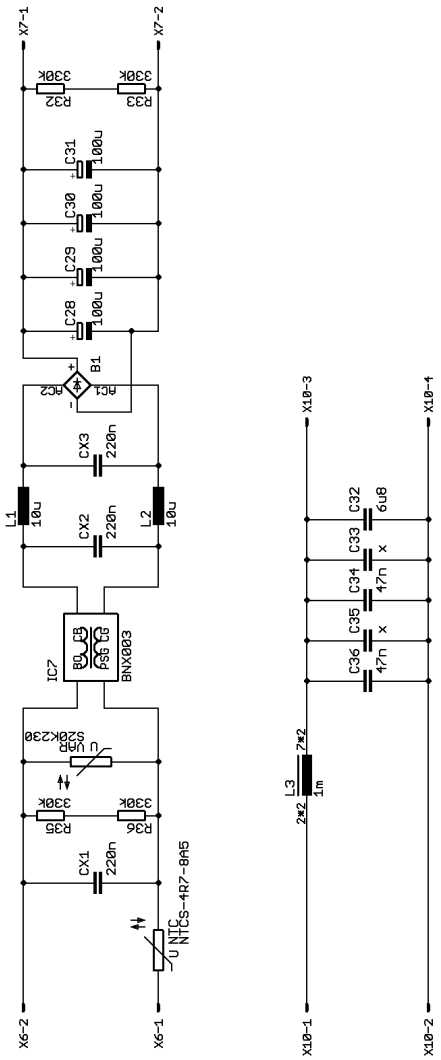


Figure A.4: Buck converter diagram designed for experiments conducted and described in this work (part 2)

Controller interface cards

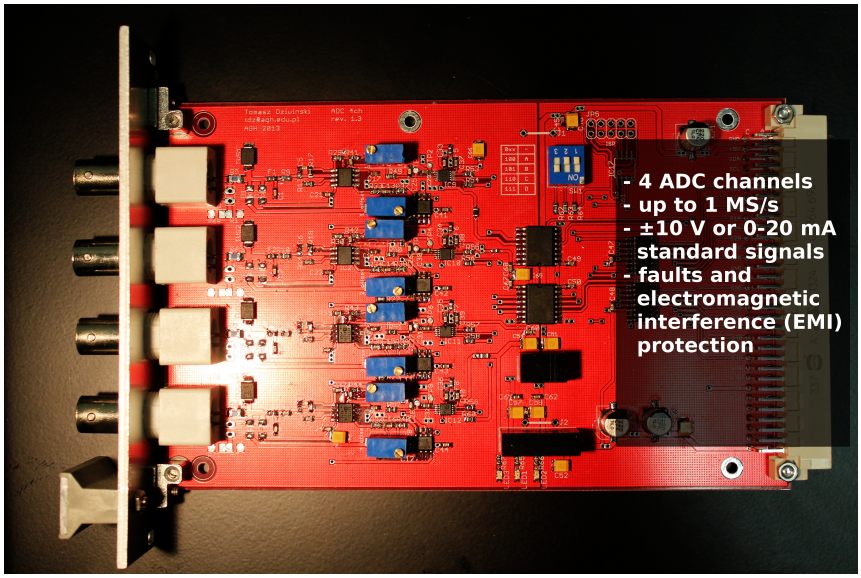


Figure A.5: Analog input interface card

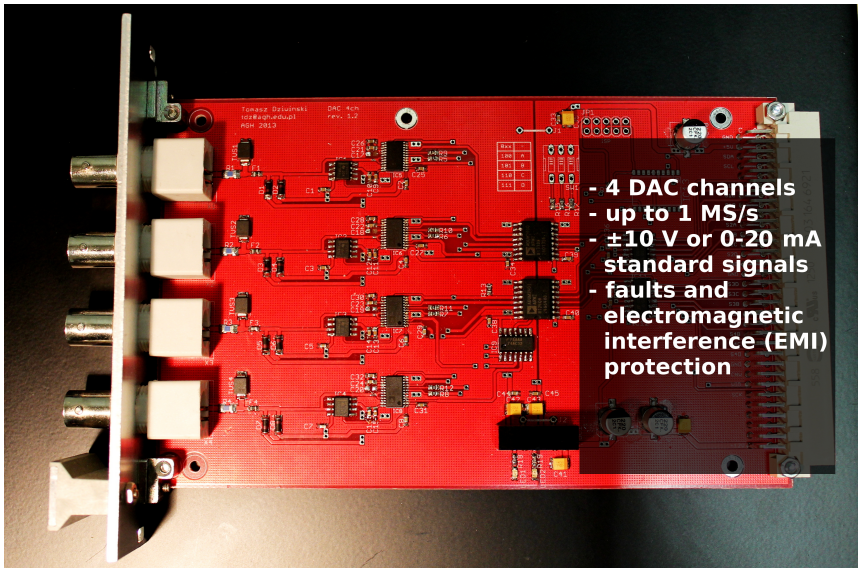


Figure A.6: Analog output interface card

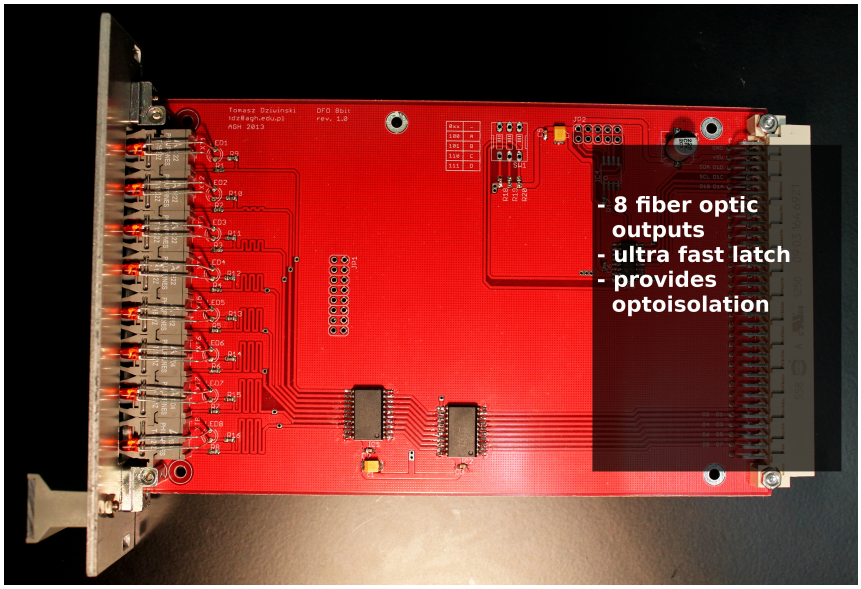


Figure A.7: Digital fiber-optic interface card