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Faculty of Electrical Engineering, Automatics,
Computer Science and Biomedical Engineering

Department of Measurement and Electronics

PH. D. DISSERTATION

Low power A/D converters for multichannel integrated circuits

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Wydział Elektrotechniki, Automatyki, Informatyki
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Katedra Metrologii i Elektroniki

ROZPRAWA DOKTORSKA

Niskomocowe przetworniki A/C dla potrzeb wielokanałowych układów scalonych

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Promotor: dr hab. inż. Robert Szczygieł

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Składam serdeczne podziękowania mojemu promotorowi,

Panu Robertowi Szczygłowi za opiekę naukową, liczne sugestie oraz cenne wskazówki.

Słowa podziękowania kieruję również do Profesora Pawła Grybosia,

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oraz do wszystkich kolegów i współpracowników z Katedry Metrologii i Elektroniki.

Contents

ACRONYMS AND ABBREVIATIONS

ADC – Analog-to-Digital Converter

ASIC – Application Specific Integrated Circuit

CBM – Compressed Baryonic Matter

CCD – Charge Coupled Device

CSA – Charge Sensitive Amplifier

DAC – Digital-to-Analog Converter

DEPFET – Depleted P-channel Field-Effect Transistor

DNL – Differential Non-Linearity

ENOB – Effective Number of Bits

FFT – Fast Fourier Transform

FoM – Figure of Merit

HEP – High Energy Physics

INL – Integral Non-Linearity

LSB – Least Significant Bit

MAPS – Monolithic Active Pixel Sensor

MS/s – Megasamples per second

MSB – Most Significant Bit

QCD – Quantum Chromodynamics

ROIC – Read-Out Integrated Circuit

SAR – Successive Approximation Register

SINAD – Signal to Noise and Distortion

SNR – Signal to Noise Ratio

1. INTRODUCTION

1.1 Outline

Silicon detectors have been adopted in many measurement and detection applications [1]. They have been widely used in High Energy Physics (HEP) experiments involving detection of charged particles and ionizing radiation and are becoming popular in various X-ray imaging applications [2]. In HEP experiments the typical measured parameters are: incident time and location [3] and the charge deposited in the detector volume [4]. This requires processing of each particle hit independently. On the contrary, in X-ray imaging systems the deposited charge can be integrated (either in the detector or in the readout electronics), therefore integrating systems like CCDs can be used. However, replacing integration with single photon counting yields many advantages, e.g.: inherent noise filtering and very wide dynamic range. This work covers the solutions for single photon/particle processing both in HEP experiments and X-ray imaging applications.

The detection systems can be divided into monolithic and hybrid. In monolithic systems (like MAPS or DEPFET) the silicon sensor is produced within the same process with readout electronics. On the contrary, hybrid systems consists of two separate parts – the silicon detector and the readout integrated circuit (ROIC). The examples of these systems are presented in Fig. 1.1. Such construction allows to independently optimize the technological processes for the sensor and the ASIC, yielding better final parameters (though higher price). This thesis focuses on the hybrid detection/measurement systems.

While the detector manufacturing process is known and perfected for years, it is the design of readout electronics what poses a challenge. Because of large number of channels, stochastic nature of the input signals and the processing requirements, the parallel signal processing is necessary and multichannel readout systems have to be employed.

The physical architecture of the readout system is determined by the detector's type and dimensions. Readout channel's pitch in majority of systems has to match the one of the detector, which is typically in the range of 50 μm to 200 μm. This condition imposes strict area limitations on a single readout channel. The maximum allowable chip power divided by the total number of channels limits the single channel power consumption. These power limitations are typically of about few miliwats per channel for strip and few tens of microwatts for pixel circuits. Also, very high parameter uniformity across all readout channels in such systems is required.

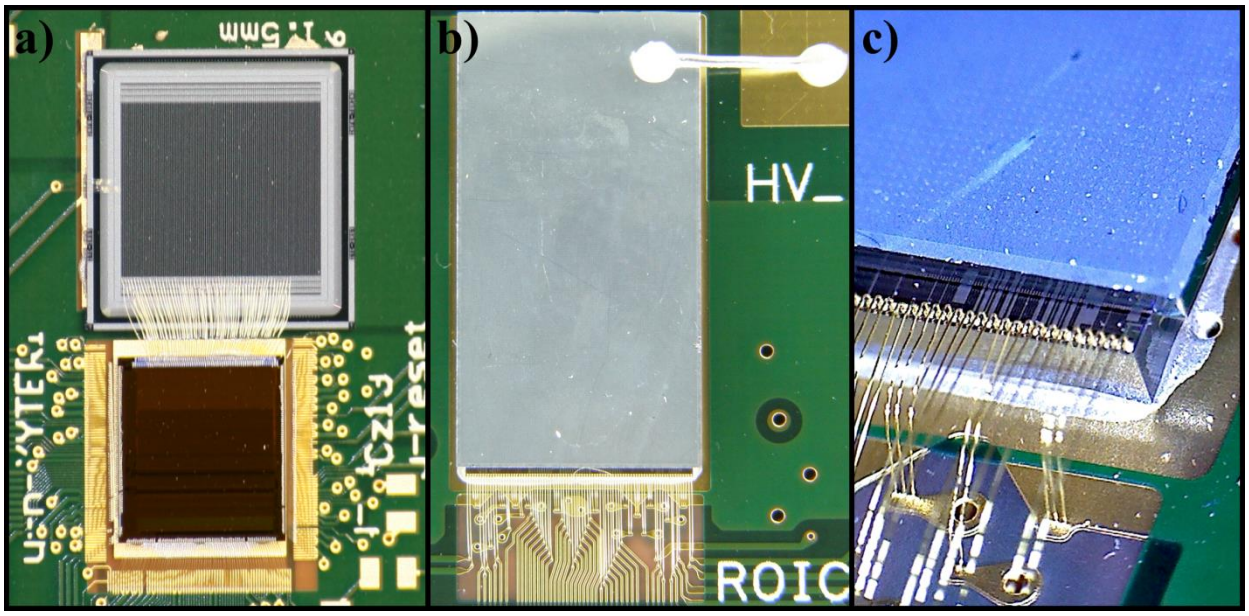

Fig. 1.1 Example of hybrid multichannel detection systems: a) silicon strip sensor (top) wire-bonded to the readout ASIC (courtesy of Krzysztof Kasiński) [5], b) pixel sensor flip-chip bonded to the readout ASIC [6][7], c) close-up on the ROIC-sensor connection.

A typical readout channel architecture in a single-pulse processing circuit is shown in Fig. 1.2. A current signal generated in the active volume of silicon strip/pixel detector is integrated in a Charge Sensitive Amplifier. At the output of the preamplifier a voltage step is obtained which amplitude is proportional to the total charge generated in the detector. The voltage step is fed to the main amplifier, called a shaper, which provides the pulse shaping according to the timing requirements and the filtration of noise to maximize the signal to noise ratio. Further signal processing at the shaper outputs in multichannel chips can be done in different ways. One of the most popular is a binary readout, by means of a discriminator, and counting the pulses above a specified threshold. A significant step forward is to allow pulse amplitude measurement and digitalization in each channel independently by means of an analog-to-digital converter (ADC).

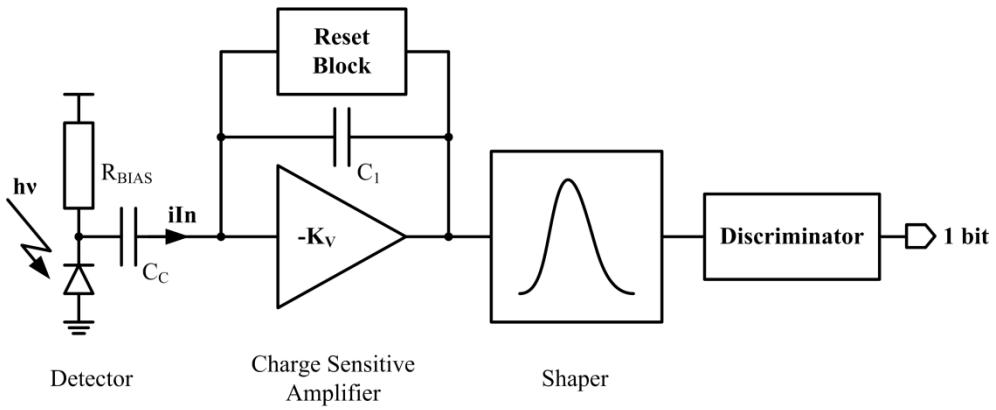

Fig. 1.2 Signal processing channel in a typical silicon detector ROIC.

Further miniaturization and functionality improvement of multichannel readout systems pose new design challenges. It is a current topic in the field, which is undertaken by many research institutes specialized in the multichannel silicon detector readout circuits design, e.g. CERN in Switzerland [8][9], Fermilab in USA [10][11] or GSI in Germany [12].

Thanks to the progress in the integrated circuits manufacturing process, decreasing feature size and power consumption, it is possible to greatly increase functionality of integrated circuits. However, modern deep submicron technologies, along with new prospects, also bring issues that need to be addressed in systems allowing analog-to-digital conversion. These are decreased transistor's intrinsic gain, limited signal processing voltage swing, leakage currents, etc. [13] Additionally, multichannel circuits' specific requirements, such as very low power consumption and silicon area occupancy, lead to various design compromises. One of them is the necessity of using transistors with dimensions close to the technology limits, which results in significant mismatch effects and random parameter variation.

These limitations impose development of new ADC architectures suitable for application in multichannel readout integrated circuits. This is the topic of the dissertation. It aims at design of low to moderate resolution analog-to-digital converters, in the range of 4-8 bits, with sample rates up to few megasamples per second and capable of independent in-channel pulse amplitude measurement. Additional goal is the development of new calibration techniques, suitable for application in multichannel readout integrated circuits.

1.2 ADC architecture from the multichannel systems perspective

The analog-to-digital conversion process can be accomplished by various converter architectures. The most important factors differentiating them are the resolution, sample rate and power consumption. These three parameters are commonly combined into a single figure of merit, called Walden FoM, given by the expression:

$$FoM_W = \frac{P}{f_S \cdot 2^{ENOB}}\ [J/conv.step], \qquad (1.1)$$

where P is the power consumption, f_S is the sampling rate and ENOB is the effective number of bits [14]. This figure assumes that energy required for conversion doubles with every additional bit of the ADC resolution. However, this approach is not representative for high-resolution designs, which are usually limited by the thermal noise. Therefore, a different figure of merit, the Schreier FoM, is also used. It assumes that energy quadruples for every additional bit of ADC resolution and is given by the equation:

$$FoM_S = SINAD + 10log\left(\frac{BW}{P}\right)\ [dB], \qquad (1.2)$$

where SINAD is the signal to noise and distortion ratio and BW is the signal bandwidth [14].

Fig. 1.3 presents a chart summarizing ADC's energy efficiency, expressed as energy per sample, with respect to its resolution, expressed as Effective Number of Bits. It is based on the designs published at International Solid-State Circuits Conferences and Symposia on VLSI Circuits in the years 2005 – 2015 [15]. This set can be considered as the representative of state-of-art in the field of ADC design. The lines mark the Walden FoM of 5 fJ/conv.step and Schreier FoM of 170 dB.

The chart clearly shows, that ADCs of different architectures and for a wide resolution range comply to the figure of merits presented above. Also, from the multichannel measurement systems perspective, the chart points out the optimal ADC architectures for the considered resolution range. The maximum attainable ADC sample rate is not directly shown, but because of the multichannel system's properties, such as parallel signal processing and low signal bandwidth, this requirement can be fulfilled with relatively low effort and is not critical. However, what is not shown at all is the converter's area occupancy.

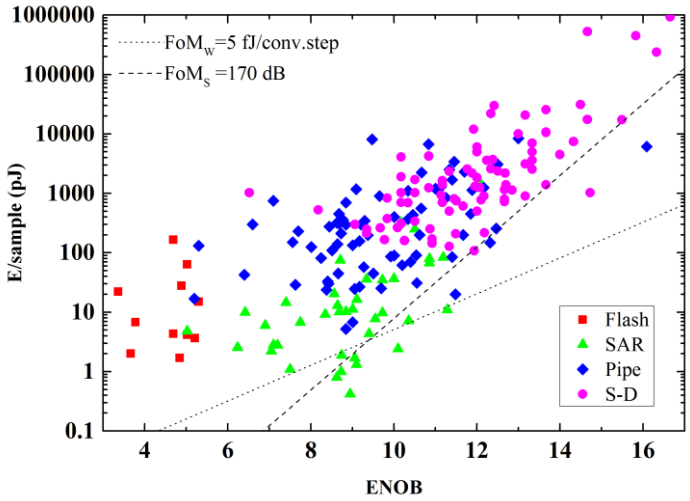

Fig. 1.3 ADC designs overview: energy per sample with respect to resolution.

This parameter is included in Fig. 1.4. The division between the different architectures is not as clear as in the previous figure. The marked area-resolution region of interest, which matches the requirements of multichannel systems, borders most closely with the regions occupied by flash and SAR architectures. Also, it is targeted by very small number of designs [16][17]. Most of the presented converters lay outside of it, as the main emphasis is usually put on ADC's resolution or sampling rate, neglecting its area occupancy. Therefore, a new approach and different priorities are required in design of a converter matching the presented requirements.

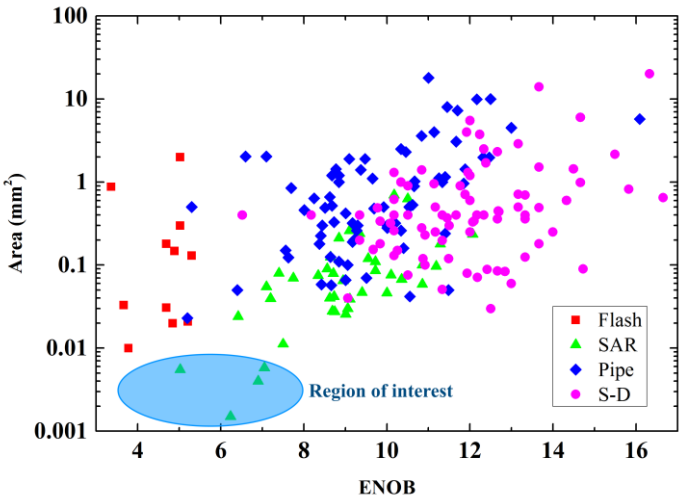

Fig. 1.4 ADC designs overview: chip area with respect to resolution.

To assess the area efficiency of the converters, a resolution-per-area parameter, defined as an effective number of comparison levels divided by chip area, was computed for all the designs. It assumes an exponential relationship between the area and resolution. The results with respect to the manufacturing process are presented in Fig. 1.5.

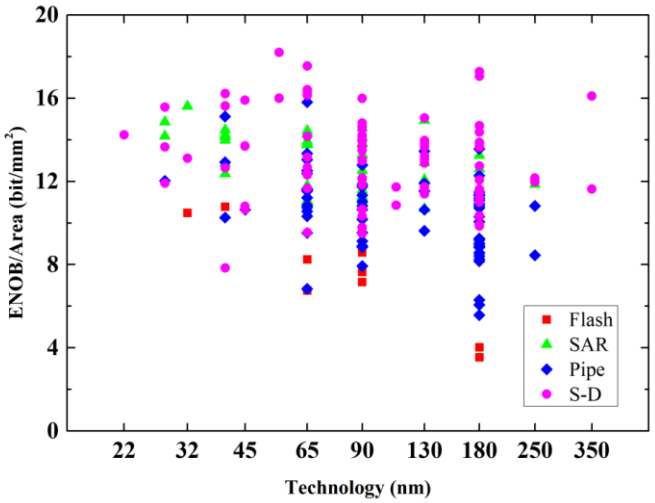

Fig. 1.5 ADC designs overview: resolution-per-area efficiency with respect to manufacturing process.

The plot shows an improvement of the area efficiency with technology, however the dependence is relatively weak and span over a large range for different designs. Good efficiency can be achieved even in older manufacturing processes and strongly depends on the chosen converter's architecture.

1.3 Thesis organization

The thesis is organized as follows: Section 2 describes the flash ADC array used in a pulse amplitude measurement system for a 128-channel ROIC, which will be a part of the detection system in the forthcoming Compressed Baryonic Matter experiment. The experiment goals and overall system architecture are briefly discussed, while the main focus is put on the design of flash ADC with a novel comparator offset voltage correction method, including the measurement results of the prototype chip.

Section 3 contains the design and measurement results of a low-power successive approximation ADC of moderate resolution with very low-area occupancy, suitable for detection systems of pixel architecture. The charge redistribution architecture is explained, sources of ADC's non-linearities are analyzed and finally a design optimization process towards the lowest area occupancy is presented.

Section 4 includes the design of ultra-low area flash ADC with dynamic offset compensation, dedicated to fast X-ray pixel imaging systems with pixel size of 100 μm × 100 μm and smaller. The measurement results of the designs implemented in two different CMOS manufacturing processes – widespread and inexpensive UMC 180 nm and modern TSMC 40 nm – are presented and compared.

Section 5 summarizes the presented ADC designs, highlights new circuit solutions and notable achievements towards application in future multichannel measurement systems.

1.4 Author's contribution

This thesis focuses on the design of low-power ADCs, with emphasis on their implementation in multichannel measurement systems in deep submicron technologies, where the minimum area occupancy is the top priority. The main author's contributions described in the thesis are:

1. Design of a 5-bit multichannel pulse amplitude measurement system, based on a flash ADC array with novel comparator offset voltage correction circuit. The proposed trimming DAC architecture allows to reduce the area of single trim DAC while maintaining its linearity. The design was implemented in a 128-channel strip detector readout system, dedicated for the forthcoming CBM experiment, and implemented in 180 nm CMOS technology.
2. Design of a 7-bit charge redistribution A/D converter, implemented in 180 nm CMOS technology, highly optimized for minimum silicon area occupancy. The circuit has dimensions of only 90 μm × 95 μm, what makes it suitable for measurement systems of pixel architecture.
3. Design of two ultra-low area 4-bit flash A/D converters with dynamic offset storage, implemented in 180 nm and 40 nm CMOS technology, dedicated for future high-count rate pixel X-ray imaging applications.

All four presented ADCs were designed (at both schematic and layout level), sent for fabrication and experimentally characterized by the author himself.

2. FLASH ADC ARRAY FOR PULSE AMPLITUDE MEASUREMENT SYSTEM IN A 128-CHANNEL CBM STS DETECTOR ROIC

2.1 Introduction

2.1.1 The Compressed Baryonic Matter experiment

The goal of the CBM research program at the Facility for Antiproton and Ion Research (FAIR) in Darmstadt, Germany, is to explore the QCD phase diagram in the region of high baryon densities using high-energy nucleus-nucleus collisions. This includes the study of the equation-of-state of nuclear matter at high densities, and the search for the deconfinement and chiral phase transitions [18].

The CBM detector is designed to measure both bulk observables with large acceptance and rare diagnostic probes, such as charmed particles and vector mesons decaying into lepton pairs [19]. The layout of CBM experimental setup is presented in Fig. 2.1.

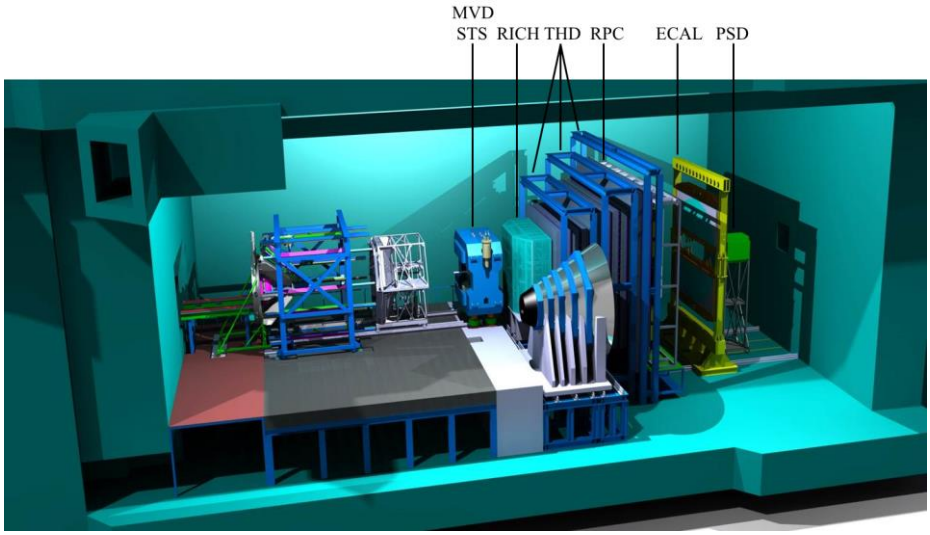

Fig. 2.1 CBM experiment detector setup [18].

The system will consist of the following components:

- The Micro-Vertex Detector (MVD): it is dedicated to identification of D mesons. It will be built of 2 or 3 layers of Monolithic Active Pixel Sensors, with a pixel size between 25 μm × 25 μm and 40 μm × 40 μm, located between 5 cm to 20 cm downstream of the target.
- The Silicon Tracking System (STS): its task is to provide track reconstruction and momentum determination of charged particles. It will be built of up to 8 layers of silicon strip detectors, located at distances from 30 cm to 100 cm downstream of the target. Its concept is based on double-sided microstrip detectors with a strip pitch of 58 μm. The sensors will be read out through multi-line micro-cables with electronics located at the periphery of the station.

- The Ring Imaging Cherenkov Detector (RICH): it is designed to provide identification of electrons and suppression of pions in the momentum range below 8 GeV/c. It comprises of a 2.9 m long gas vessel filled with nitrogen, a glass mirror and two photodetector planes.
- The Transition Radiation Detector (TRD): Three TRD stations, each consisting of 3-4 detector layers, will serve for particle tracking and for the identification of electrons and positrons with p > 1.5 GeV/c. The detector stations are located at approximately 5 m, 7.2 m and 9.5 m downstream of the target, with the total active detector area of 1100 m^2.
- The timing Resistive Plate Chambers (RPC): it will be used for hadron identification via time-of-flight (TOF) measurements. The TOF wall is located 10 m downstream of the target and covers an active area of about 120 m^2.
- The Electromagnetic Calorimeter (ECAL): a "shashlik" type calorimeter will be used to measure direct photons and neutral mesons decaying into photons. It will be composed of modules which consist of 140 layers of 1 mm lead and 1 mm scintillator.
- The Projectile Spectator Detector (PSD): it will be used to determine the collision centrality and the orientation of the reaction plane.

This section concerns a part of the STS silicon strip detectors' readout electronics, the STS-XYTER chip, a multichannel application specific integrated circuit.

2.1.2 System requirements

To allow track reconstruction and momentum determination of charged particles, each channel of the readout electronics has to independently determine the timestamps of interactions and the charge deposited in the detector by passing particles. The required timing resolution for the timestamp is 2 ns, while the required charge measurement resolution is 0.5 fC, within the range of 0.5 fC to 16 fC.

The number of measurement channels per ASIC is set to 128. They are arranged in a strip layout with a pitch of 58 μm. The small pitch limits the available silicon area, while large number of ASICs in the final system (approximately sixteen thousands chips) and cooling conditions limit single channel power consumption to 5 mW per channel [20].

Additionally, as the readout electronics will be placed at the perimeter of the detector station and it will be exposed to radiation, the design has to be radiation hardened. Therefore, certain design considerations were taken, such as:

- Enclosed Layout Transistors (ELT) design and separate protection rings for NMOS transistors, which limits the available W/L ratio and requires additional silicon area,
- radiation hardened SRAM memory with improved Single Event Upset (SEU) immunity,
- triple-redundant control logic.

2.2 Architecture of STS-XYTER ASIC and pulse amplitude measurement subsystem

The STS-XYTER chip block diagram is presented in Fig. 2.2 [21]. The signal processing in each channel is split into two separate paths – fast and slow. The fast path is dedicated for precise time-of-interaction measurement. It consists of a fast shaping amplifier (40 ns shaping time), fast comparator and a time-stamp latch. The slow path is designed for precise measurement of deposited charge value, containing a slow shaping amplifier (90 ns shaping time), a 5-bit flash ADC and a Digital Peak Detector (DPD). The input Charge-Sensitive Amplifier (CSA) is common for both paths. Data coming from all channels are serialized and sent further through the CBMnet interface [22].

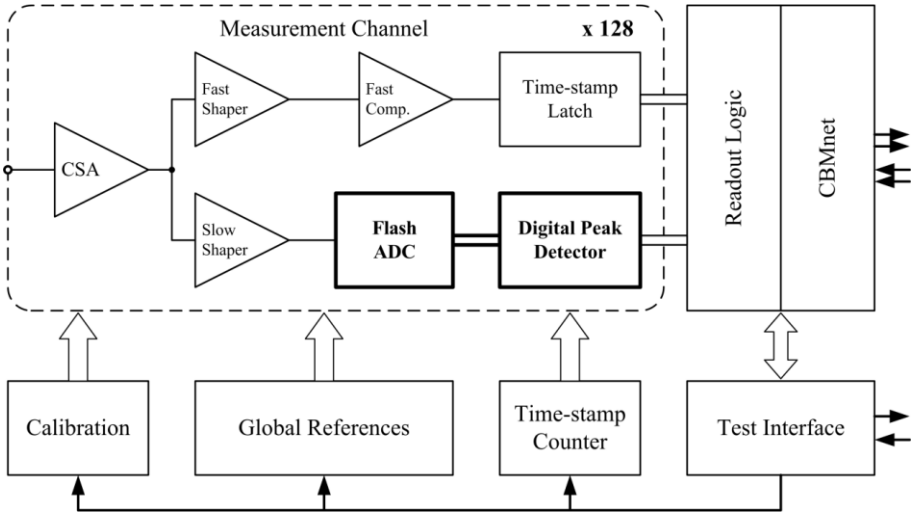

Fig. 2.2 STS-XYTER chip block diagram with author's contribution bolded.

The analog front-end operates asynchronously. The input charge from the detector is collected by the CSA and converted into a voltage step. After shaping, a pseudo-gaussian pulse with amplitude proportional to the input charge is obtained at the flash ADC's input. The idealized pulse example is depicted in Fig. 2.3.

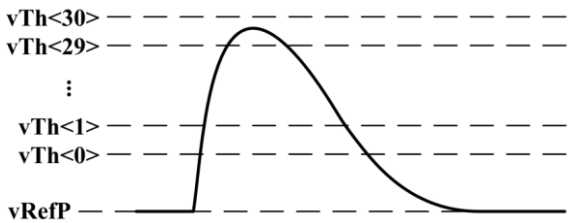

Fig. 2.3 Exemplary idealized ADC's input pulse.

The main task of the author in the STS_XYTER project was to design the pulse amplitude measurement system. A novel pulse amplitude measurement method, basing on a continuous-time flash ADC, is proposed. The pulse is detected and its peak value is measured in the digital domain.

There is no sample-and-hold or peak detector circuit – the voltage is continuously measured by the flash ADC. After the peak is detected, comparator's outputs are latched by the DPD's latches to determine its amplitude. When the signal returns to the base level, the thermometer code value is converted into binary code and the Digital Peak Detector is reset.

Because of large number of comparators present in the ADC block (128×31= 3968) and limited amount of available silicon area, both the size and current consumption of a single comparator has to be minimized. These factors increase impact of the mismatch effects, causing significant comparator's input offset voltage variations and can result in missing codes or large nonlinearities in the ADC transfer characteristic. For proper ADC operation an offset correction technique is necessary.

The trimming solution, basing on adding a trim DAC to each comparator, is implemented [23]. Compared to the other commonly used approaches – e.g. the dynamic offset compensation [24] – it offers the possibility of asynchronous operation, good repeatability and freedom in adjusting the individual offset values. These technique also allows to correct nonlinearities of the preceding stages, such as slow shaper, and allows arbitrary shaping of the ADC transfer characteristics.

The detailed block diagram of the pulse amplitude measurement subsystem is depicted in Fig. 2.4. It contains two global reference circuits, whose outputs are common to all channels: a coarse correction reference and a threshold voltage reference. The measurement channel consists of 31 identical comparator cells and a digital peak detector. Each cell consists of a comparator with a correction buffer and an 8-bit trim DAC with a memory block. Additionally, output of each comparator is connected to a counter, which is used to simplify the offset correction procedure.

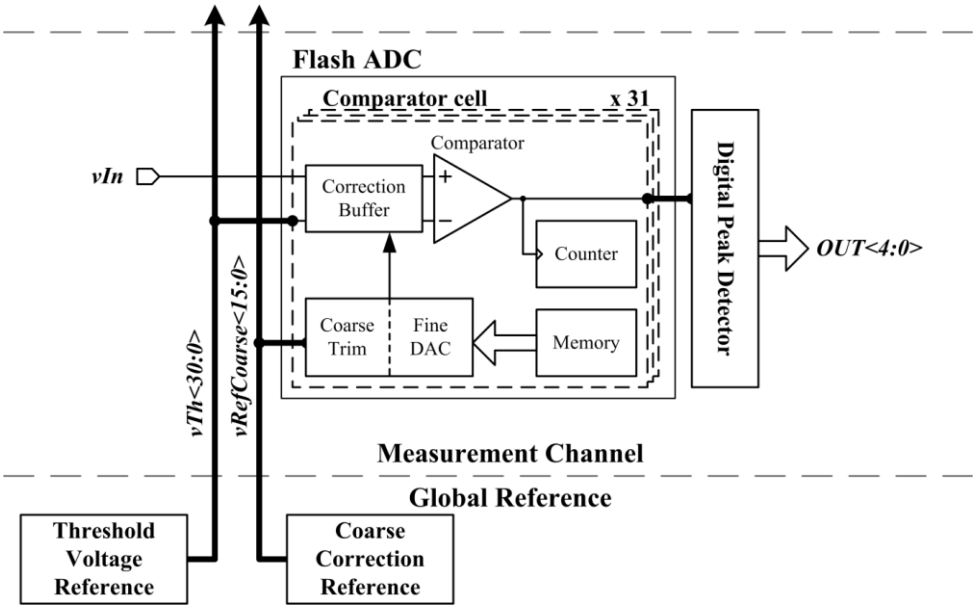

Fig. 2.4 Pulse amplitude measurement subsystem block diagram.

2.3 Design

The pulse amplitude measurement subsystem in each of 128 channels is built of the following blocks:

- Trim DACs – generate the trimming voltage for given bit setting,
- Correction buffers – combine the trimming voltage with the input signal,
- Comparators – compare the trimmed signal with the corresponding threshold voltage,
- Digital peak detector – detects and latches the peak signal value.

2.3.1 Trim DAC

In a trim DAC design, the linearity and monotonicity are not critical parameters, as the area occupancy together with span and coverage of output voltage values are the most important factors [25]. Therefore, the most common approach is to use high-resolution DACs, built of very small devices, whose transfer characteristics are non-monotonic and have large nonlinearities [26]. However, it is beneficial when the trim DAC characteristic is monotonic [27], because the binary search algorithm can be used and the correction procedure can be simplified. As the result, the chip calibration process can be performed much faster.

In order to design a trim DAC with improved monotonicity and reduced area occupancy, a novel approach is proposed. The correction circuit is divided into two stages – coarse and fine. As the most significant bits occupy the majority of the area, only the least significant bits are generated in each trim DAC independently, by a conventional current-steering DAC (fine DAC), while the most significant ones are derived from a single, global reference circuit – the Coarse Correction Reference. The Coarse Correction Reference generates multiple voltage references, which are distributed to all trim DACs. Then, in each trim DAC, one reference voltage is selected, converted into a current and combined with the fine DAC's output to obtain the final correction voltage. The schematic of such 8-bit trim DAC, with 4-bit coarse and 4-bit fine correction is presented in Fig. 2.5.

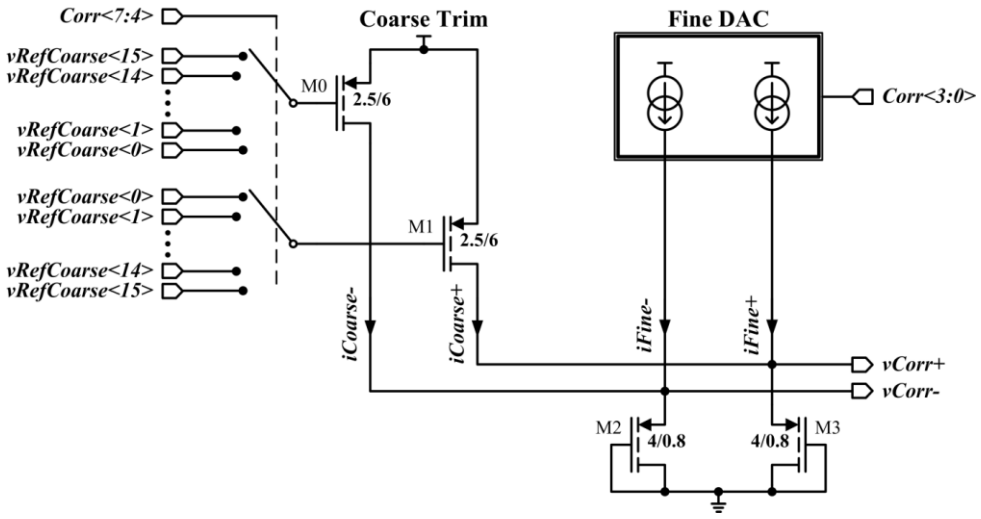

Fig. 2.5 Trim DAC schematic.

The trim DAC has a differential design. The coarse correction is realized by transistors M0-M1 and two analog multiplexers. Bias voltages of the transistors M0 and M1 gates are chosen in a complementary manner amongst the sixteen vRefCoarse voltage references, generating the coarse correction currents iCoarse. The fine correction currents iFine are generated by the 4–bit current-steering fine DAC. Its range is equal to the coarse current increment. Coarse and fine currents are finally combined on two PMOS diode-connected transistors M2 and M3. The voltage difference between the sources of these transistors is the final correction output voltage. Total current consumption of a single trim DAC is constant and equal to 3.2 μA.

The correction range has to be sufficiently large to cover not only the variations of correction buffer's output and comparator's input offset voltage, but also compensate possible nonlinearities of the slow shaping amplifiers.

The fine DAC is built of an array of four PMOS current sources M0-M3 with binary scaled currents (Fig. 2.6). Current source's outputs can be directed to one of the differential outputs iFine. The vBiasFine voltage is generated in each channel separately, derived from the submultiple of the current generated from the vRefCoarse voltage reference. Current of a single PMOS current source is equal to 12.2 nA, resulting in a total current consumption of 183 nA. The transistors are chosen sufficiently large to ensure the monotonicity of the fine DAC.

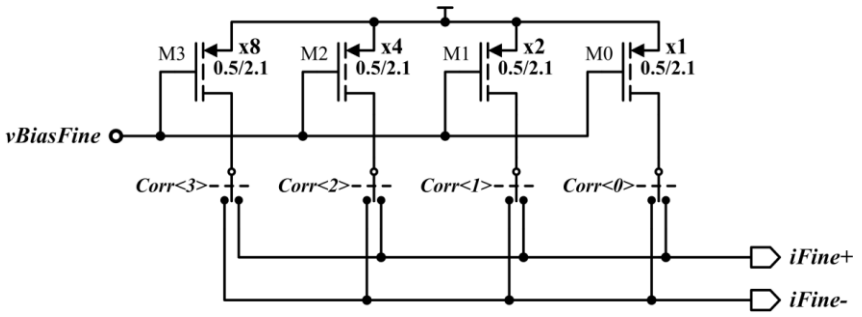

Fig. 2.6 Fine DAC schematic.

The coarse correction reference is built of an array of sixteen NMOS current sources M1-M16 with linearly scaled currents (Fig. 2.7). The current source's outputs are connected to the PMOS diode-connected transistors M17-M32, generating sixteen reference voltages vRefCoarse<0:15>. Both NMOS and PMOS transistors are dimensioned to provide good matching, adequate for the final resolution of 8 bits. The vBiasCoarse voltage is generated on-chip, using the built-in band-gap reference source. Current of the smallest NMOS current source is equal to 7.7 μA, resulting in a total current consumption of 1.1 mA, including current of the bias transistor M0.

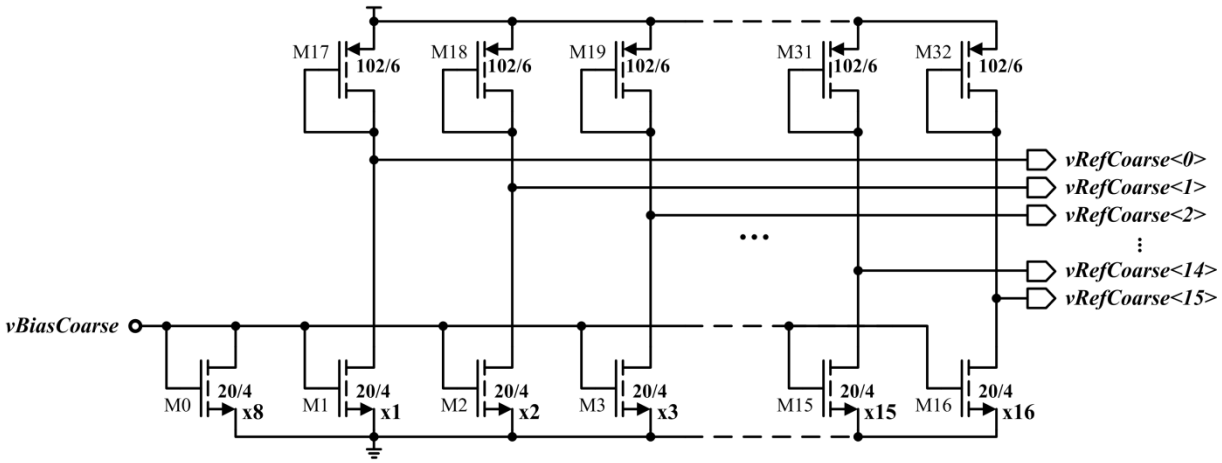

Fig. 2.7 Coarse correction reference schematic.

In the presented trim DAC design, the most significant bits are defined by a single transistor with well-defined bias voltages, thus the coarse current characteristic is inherently monotonic. The fine DAC, as it has relatively low resolution, can be dimensioned to provide monotonic output current without sacrificing much silicon area.

The only possible source of non-monotonicity is when the range of the fine DAC differ from the coarse current increment. Magnitude of these non-linearities depends on the matching of transistors in the Coarse Correction Reference and the coarse current transistors M0-M1 in the particular trim DAC. However, these possible non-monotonicities occur only for known input codes – at the fine DAC's range boundaries.

The ideal characteristic of the trim DAC differential output voltage (vCorr+ – vCorr-) is presented in Fig. 2.8. The non-linearity is the effect of current-voltage characteristic of the PMOS diodes M2-M3 (see Fig. 2.5).

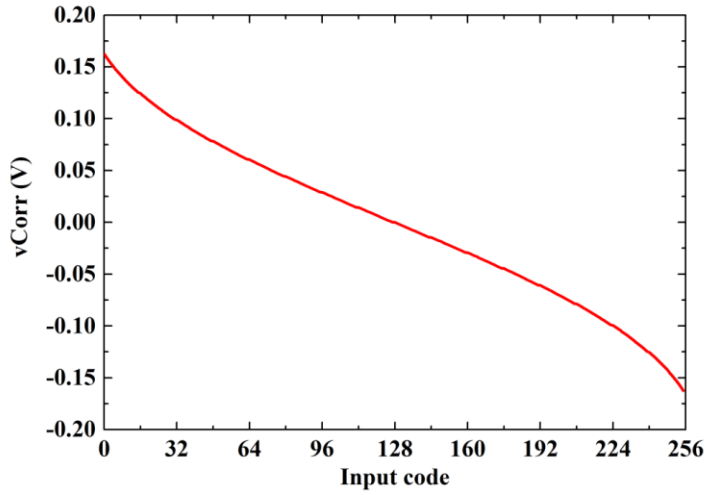

Fig. 2.8 Simulated trim DAC characteristic.

2.3.2 Correction buffer

The offset voltage correction buffer combines the input voltage signal with the output voltage of the correction trim DAC vCorr. It is built as a differential pair with source followers acting as load (Fig. 2.9). The input signal is fed to the differential pair (M1-M2), while the correction voltage is applied to the source follower's gates (M3-M4). All transistors are placed in separate N-wells. The bias current of transistor M0 is equal to 3 µA.

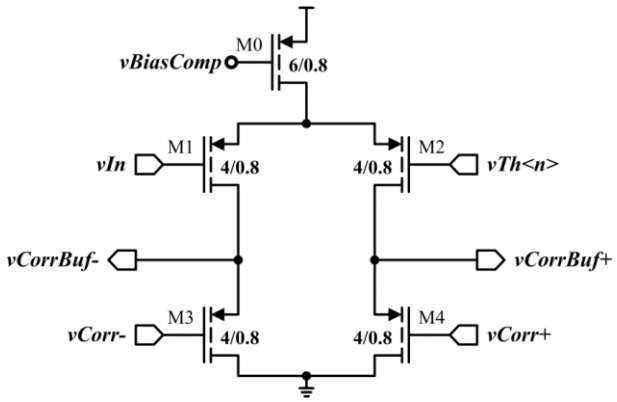

Fig. 2.9 Comparator's offset voltage correction buffer schematic.

The differential correction voltage vCorr sets the differential output signal baseline, independently of the input voltage signal. Therefore, it can be adjusted to correct the input offset voltage of the following stage and the output offset voltage of the correction buffer itself. The simulated correspondence between the differential correction voltage vCorr and output voltage vCorrBuf is depicted in Fig. 2.10.

The correction buffer's Monte-Carlo simulations indicate the output offset voltage standard deviation equal to 5 mV.

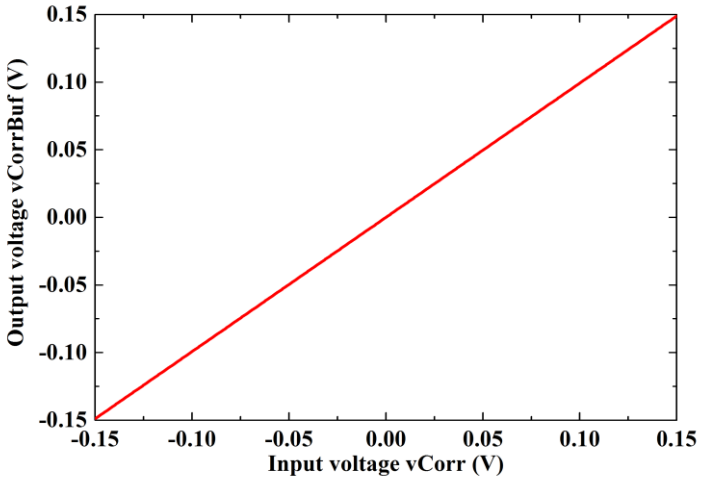

Fig. 2.10 Correction buffer output voltage vs input correction voltage.

2.3.3 Comparator

The comparator is built of two stages: a transconductance amplifier and a current comparator [28] (Fig. 2.11). The transconductance amplifier is the primary amplification component. It converts the differential input voltage vCorrBuf to a current, which is sourced or sunk – depending on the input voltage polarity – at the output. The bias current of transistor M0 is equal to 3 µA.

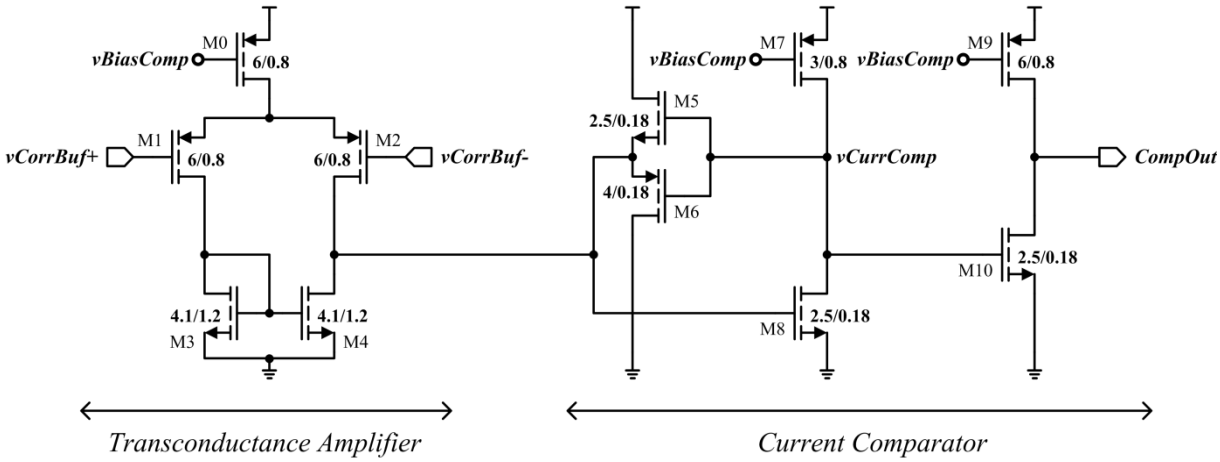

Fig. 2.11 Comparator's schematic.

The second stage is the current comparator. It is built as a common source amplifier (M7-M8) with a push-pull follower (M5-M6) in the feedback loop. The input current – depending on its polarity – is either sunk by the PMOS transistor M6 or sourced by the NMOS transistor M5. Voltage vCurrComp is set at low or high level respectively. Finally, a common source amplifier M9-M10 amplifies the signal to the power line levels. The total bias current of this stage is equal to 4.5 µA.

The comparator's Monte-Carlo simulations indicate the input offset voltage standard deviation is equal to 10 mV.

2.3.4 Digital peak detector

The digital peak detector latches the outputs of the comparators and converts the result into a binary value. The conversion is done in two steps: first the thermometer latched value is converted into 1 of 31 code, then to a binary one. The digital peak detector has to be reset after each conversion.

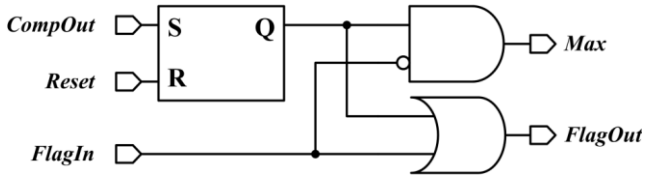

Fig. 2.12 Encoder cell simplified schematic.

Conversion of the thermometer code is done by an encoder cell, present at each comparator (Fig. 2.12). It latches the high level at the input *CompOut* and sets the output *Max* for only one comparator, at the highest threshold voltage.

The encoder cells are connected in a cascade manner, in order from the highest threshold comparator to the lowest, as presented in Fig. 2.13. The *Max* outputs of all cells are connected to the binary encoder, which converts the 1 of 31 code to the final binary value.

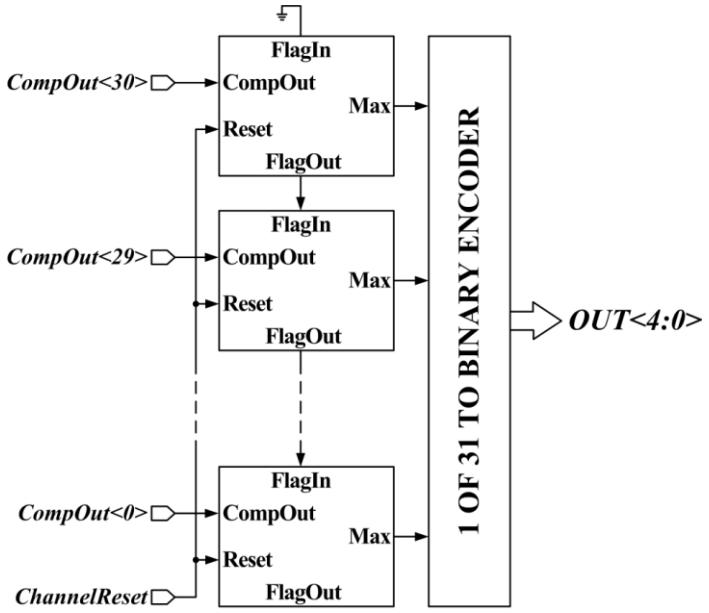

Fig. 2.13 Digital peak detector block diagram.

2.3.5 Threshold voltage reference

The threshold voltage reference generates the thresholds directly connected to comparators in all channels. The threshold voltages have to be linearly and evenly spaced between the two reference voltages vRefP and vRefN. Also, as the threshold voltages are common to all channels, the resistance of the reference voltage source has to be sufficiently low to prevent inter-channel crosstalk.

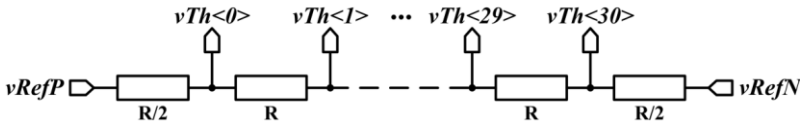

Fig. 2.14 Threshold voltage reference schematic.

A single resistor ladder has been used as a threshold voltage reference, as presented in Fig. 2.14. The salicide, P-diffusion resistors, with a sheet resistance of 8 Ω/□ and dimensions of 8 μm × 63 μm were used. The final resistance of a single resistor is equal to 63 Ω. The reference voltages vRefP and vRefN are generated by on-chip DACs.

2.3.6 Layout

Layout of a single comparator cell, up to metal 2 layer, with functional blocks highlighted, is presented in Fig. 2.15. The trim DAC occupies the area of 37 µm × 17 µm, where 36% is used by the analog multiplexers, 30% by the fine DAC and 34% by the remaining trim DAC components. The comparator with the correction buffer occupies 21 µm × 19 µm.

The most area-consuming block is the 12-bit counter, added to every comparator to simplify the correction process. The 8-bit memory block is built of dice cells [29] for improved radiation immunity, therefore it requires more area than standard SRAM. The digital peak detector logic is distributed uniformly among the comparator cells.

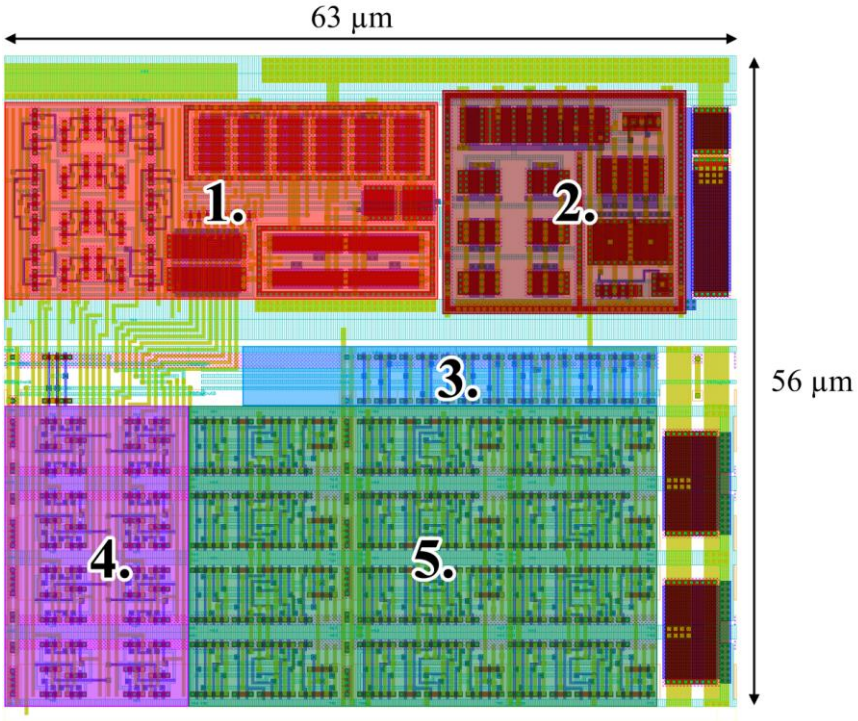

Fig. 2.15 Comparator cell layout with marked functional blocks: 1. Correction trim DAC, 2. Comparator with correction buffer, 3. Digital peak detector logic, 4. Correction memory, 5. Counter.

The coarse correction and the threshold voltage references are located in the periphery area of the chip and occupy 650 µm × 120 µm and 1950 µm × 220 µm respectively.

The layout of the STS-XYTER integrated circuit is presented in Fig. 2.16. The chip measures 6.5 mm × 10 mm.

a)

b)

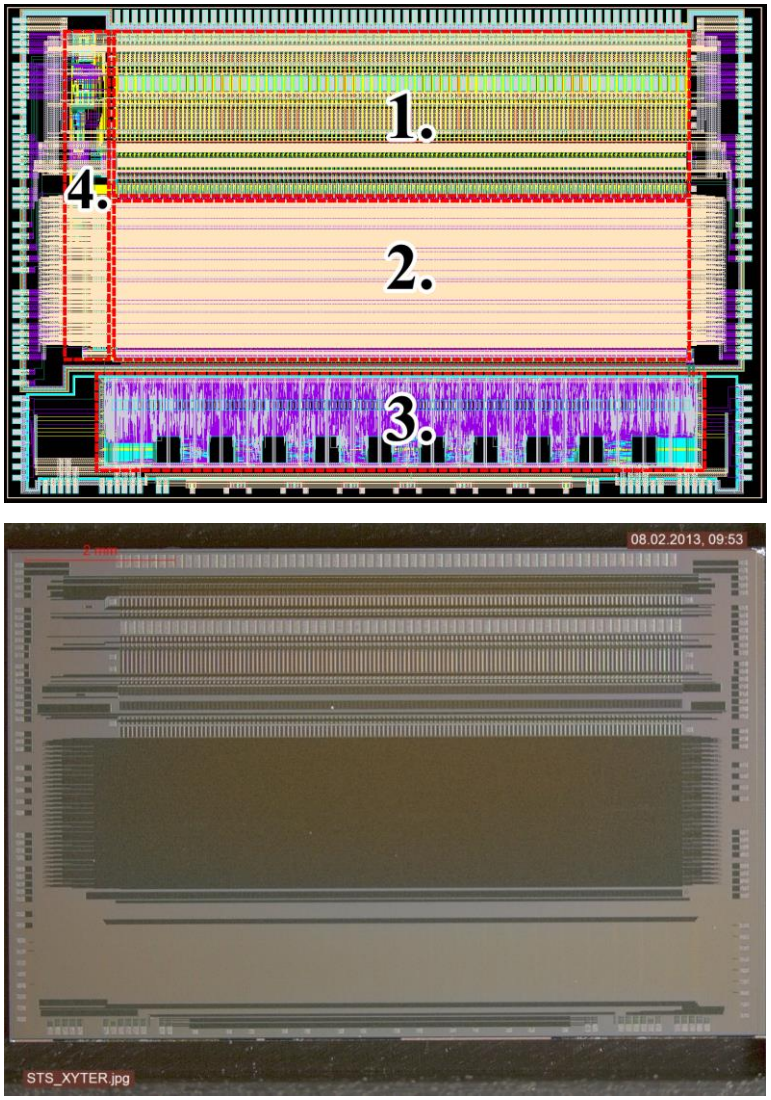

Fig. 2.16: a) STS-XYTER layout:
1. Analog front-end, 2. Flash ADC and DPD, 3. Readout logic and CBMnet, 4. Reference block,
b) STS-XYTER chip photograph.

2.4 Measurement results

The STS-XYTER ASIC was successfully designed and manufactured. Further task of the author was to prepare the test setup and testing procedure.

2.4.1 Test setup and testing procedure

The measurement setup consisted of the test PCB (Fig. 2.17), the NI-PXI system with the NI PXIe-7962R FPGA module and the arbitrary function generator Tektronix AFG3251C. The SysCore-v3 FPGA board and the oscilloscope were used for monitoring purpose. The test pulses of desired amplitude were generated by injecting a known, controllable charge to the input of the channels, using the external arbitrary function generator. The threshold voltages vTh<0> to vTh<30> were set to values from 0.01 V to 0.31 V with 0.01 V step, in pulse amplitude domain.

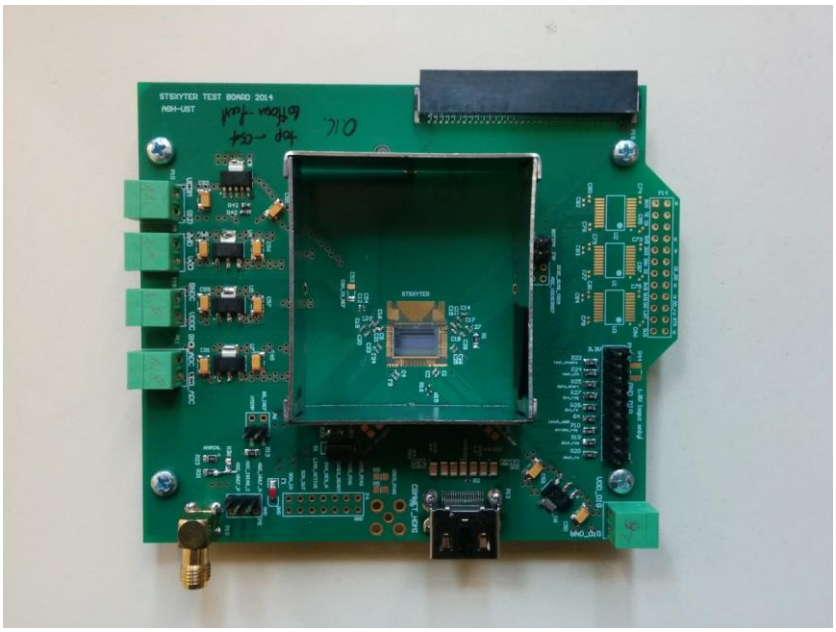

Fig. 2.17 STS-XYTER test PCB.

To measure the trim DAC characteristic, for every input word a corresponding comparator's threshold voltage have to be found. To determine the comparator's threshold voltage, an input pulse amplitude scan was performed and then the threshold voltage was read from an S-curve (Fig. 2.18). An amplitude scan runs as follows:

- the counters are reset,
- a known number of pulses with specified amplitude is generated,
- the registered number of counts is read from the counters,
- the pulse amplitude is incremented and the procedure is repeated.

Finally, an S-curve is obtained and the comparator's threshold voltage can be determined. After repeating the pulse amplitude scan for every DAC value a complete trim DAC characteristic is obtained.

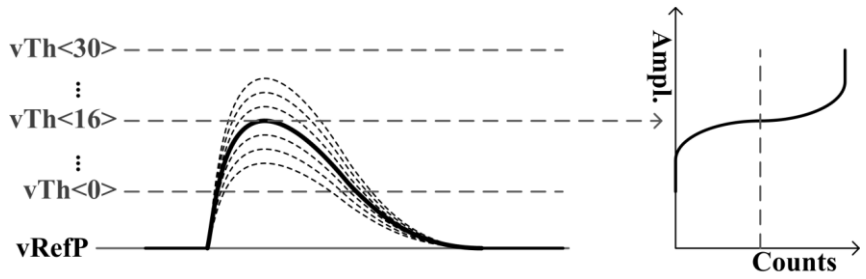

Fig. 2.18 Exemplary waveforms of the ADC input pulses and the obtained S-curve.

2.4.2 Trim DAC measurement results

The trim DACs across all 128 channels were measured. To effectively utilize the input amplitude range and cover all trim DAC values, only one trim DAC from each channel, at the threshold voltage of vTh = 0.23 V, was characterized. The resulting characteristics are presented in Fig. 2.19. The average trim DAC range is 331 mV and the average resolution is equal to 1.3 mV. The obtained voltage span meets the requirements and the non-monotonicities occur only at the boundaries of the fine DAC range.

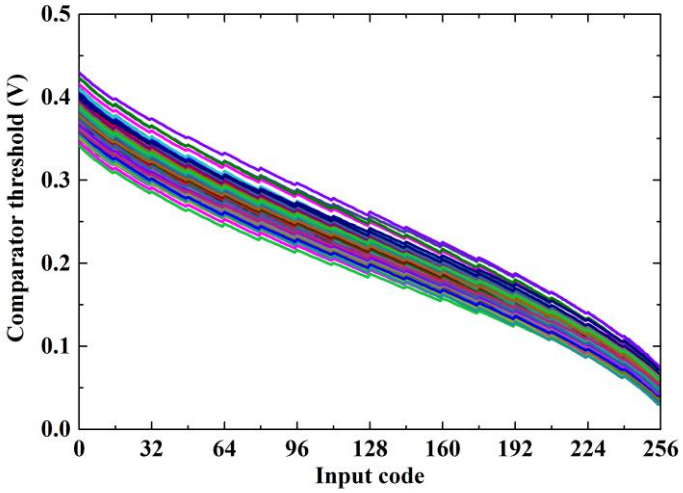

Fig. 2.19 Measured trim DAC's characteristics.

2.4.3 Comparator offset voltage correction results

To measure the effectiveness of the offset correction method, first all trim DAC at the chosen threshold voltage of vTh = 0.17 V were written with the same value of 128. The obtained S-curves are presented in Fig. 2.20.

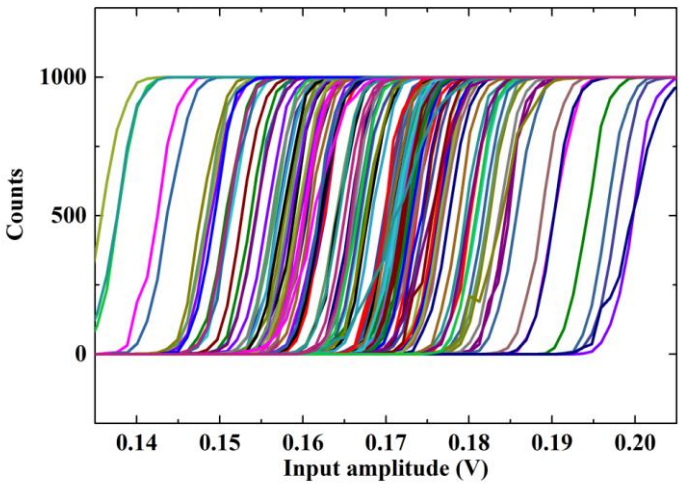

Fig. 2.20 S-curves at the threshold voltage vTh = 0.17 V, before correction, σvTh = 12.3 mV.

Secondly, for each comparator a specific trim DAC value, corresponding to the desired threshold voltage, was found. Fig. 2.21 presents these S-curves after correction. The threshold voltage standard deviation before and after correction is 12.3 mV and 0.75 mV respectively, giving a correction factor of 16.4.

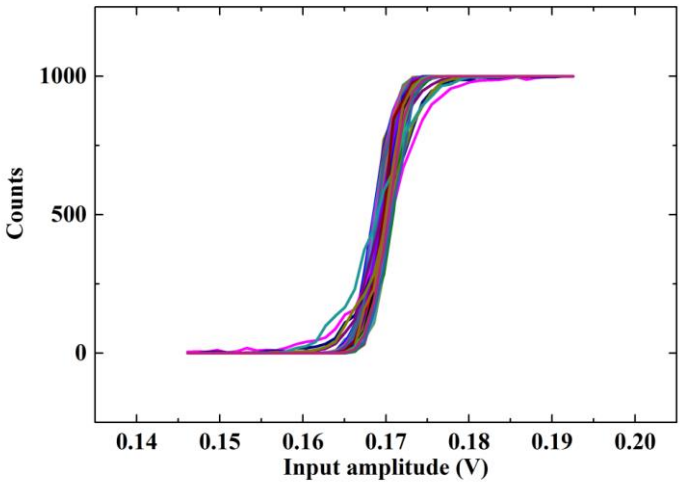

Fig. 2.21 S-curves at the threshold voltage vTh = 0.17 V, after correction, σvTh = 0.75 mV.

2.4.4 ADC performance

To allow ADC characterization, a full-chip correction procedure was performed. After a full-scale pulse amplitude scan, nonlinearity characteristics of ADCs in all 128 channels were obtained (Fig. 2.22). The maximum INL and DNL are 0.16/-0.15 LSB and 0.22/-0.24 LSB respectively.

Because the ADC operates in an asynchronous, pulsed manner and its sampling frequency is determined by the rate of the input pulses, which is limited by the analog front-end processing time, the dynamic performance, such as signal-to-noise-and-distortion and effective number of bits cannot be measured directly.

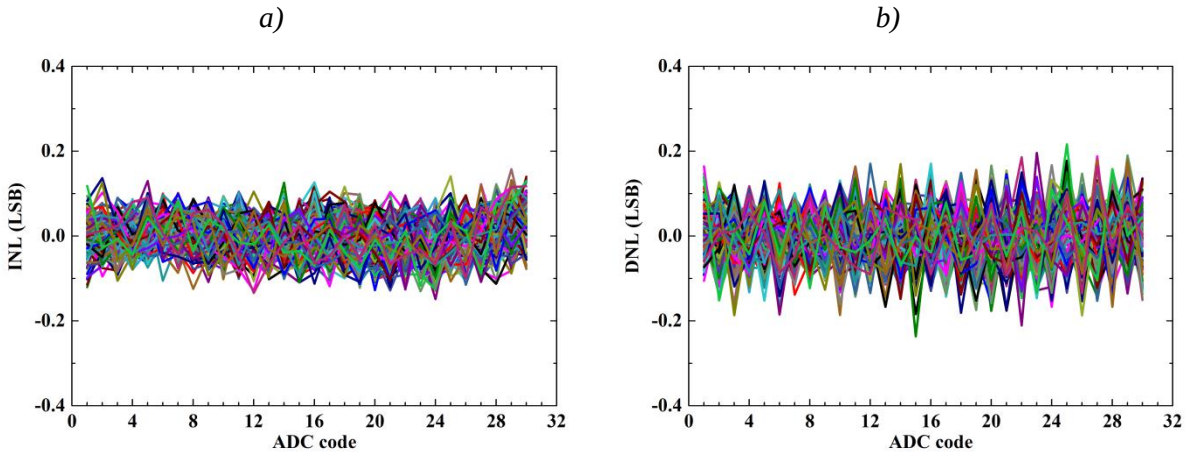

Fig. 2.22 ADC nonlinearity in 128 channels, after correction: a) integral, b) differential.

2.5 Summary

A 5-bit multichannel pulse amplitude measurement system, based on a flash ADC array was presented. The system uses a novel low-area comparator offset voltage correction circuit. It bases on a two-stage trim DAC design and it allows to significantly lower its area consumption per single channel [30]. It was estimated, that the area occupied in each channel by the presented 8-bit trim DAC can be used as:

- 6-bit conventional current steering DAC, built of the same transistors as the fine DAC, with similar nonlinearity,
- 8-bit conventional current steering DAC, built of quarter-size transistors of the fine DAC, with approximately four times higher nonlinearity,

where the nonlinearity term denotes to the trim DAC's DNL standard deviation.

The solution was successfully implemented in the self-triggering 128-channel readout system, which will be a part of the STS detector system in the upcoming CBM experiment at FAIR.

3. SMALL AREA SUCCESSIVE APPROXIMATION ADC FOR PIXEL SYSTEMS

3.1 Introduction

Pixel systems with pulse amplitude measurement usually require ADC of moderate resolution of 6 - 8 bits and sample rate of up to few megasamples per second [31]. The commonly used architecture for such applications is a single-slope, Wilkinson type ADC [32]. The main properties in favor of this solution are its very limited analog circuitry and low area occupancy. Its major disadvantage is the exponential relation between the conversion time and the resolution, which results in low conversion rates or requires a very high-speed clock.

In this section the successive approximation architecture for the aforementioned applications is considered. The main advantage of this solution is its very good energy efficiency. Additionally, it is well suited for the modern manufacturing processes, as the comparator is the only analog block and the conversion process bases almost exclusively on passive elements. The design of a 7-bit successive approximation ADC, which is suitable for the pixel systems with pixels of moderate size in the order of 200 μm × 200 μm is presented in this chapter.

3.2 Architecture overview

3.2.1 Successive approximation principle

The idea of the conversion process in a successive approximation architecture bases on a DAC in a feedback loop. In the first phase the analog input voltage is sampled and stored. Then, in the second phase, a digital word is found for which the DAC output voltage matches the stored input voltage most closely. This word is a digital representation of the input voltage and the output of the ADC. The block diagram of this architecture is presented in Fig. 3.1.

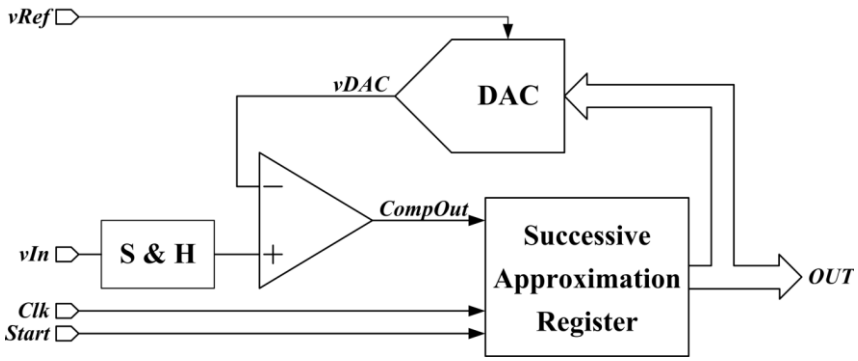

Fig. 3.1 Block diagram of the SAR ADC.

The output word is found bit-by-bit, starting from MSB, by means of the comparator. First, the most significant bit is set to '1', while the rest are set to '0'. If the resulting DAC output voltage vDAC is smaller than the held input voltage, the bit remains at '1', otherwise it is reset to '0'. The procedure is

repeated for the subsequent bits. For a n-bit resolution ADC, the conversion requires n clock cycles for determining the output word and at least one cycle for sampling the input voltage. An exemplary conversion process is presented in Fig. 3.2.

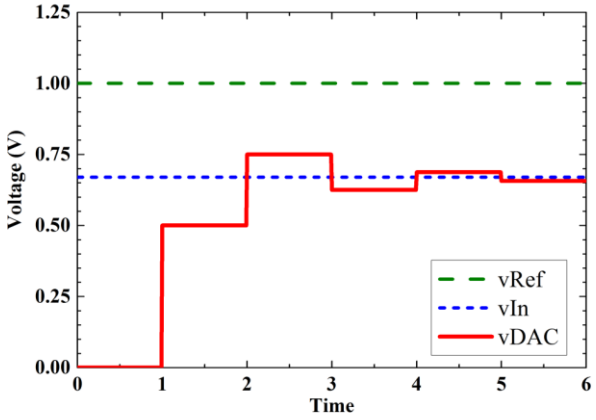

Fig. 3.2 Exemplary conversion process – vDAC → vIn.

The disadvantage of the presented algorithm is the fact, that the DAC's output voltage vDAC tends to the input voltage vIn. As these voltages are compared in every step, the comparator has to operate over the entire input signal range. This results in a complex comparator design, due to larger input common mode voltage range requirement.

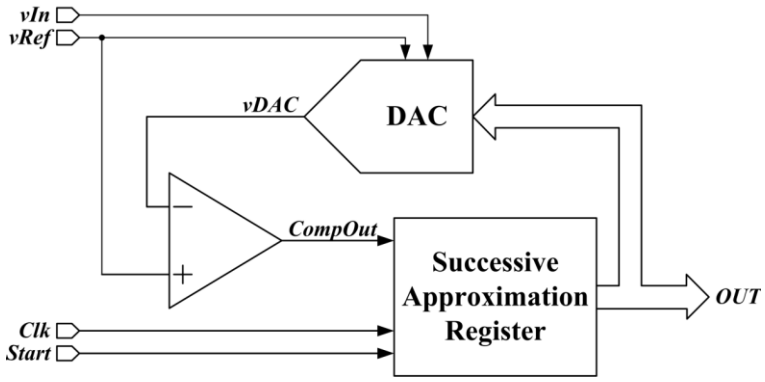

Fig. 3.3 Block diagram of the SAR ADC, complementary algorithm.

A solution can be a modified successive approximation algorithm. In the complementary algorithm (Fig. 3.3) the tested voltage is obtained from sum of the DAC output voltage and the stored input voltage. This approach requires different DAC design, which allows the sample and hold functionality. The tested voltage tends to the reference voltage vRef, thus the comparison always takes place near the reference voltage, hence the algorithm relaxes the requirements of the comparator's input voltage common range. The DAC's input word is the binary complement of the input voltage's digital representation. An exemplary conversion process is presented in Fig. 3.4.

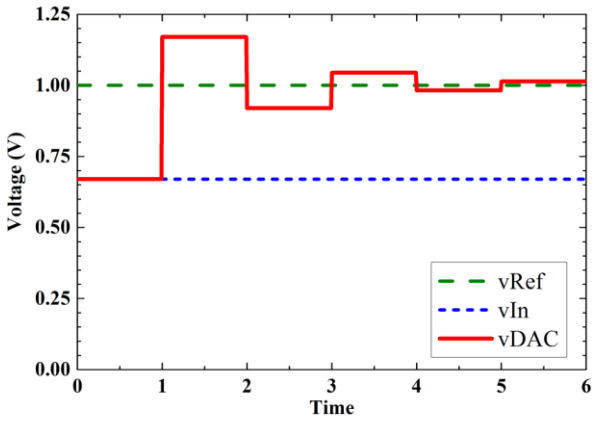

Fig. 3.4 Exemplary conversion process for a complementary algorithm – vDAC → vRef.

3.2.2 Charge redistribution converter architecture

The presented ADC design uses the complementary approximation algorithm. A practical implementation of the complementary successive approximation algorithm is the charge redistribution ADC. In this approach, a charge sharing converter is used as a DAC combined with sample-and-hold circuit [33]. The schematic diagram of 4-bit implementation of such circuit is presented in Fig. 3.5.

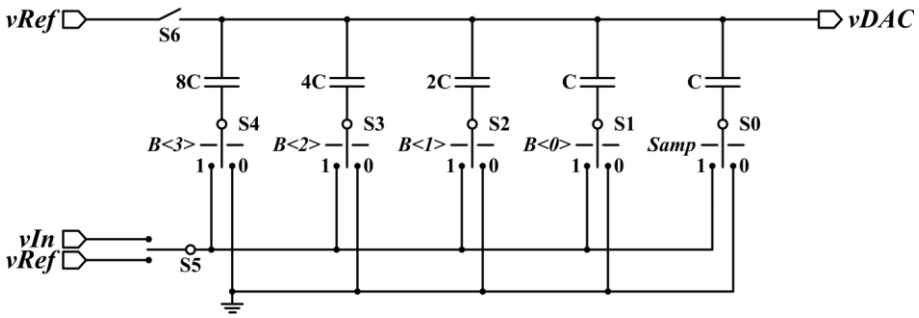

Fig. 3.5 Schematic diagram of the charge redistribution converter.

It consists of a binary-weighted capacitor array. Each capacitor consists of a multiplies – equal to the powers of two – of a unit capacitor C, where the smallest capacitor in the array is made of a single unit capacitor. The top-plate is common to all capacitors and it is also the output of the converter vDac. The bottom plate of each capacitor can be switched independently between the input voltage vIn – during the sampling phase – or between the reference and ground voltages during the charge redistribution phase. The voltage stored on the capacitor array in the sampling phase is maintained during the whole redistribution phase and is added to the output voltage of the converter resulting from the capacitance ratio.

a)

b)

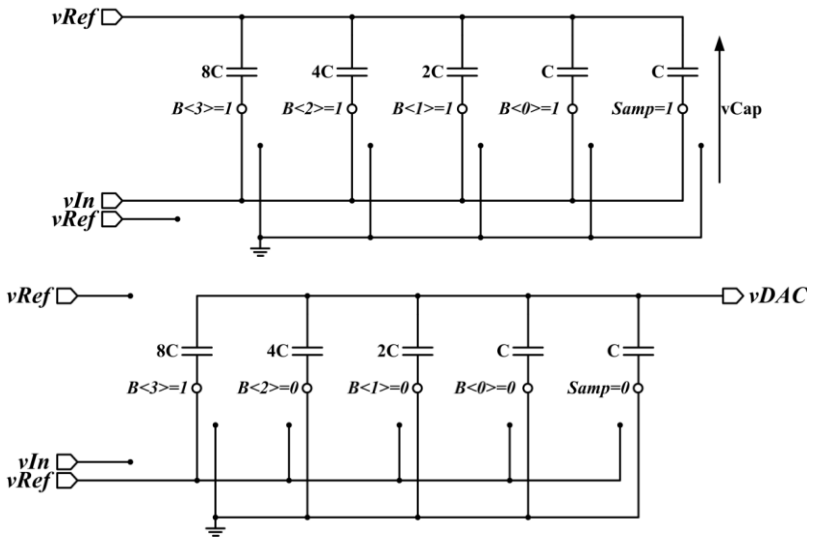

Fig. 3.6 Conversion process: a) sampling phase, b) beginning of the charge redistribution phase.

The conversion process is depicted in Fig. 3.6. In the first phase the input voltage is sampled. Switches S4 – S0 connect the bottom plate of all capacitors to the voltage vIn, switch S5 is on and connects the top plate to the reference voltage vRef. The voltage on the capacitor array is equal to:

$$vCap = vRef - vIn. \tag{3.1}$$

In the second phase the actual charge redistribution begins – the switch S5 is turned off, and switches S4 – S0 are connected to either vRef or ground. The output voltage vDAC is equal to:

$$vDAC = \frac{C_{TOP}}{C_{DAC}} \cdot vRef + vCap, \tag{3.2}$$

where C_{TOP} is the sum of capacitors connected to the vRef voltage and the C_{DAC} is the sum of all capacitors in the DAC.

At the end of the redistribution process the output voltage $vDAC_{FINAL}$ is nearly equal to the reference voltage vRef:

$$vDAC_{FINAL} = vRef, \tag{3.3}$$

thus, substituting equations (3.1) and (3.3) into (3.2) we obtain:

$$vRef = \frac{C_{TOP\_FINAL}}{C_{DAC}} \cdot vRef + vRef - vIn \Leftrightarrow vIn = \frac{C_{TOP\_FINAL}}{C_{DAC}} \cdot vRef. \tag{3.4}$$

Therefore, after the charge redistribution process, the DAC's output voltage $vDAC_{FINAL}$, resulting from the capacitance ratio, is equal to the input voltage vIn, hence the DAC input word is the digital representation of the input voltage.

The digital-to-analog converter is the most important block in the charge redistribution ADC design, as it determines its resolution and linearity. The resolution of a charge sharing converter depends on the number of capacitors in the array. To increase it by one bit, it is necessary to double the number of capacitors in the array. From the power consumption, sampling rate and area occupancy point of view, it is desired to use capacitors of small value. However, there are two factors limiting the minimum capacitor size: mismatch and thermal noise.

3.2.3 Charge-redistribution converter accuracy - mismatch

In modern technologies, for the low-to-moderate resolution data converters, the mismatch effect is the main factor limiting their accuracy. In charge redistribution converters, it affects the ratio between the consecutive capacitors in the array, which is ideally equal to 2, and results in uneven voltage steps for the succeeding DAC's codes. The absolute error value depends on the difference in capacitor's arrangements for the given codes. The largest error arises at the MSB transition, when arrangement of all capacitors is changed: the MSB capacitor is connected to the reference voltage, while the remaining capacitors to the ground for the 100… code and vice-versa for the 011… code. Assuming that unit capacitor's value has a standard distribution with mean value of C and standard deviation of $C \cdot \sigma_C$, the resulting error voltage v_{ERR_MSB} when switching between these two codes has a standard deviation of:

$$\sigma v_{ERR\_MSB} = \sigma_C \cdot vRef \cdot \frac{\sqrt{2^N - 1}}{2^N}, \tag{3.5}$$

where N is the resolution of the converter [34][35].

The unit capacitor value has to be large enough, so as its mismatch does not deteriorate the DAC's accuracy, i.e. the voltage error is smaller than ½LSB. As the largest error arises at the MSB transition, it can be treated as the boundary case; therefore, assuming 3σ margin, corresponding to 99.7% of occurrences, the following condition for the DAC's accuracy is stated:

$$3 \cdot \sigma v_{ERR\_MSB} \leq ½ \cdot v_{LSB}, \tag{3.6}$$

where v_{LSB} is the minimum voltage step of the DAC, equal to:

$$v_{LSB} = vRef \cdot \frac{C}{C_{DAC}} = \frac{vRef}{2^N}, \tag{3.7}$$

Substituting equations (3.5) and (3.7) into equation (3.6), the condition for required unit capacitor's maximum standard deviation is obtained:

$$\sigma_C < \frac{1}{6\sqrt{2^N - 1}}. \tag{3.8}$$

3.2.4 Charge-redistribution converter accuracy – thermal noise

The thermal noise in charge redistribution converters manifests itself during the sampling procedure. The voltage stored on the capacitor array vCap (see Fig. 3.6a) is affected by the thermal noise v_N, given by the equation:

$$v_N = \sqrt{\frac{k_B T}{C}}, \tag{3.9}$$

where k_B is the Boltzmann constant and T is the absolute temperature [36]. After the switches are turned off, the voltage on the capacitor array is frozen and the thermal noise voltage is added to the sampled one.

The sampling circuit's capacitance has to be large enough, so as its thermal noise does not deteriorate the ADC's accuracy. The minimal values of the sampling capacitors required to achieve a given resolution are included in Table 3.1.

Table 3.1 Minimum total DAC capacitance C_{DAC} for $v_N \leq$ ½ LSB, vRef = 1 V.

Resolution	C_{DAC}
4	4.24 aF
6	67.9 aF
8	1.09 fF
10	17.4 fF
12	278 fF
16	71.2 pF
20	18.2 nF
24	4.66 µF

The thermal noise may pose a limit in high resolution, high accuracy ADC designs, however for the discussed resolution range it is irrelevant.

3.2.5 Split-DAC architecture

The total number of capacitors so as the total DAC's area increases exponentially with resolution. The first intuitive remedy is to use devices of smaller size. However, because of the routing overhead and technology layout rules for minimum device size and spacing, decreasing the device area below a certain point is ineffective.

Therefore, to reduce the number of devices and area occupation of the DAC, a split-DAC architecture is often used. This approach bases on dividing the DAC into two parts – primary DAC and a secondary sub-DAC. The primary DAC determines the most significant bits, while the sub-DAC – the remaining ones. This solution allows to use two smaller DACs instead of a large, single one [37].

However, the primary DAC still has to maintain the full-DAC's resolution, thus the used devices has to be larger, adequately to the total DAC resolution, to provide sufficient matching.

The example of a charge sharing converter using split-DAC architecture is presented in Fig. 3.7. It is built of 2^N-1 capacitors C forming the primary DAC and 2^M capacitors for the sub-DAC, giving the total resolution of M+N bits.

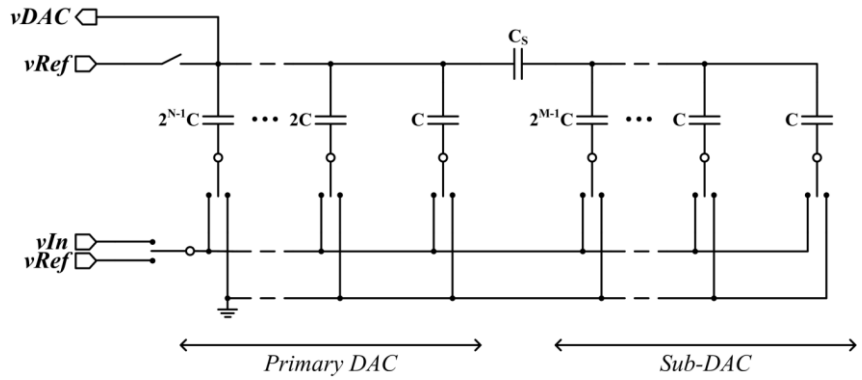

Fig. 3.7 Schematic diagram of the split-DAC converter with scaling capacitor C_S.

Value of the additional scaling capacitor is given by the equation [38]:

$$C_S = C \cdot \frac{2^M}{2^M - 1}. \qquad (3.10)$$

The sub-DAC does not have to be of the same type as the primary DAC. For the charge sharing converter, in principle any DAC with voltage output can be used as a sub-DAC. In Fig. 3.8 a split-DAC variant with a resistive sub-DAC, with a total resolution of M+N is presented.

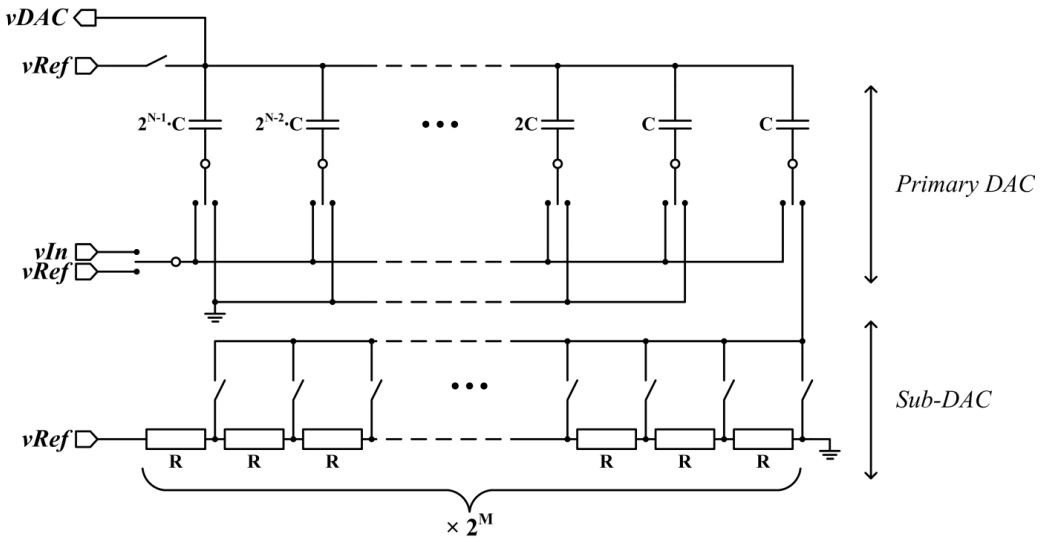

Fig. 3.8 Schematic diagram of the split-DAC converter with resistive sub-DAC.

3.3 Design

3.3.1 Digital-to-analog converter

In the used technology even the minimum-sized capacitors has matching characteristics that fulfill the condition (3.8) with a large margin. Employing only such devices would lead to unnecessarily large area and capacitance of the DAC. Therefore, a split-DAC architecture is implemented.

The capacitive split-DAC with scaling capacitor (Fig. 3.7) is sensitive to the variations of scaling capacitor value and the parasitic capacitance at the output of the sub-DAC, hence it requires a parasitic charge cancelation or trimming circuits. These techniques increase the circuit complexity, area occupancy and involve additional operation effort (calibration procedure).

The accuracy of split-DAC with resistive sub-DAC (Fig. 3.8) can be guaranteed with only proper device scaling. Monotonicity of the resistive sub-DAC is guaranteed by its structure. Its disadvantage is the static current. However, the power consumption penalty can be reduced by turning on the sub-DAC only for determining the least significant bits, and turning it off during the rest of the ADC operation, by means of an additional switch.

In spite of the aforementioned facts, a split-DAC with resistive sub-DAC is chosen. To choose the optimal ratio between the primary and sub-DAC resolution, a power-area estimations for all possible combinations were conducted. The calculations were done according to the following assumptions:

- The sample rate is equal to 500 kS/s and the reference voltage to 0.8 V.
- The capacitive DAC has to maintain the full-converter resolution accuracy. Therefore, its total capacitance is constant and set to fulfill the condition (3.8).
- The capacitive DAC is divided into a corresponding number of unit capacitors. It is built of MIM capacitors with capacitance density of 1 fF/μm^2. Its estimated total area takes into account the technology layout rules for the CMOS 180 nm process, such as minimum device area and spacing.
- The capacitive DAC's estimated average power consumption is basing on a conventional binary search switching procedure, with an average switching energy equal to:

$$E_{AVG} = \left(\sum_{i=1}^{N}\left(2^i - 1\right) \cdot 2^{N+1-2i}\right) \cdot C_{LSB} \cdot vRef^2, \qquad (3.11)$$

  where N is the resolution of the capacitive DAC and C_{LSB} is the smallest capacitor [39].
- A resistor, which layout fulfills the minimum technology recommended layout rules, has matching characteristic that suffices for the resolution range under consideration. The most important factor affecting the choice of type and size of the unit resistor is the power consumption and area occupancy of the resistive sub-DAC. Therefore, a high-resistive poly

resistor type, with the highest sheet resistance available, is chosen. Also, to simplify the calculations, the unit resistor size is constant for all configurations and is equal to:

$$W_R/L_R = 2\ \mu m\ /\ 30\ \mu m.$$

- Resistive DAC's power consumption estimation takes into account operation only for determining the required bits.
- The total area and power consumption does not take into account the other ADC components, such as the switches, comparator and SAR.

The power-area estimations for different split-DAC configurations is summarized in Table 3.2.

Table 3.2 Comparison of different resistive split-DAC configurations.

Cap. bits	Res. bits	Capacitive DAC		Resistive DAC		Total	
		Area [µm^2]	Power [µW]	Area [µm^2]	Power [µW]	Area [µm^2]	Power [µW]
6	1	1730	0,14	170	2,53	1900	2,67
5	2	1216	0,14	340	2,53	1556	2,67
4	3	906	0,13	680	1,90	1586	2,03
3	4	713	0,12	1360	1,27	2073	1,38
2	5	589	0,09	2720	0,79	3309	0,89
1	6	509	0,05	5440	0,47	5949	0,53

The configuration with 4-bit capacitive DAC and 3-bit resistive sub-DAC is chosen, because of the smallest area occupancy and 24% lower power consumption than the second-best option. The diagram of the capacitive DAC and the resistive sub-DAC is presented in Fig. 3.9.

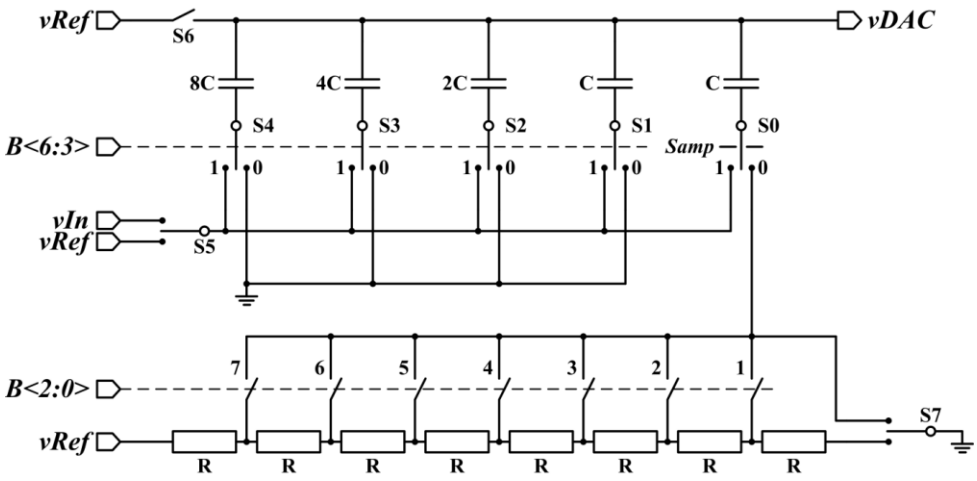

Fig. 3.9 Diagram of capacitive DAC and resistive sub-DAC.

The chosen unit capacitance is equal to C = 21.3 fF and the unit resistance equal to R = 15.7 kΩ.

The switch S8 is added to turn off the resistive sub-DAC when it is not necessary. While not in use, all sub-DAC's switches are open, its output is connected to the ground and the circuit consumes no current. Therefore, for continuous ADC operation and a typical reference voltage of 0.8 V, the sub-DAC power consumption is reduced from 5.1 µW to 1.9 µW.

All switches used in the design are transmission gates with W/L ratios equal to:

$$W_N/L_N = 0.44\ \mu m / 0.18\ \mu m,$$

$$W_P/L_P = 0.88\ \mu m / 0.18\ \mu m.$$

3.3.2 Comparator

As the ADC has single-ended architecture, it introduces an imbalance at the comparator's inputs. The inverting input of the comparator is connected directly to the DAC's output, which is in simple terms a capacitive divider, while the non-inverting one to the reference voltage, which is a low-impedance voltage source (see Fig. 3.3). That fact makes the circuit very prone to the comparator kickback noise. To alleviate this effect, the comparator circuit is made up of two stages: the preamplifier and the latch.

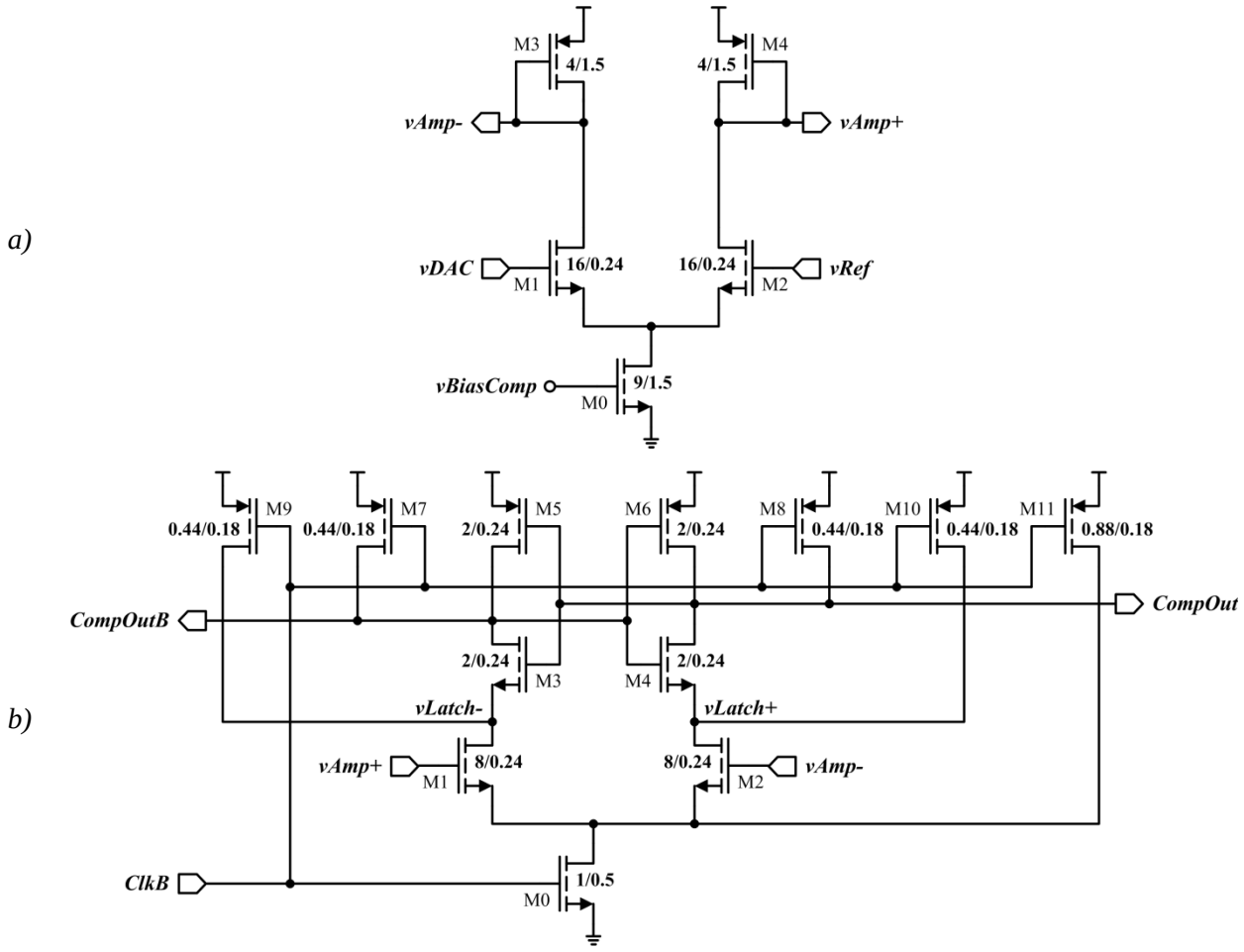

Fig. 3.10 Scheme of the comparator: a) preamplifier, b) synchronous latch.

The preamplifier (Fig. 3.10a) is built of a differential pair, consisting of transistors M1-M2, with diode-connected transistors M3-M4 acting as a load. Its main role is to act as a buffer between the sensitive DAC output and the second stage of the comparator.

Settling time of the preamplifier's output is a main factor limiting the speed of the circuit. The bias current of the transistor M0 was chosen so as the worst-case settling time is lower than the nominal single clock period and is equal to 500 nA.

The main stage of the comparator is the synchronous latch (Fig. 3.10b). It is built of a differential pair M1-M2 with cross-connected inverters M3-M6 acting as a load. It is a dynamic circuit which operates in two phases. In the first, reset phase, when the ClkB signal is low, all nodes are connected to the power supply line, to avoid memory effects. As the M0 transistor is turned off, the circuit does not consume any current in this phase. After rising ClkB edge, circuit starts the regeneration phase. Transistor M0 is turned on and transistors M1 and M2 start conducting current, which value depends on the input voltages vAmp+ and vAmp-. The electrical potential of the corresponding nodes vLatch- and vLatch+, so as the output nodes CompOut and CompOutB is decreasing at different rates. When the voltage difference between the output nodes is large enough, the positive feedback loop is formed and the circuits enters one of two stable states, with one of the outputs set to high and the other one to low, which indicates the end of the regeneration phase. In this state the circuit also does not consume any current.

The transistors M7-M11 serve as switches, pulling all internal nodes to the supply voltage during the reset phase, to prevent any memory or hysteresis effects.

The comparator does not have any offset correction circuit. In the presented architecture, the comparator's input offset voltage is directly added to the measured input voltage, thus it results in a shift of the ADC's transfer characteristic, but it does not affect its linearity.

3.3.3 Successive Approximation Register

The Successive Approximation Register (SAR) is a digital control block responsible for generating the comparator and DAC control signals. The circuit is designed in full-custom manner to ensure minimum area occupancy.

The simplified block diagram of the SAR is presented in Fig. 3.11. It is build up of two parts: the D flip-flops string, forming a one-hot counter and D latches, responsible for holding the current DAC input word.

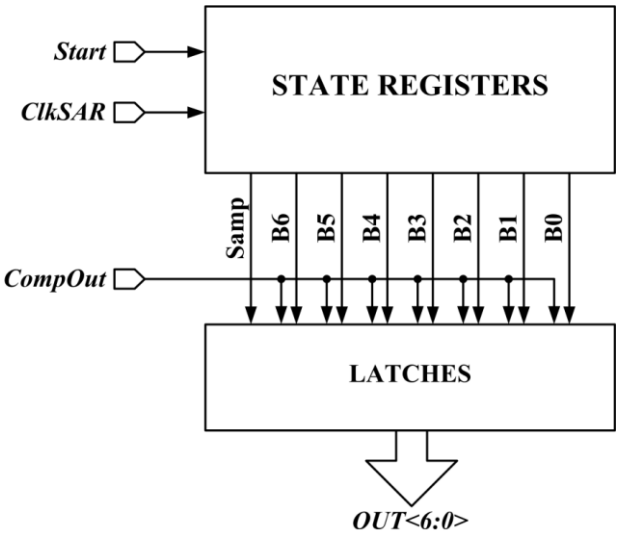

Fig. 3.11 Block diagram of Successive Approximation Register.

Single conversion last for a period of at least 8 clock cycles, of which the actual conversion lasts for 7 clock cycles and at least 1 clock cycles is necessary for sampling the input voltage. The circuit is designed to work at clock frequencies up to 20 MHz, which corresponds to a maximum sampling rate of 2.5 MS/s.

3.3.4 Comparator-based clocking

The presented A/D converter is a synchronous design, which uses both edges of the clock signal. The rising edge drives the SAR logic, which sets the next DAC input word depending on the comparator's output, while the falling edge triggers the synchronous latch and determines the comparison time. However, the settling time of the DAC and preamplifier is much longer than the latch's propagation delay. Also, when the regeneration state of the synchronous latch is over, its output is stable and next bit can be tested. Therefore, it would be beneficial if the clock signal had a duty cycle higher than 50%.

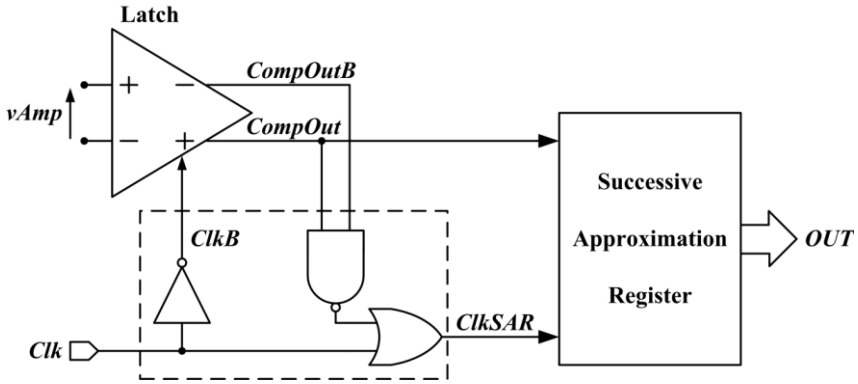

Fig. 3.12 Comparator-based clocking idea block diagram.

The appropriate clock signal is generated on-chip. It is derived from the original symmetrical clock signal and the differential outputs of the comparator. It bases on a fact, that during the reset state both outputs are in high state, whereas when the output is valid one of them is in high state and the other one – in low. The internal ClkSAR signal is obtained, which drives the SAR logic and set the DAC input word earlier, before the next rising Clk edge. The idea block diagram of this solution is depicted in Fig. 3.12.

The preamplifier required settling time is relaxed significantly. As the regeneration phase usually lasts for about 1 ns, which is much shorter than the clock period, the maximum allowed settling time is increased almost by a factor of two. The exemplary waveforms and digital control signals of comparator-based clocking are presented in Fig. 3.13.

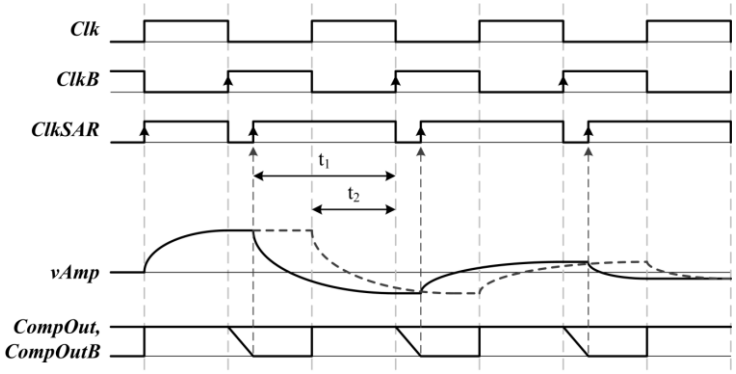

Fig. 3.13 Comparison of preamplifier settling time: t1 - comparator-based clocking, t2 - conventional clocking.

3.3.5 Layout

The charge sharing converter is the circuit, which accuracy to large extent depends on its layout. In order to avoid nonlinearity errors, parasitic capacitances formed between the switches and the DAC output node must scale proportionally to the values of the corresponding capacitors. To achieve this, careful and uniform routing, verified by post-layout analysis, is required. Additionally, dummy structures were added at the borders of the array, to provide similar surrounding for all capacitors.

The ADC layout is presented in Fig. 3.14. The total area is approximately 90 μm × 95 μm. Proportional area occupation of specific blocks is summarized in Table 3.3.

Table 3.3 Area occupancy of specific blocks.

DAC	40%
Comparator	5%
SAR	25%
Routing, etc.	30%

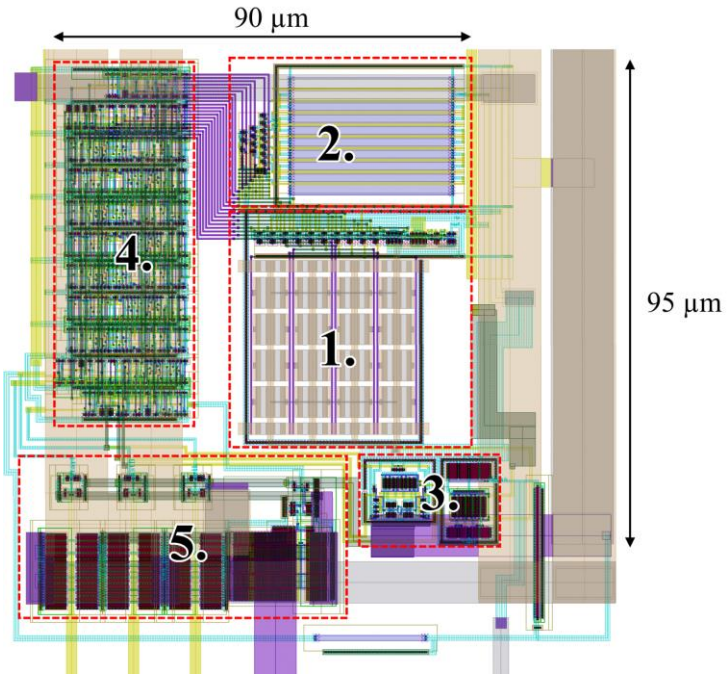

Fig. 3.14 Chip layout: 1. Charge sharing primary DAC, 2. Resistive sub-DAC, 3. Comparator, 4. SAR, 5. Output buffers and protection diodes.

The described ADC design was implemented as a part of multi-project ASIC. The chip photograph with the wire-bonded ADC structure is presented in Fig. 3.15.

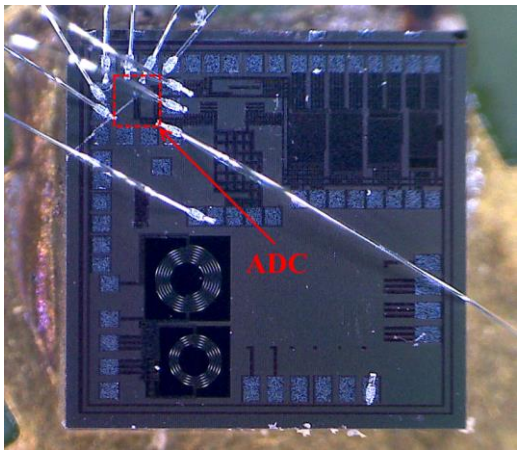

Fig. 3.15 Test chip photograph.

3.4 Measurement results

The chip was implemented in 180 nm CMOS technology. It was tested with the NI sbRIO 9636 evaluation board with Xilinx Spartan-6 FPGA and two 16-bit DACs. The bit stream was controlled by the FPGA software.

A ramp histogram test was performed to measure the static performance of the converter. Obtained integral and differential nonlinearity plots are presented in Fig. 3.16. The peak INL and DNL are

+0.29/-0.28 LSB and +0.23/-0.35 LSB respectively. These results confirm the proper choice of the DAC's elements in terms of matching.

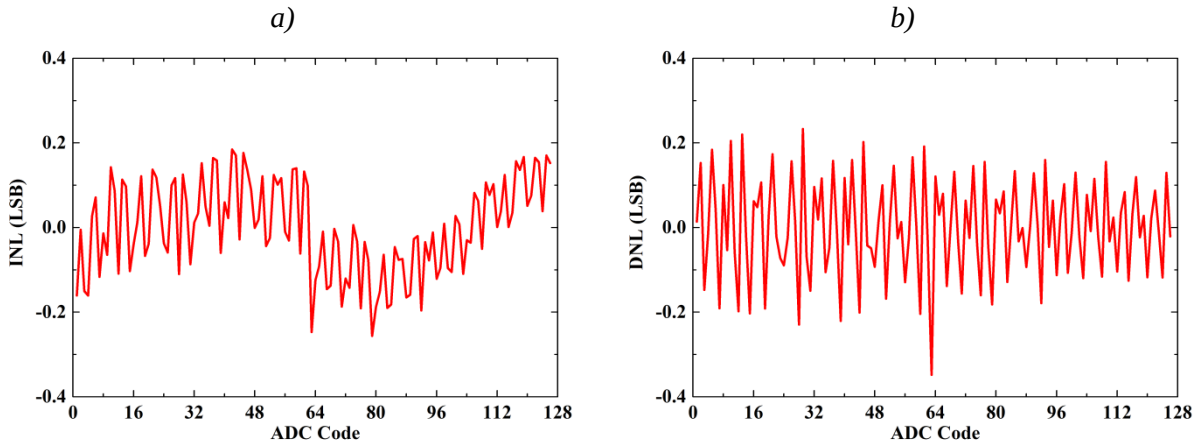

Fig. 3.16 a) Integral nonlinearity, b) differential nonlinearity.

To verify the dynamic performance of the converter a sine test was conducted. The ADC sample rate was set to nominal 500 kS/s, however, due to the limitation in the used external reference DAC's update rate, the ADC output data was decimated by a factor of 4. The FFT plot for a full-scale, 62.3 kHz sinusoidal signal is presented in Fig. 3.17. Obtained SINAD is equal to 41.2 dB, which corresponds to 6.54 effective bits, while SFDR is equal to 56.4 dB.

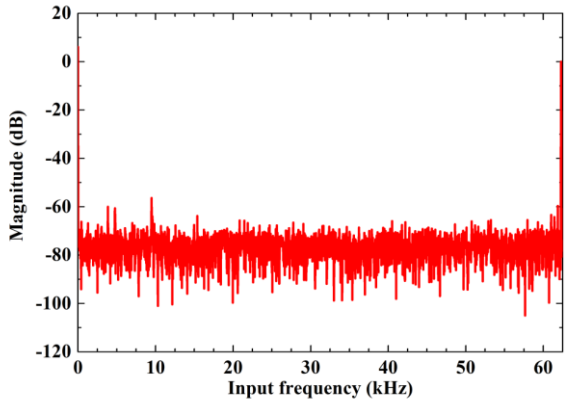

Fig. 3.17 Signal spectrum of 62.3 kHz input, sampled at 125 kS/s, 4 MHz clock frequency.

The power consumption of the specific blocks is presented in Table 3.4. The comparator and SAR are supplied from the single 1 V line, while the DAC is using the 0.8 V external reference voltage. The power consumption of the DAC is relatively high compared to the rest of the converter. Most of it comes from the resistive divider, which is active for at least ⅜ of the conversion time and consumes static current, regardless of the used sampling rate. However, this is the cost of the reduced area occupation of the circuit.

Table 3.4 Power consumption.

Comparator + SAR	2.45 µW
DAC	2.0 µW

Table 3.5 summarizes the measured parameters of the presented converter.

Table 3.5 ADC parameters summary.

Process	180 nm
Power Supply	1.0 V
Resolution	7 bits
Sampling rate	500 kS/s
Clock frequency	4 MHz
Power consumption	4.45 µW
Input voltage range	0 – 800 mV
INL	+0.18 / -0.25 LSB
DNL	+0.23 / -0.35 LSB
ENOB	6.54
FoM	96 fJ/conv.step
Area	90 µm × 95 µm

3.5 Summary

The design of a 7-bit SAR ADC dedicated to low-power multichannel systems was demonstrated. The proposed converter is characterized by very low nonlinearity and good energy efficiency. It has very low silicon area occupancy of 90 µm × 95 µm, which is one of the best results for this resolution range. These properties allow to use it even in systems with very-low area requirements.

The comparison of the similar ADC designs is presented in Table 3.6.

Table 3.6 Comparison of similar ADC designs.

	[40]	**[41]**	**[42]**	**This work [43]**
Technology	130 nm	180 nm	130 nm	180 nm
Supply	1 V	1 V	1.2 V	1 V
Power Consumption	8.8 µW	6.15 µW	0.9 µW	4.45 µW
Sample Rate	1 MS/s	400 kS/s	100 kS/s	500 kS/s
ENOB	7.7	7.31	7.55	6.54
FoM	42.3	96.9	48	96
Area	0.164 mm^2	0.062 mm^2	0.07 mm^2	0.0085 mm^2
Relative Area	19.3	7.3	8.2	1.0

4. FLASH ADC WITH DYNAMIC OFFSET STORAGE FOR HIGH COUNT RATE IMAGING PIXEL SYSTEMS

4.1 Introduction

Nowadays, there is a growing interest in digital position sensitive X-ray imaging systems for biology, medicine, chemistry and solid state physics applications [44]. Such systems consist of an array of pixel sensors and readout electronics. In the most advanced imaging systems each sensor pixel has an individual readout channel to amplify the signal, increase SNR and convert analog information from sensor to digital domain. The example of such imaging system is a hybrid pixel sensor detector, consisting of a pixelated sensor and multichannel readout ASIC of pixel architecture (Fig. 4.1).

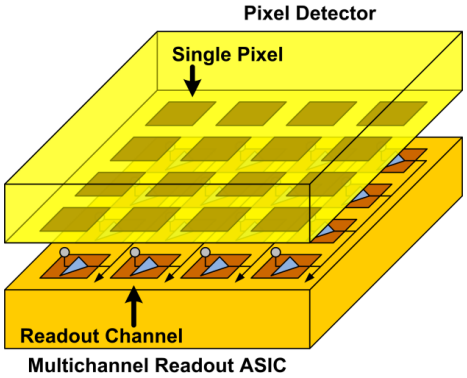

Fig. 4.1 Pixel detector with readout ASIC.

Solutions for fast X-ray digital imaging most frequently use one or a few discriminators per single channel [45]. This architecture is used in various imaging techniques, where it is sufficient to measure the spatial distributions of X-rays of energies above a given threshold or within a given energy window. The counters after the discriminators store the information about the number of hits - signals, which amplitude was higher than the given threshold level. As each channel works independently, this solution is suitable for very high intensity of X-rays (even more than 1 Mhits/s per single channel). To enable complete photon energy measurement, one of the required steps is to include an independent ADC in each pixel [46]. It is an emerging subject, as there are currently no solutions implementing an ADC in pixel size smaller than 100 µm × 100 µm. Such improvement would also help to solve the charge sharing issue and simplify the chip correction procedure.

Design of an ADC suitable for pixel measurement system is a demanding task. As the available area and power consumption are very limited, such applications favor simplicity in choice of the ADC architecture. Various correction methods, like trimming [47] or redundancy [48] require too much area, therefore different solution is necessary. Asynchronous, clock-less operation is also beneficial, as it eliminates the necessity of power-hungry clock tree distribution. Because of the above conditions and the low-resolution requirement, an asynchronous flash converter architecture was chosen.

To keep the area of the ADC as low as possible, comparator has to be built of very small transistors. This arises problem with random offset voltage variation due to mismatch effects, which results in significant nonlinearities, even for a low resolution ADC. As there is no possibility for an additional trim DAC for every comparator, because area requirement of this method is too high, therefore a dynamic offset storage technique is chosen.

Another issue is the triggering scheme of the ADC. As the incoming pulses have stochastic distribution, an asynchronous trigger for the dynamic offset compensation is required. The solution is to use two shaper amplifiers – fast and slow (see section 2.2). The fast shaper has low peaking time and high gain, while its noise level and linearity are not as important. Its task, together with a discriminator, is an early pulse detection and generating the ADC's trigger signal. The slow shaper delivers the input signal for the ADC, therefore it has lower noise and higher linearity, in expense of higher peaking time.

The ADC design has been implemented in two technologies: a wide-spread and inexpensive 180 nm CMOS and a modern 40 nm CMOS process, for further architecture development and possible application in future systems. To make the comparison between the technologies more meaningful and to clearly estimate the advantages of moving the circuit to a newer technology node, both converters use the same architecture and were designed in a way to make the main parameters, such as the sampling rate and input voltage range, identical. Both ADCs have resolution of 4 bits, nominal sample rate of 5 MS/s and the input voltage range equal to 300 mV

4.2 Architecture overview

The top level block diagram of the single flash ADC is presented in Fig. 4.2. It is built of three functional blocks: a threshold voltages reference, a comparator array and a binary encoder. In the final multichannel system, the threshold voltages can be common to all channels, while the comparator array and the encoder has to be present in each channel individually. Also the clock signal has to be generated locally, separately in each channel, by a additional discriminator. As the comparator uses dynamic offset storage and no digital offset correction is foreseen, there is no need for additional diagnostic circuitry, such as counters or memory registers.

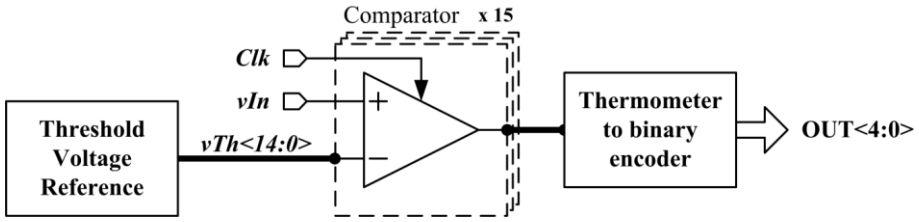

Fig. 4.2 Flash ADC block diagram.

4.3 Design

4.3.1 Threshold voltage reference

A resistor ladder is used as a threshold voltage reference, as described in section 2.3.5. The used resistor's types and values are summarized in Table 4.1. Because the test chips consist of only single ADC, there are no issues with inter-channel cross-talk, therefore the resistor's values are relatively large. However, in the final multichannel implementation, their values will have to be lowered significantly.

Table 4.1 Threshold voltage reference resistors.

	180 nm	**40 nm**
Resistor Type	N-Diffusion	N-Polysilicon
Value	1.16 kΩ	3.12 kΩ

4.3.2 Comparator

The chosen comparator offset compensation method is the input offset storage technique. A simplified single comparator diagram is depicted in Fig. 4.3. It operates in two phases: Φ_1 - offset storage phase and Φ_2 - comparison phase (Fig. 4.4). In the first phase the feedback loop is closed and the comparator is configured as an unity gain amplifier. The output voltage vAmp is equal to the sum of the voltage at non-inverting terminal, which is a corresponding to the threshold voltage vTh and a comparator input offset voltage. The capacitor C_S is connected between the output of the comparator and a reference voltage, hence the voltage across it equals to the comparator input offset voltage.

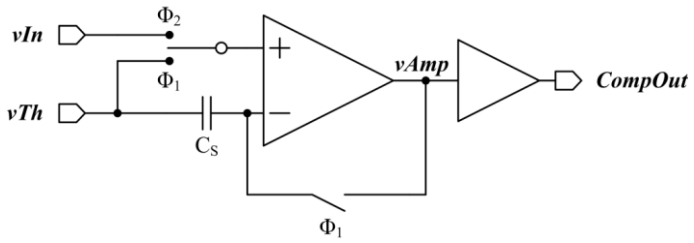

Fig. 4.3 Simplified diagram of a comparator with input offset storage.

In the second phase the feedback loop is opened and the input voltage is connected to the comparator's input. The capacitor with previously stored input offset voltage is connected in series with the reference voltage to the inverting terminal, compensating the comparator's offset voltage.

The main factors limiting the accuracy of this technique is the channel charge injection effect and clock feed-through coming from the switches and finite comparator gain. Also, the comparator has to be stable in unity-gain closed-loop configuration.

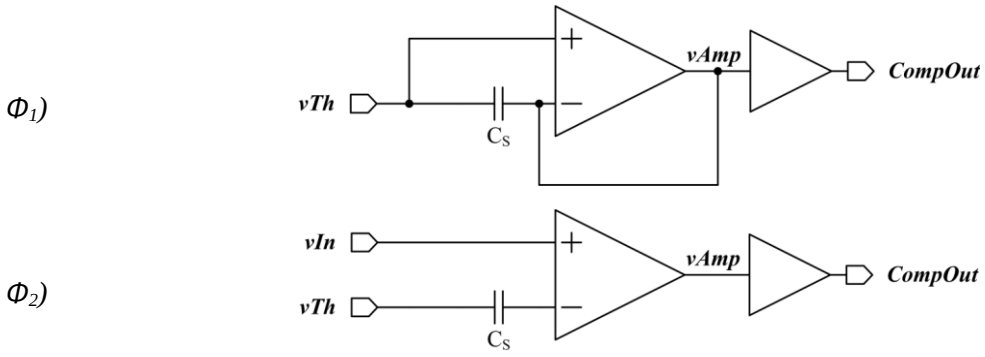

Fig. 4.4 Operation of a comparator with input offset storage: Φ_1 – offset compensation phase, Φ_2 – comparison phase.

The comparator electrical scheme is presented in Fig. 4.5. It is composed of two stages: a telescopic cascode and a common source amplifier. For the offset compensation purpose only the output of the first stage is used, so it is stable in closed-loop operation. The transistor's dimensions and bias currents are presented in Table 4.2 and Table 4.3 respectively. The simulated telescopic cascode voltage gain and bandwidth for the valid input voltage range are presented in Table 4.4.

The offset storage capacitor C_S is chosen to match the comparator's area. In 180 nm technology it is implemented as a MIMCAP with value of 135 fF, while in 40 nm technology as a MOMCAP with value of 40 fF.

In 40 nm process, to minimize gate and leakage currents, only thick oxide transistors were used.

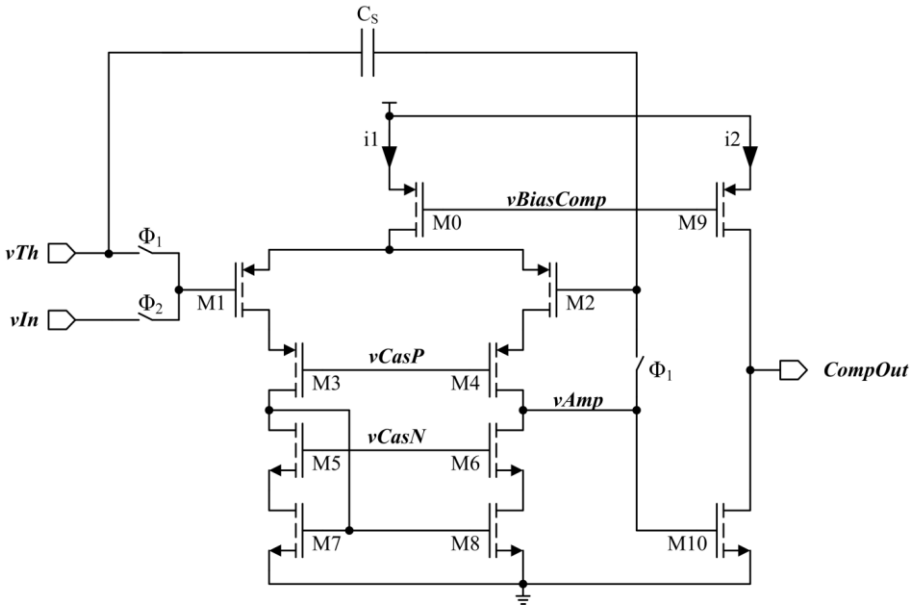

Fig. 4.5 Comparator electrical diagram.

Table 4.2 Comparator's transistor dimensions.

Transistor	W/L [µm]	
	180 nm	**40 nm**
M0	4/1	2.4/0.8
M1, M2	2/0.8	1.2/0.3
M3, M4	2/0.8	1.2/0.3
M5, M6	2/1	1.2/0.5
M7, M8	2/1	1.2/0.5
M9	2/1	0.6/0.8
M10	2/1	0.6/0.3

Table 4.3 Comparator's bias currents.

Current	180 nm	40 nm
i1	1.0 µA	0.4 µA
i2	0.5 µA	0.1 µA

Table 4.4 Comparator's core parameters.

	180 nm	40 nm
Gain	1200 V/V	375 V/V
BW	32.2 kHz	358.1 kHz
GBW	38.6 M	134 M

4.3.3 Thermometer to binary encoder

The thermometer to binary decoder is designed in similar way as described in section 2.3.4. The only difference is that the logic is not distributed uniformly across all comparators, but placed in a single block. Thereby it is more convenient to synthesize it with help of the dedicated software.

4.3.4 Layout

The layout comparison of both ADC's cores with their dimensions are presented in scale in Fig. 4.6. Both layouts are arranged in a similar manner. The comparator array and binary encoder are placed as an isolated blocks, with separate power lines and guard rings, to avoid interference from the digital part to the signal path.

The binary encoder in 180 nm technology was synthesized using the Cadence RTL Compiler and Encounter software. However, in the 40 nm technology, due to the lack of required gate libraries, the encoder block was designed in full custom manner, maintaining identical functionality as the 180 nm counterpart. Additionally, the size ratio of the digital part to analog part decreased from 71% in 180 nm technology to 47% in 40 nm technology, which confirms a moderate scaling for analog blocks and good scaling for digital blocks with the technology progress.

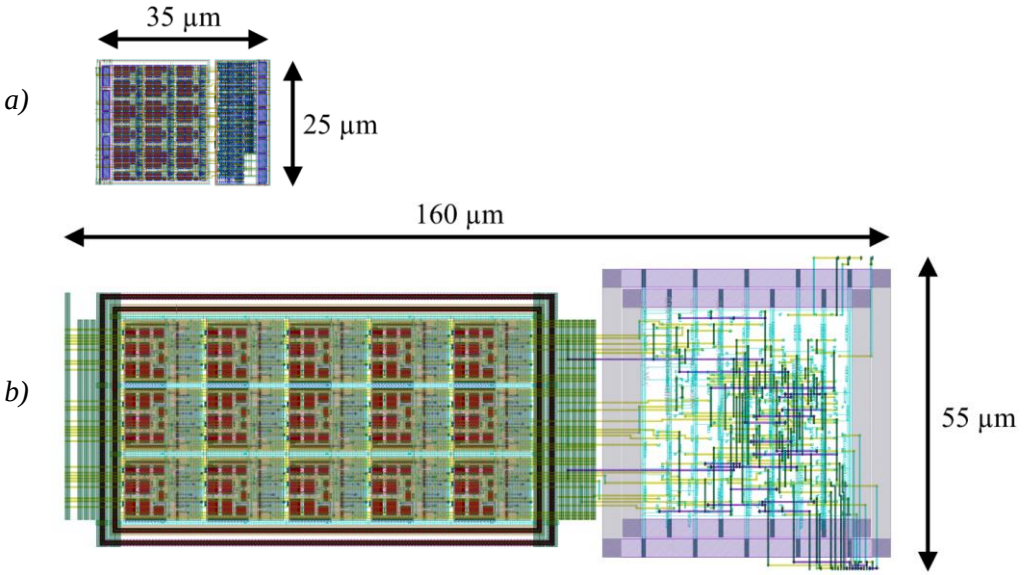

Fig. 4.6 Comparison of ADC's core layouts (in scale): a) 40 nm, b) 180 nm.

4.4 Measurement results

Both chips were manufactured and experimentally characterized. Tests were conducted using NI-RIO9636 measurement system and a dedicated, custom mixed-signal circuit test board. Three prototype chips for both technologies were tested. The sampling rate during all tests was set to 5 MHz.

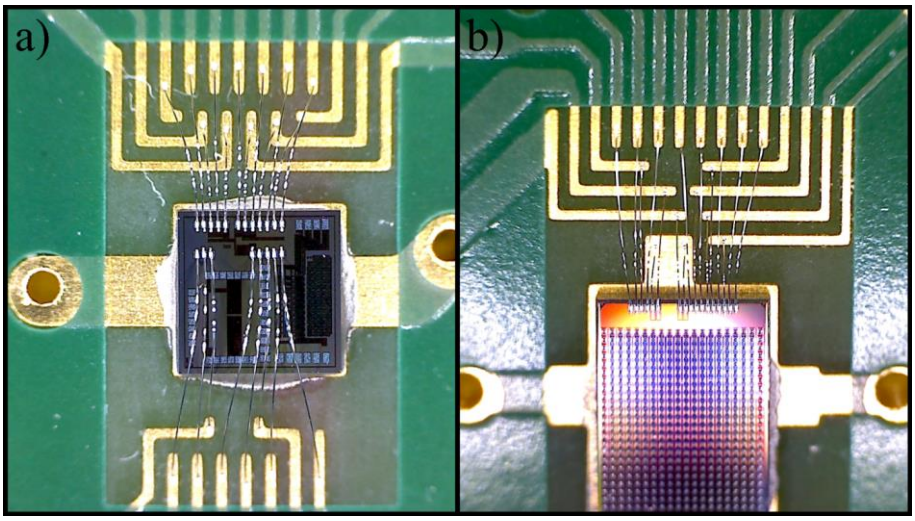

Fig. 4.7 Test chips photographs: a) 180 nm, b) 40 nm.

4.4.1 Offset voltage correction

To measure the performance of the implemented technique, the offset voltage of each comparator has been tested independently, with and without (storage capacitor shorted) offset voltage correction active, by the input signal amplitude scan (see section 2.4.1). The measurement results of 3 ASIC prototypes manufactured in the 180 nm and 40 nm technologies are presented in Fig. 4.8 and Fig. 4.9 respectively.

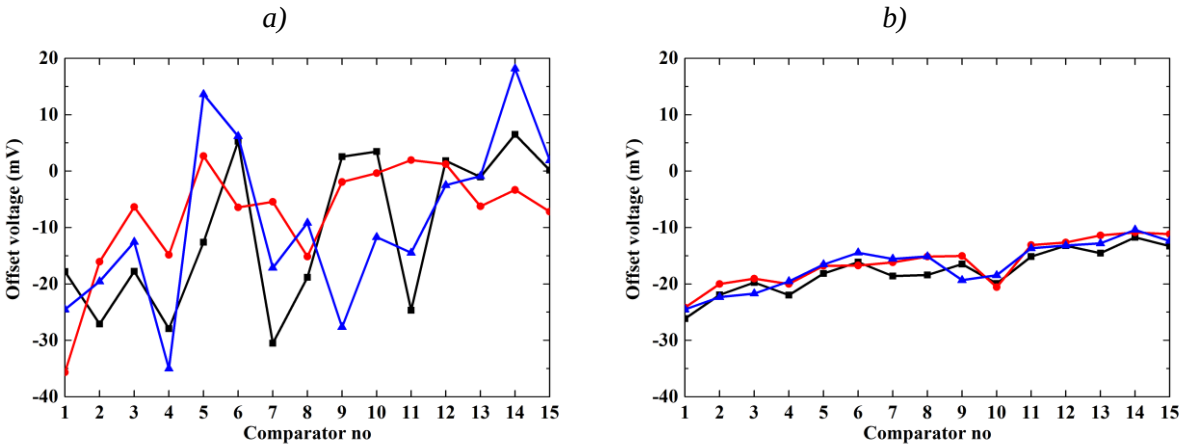

Fig. 4.8 Offset voltage for the 180 nm chips: a) before correction, b) after correction.

For the 180 nm chip, the plot shows clear improvement in the offset voltage standard deviation. However, there is a noticeable dependence between the threshold voltage and the compensated offset voltage value. Additional simulations indicate that the issue is related to the dynamic performance of the comparator, and caused by too low bandwidth of the used cascode.

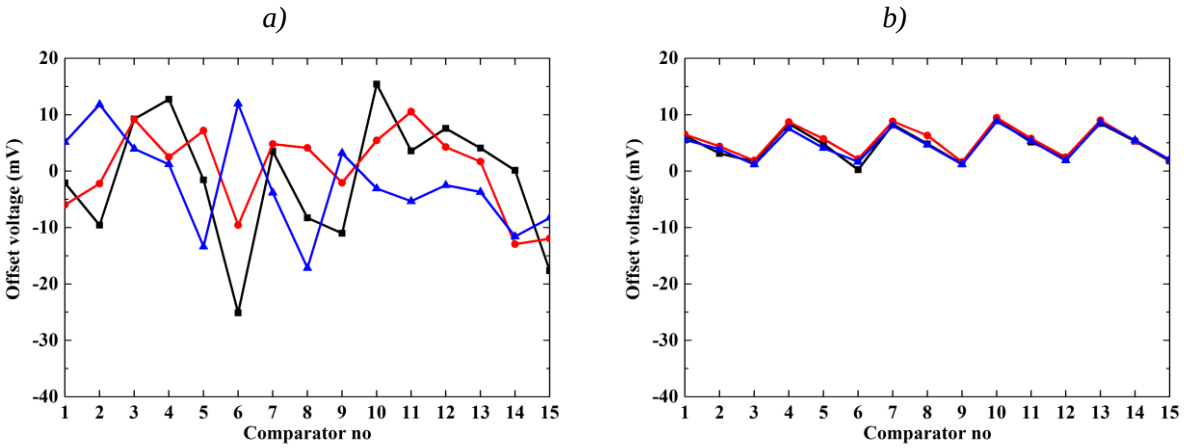

Fig. 4.9 Offset voltage for the 40 nm chips: a) before correction, b) after correction.

In the case of the 40 nm chip, the plot shows a distinctive saw-tooth pattern. It corresponds to the placement of the comparators in the layout, where comparators no. 1, 4, 7, 10 and 13 belongs to the first column, comparators no. 2, 5, 8, 11 and 14 to the second one, etc. The first investigation shows that the main reason of such behavior is layout-related.

The results of the offset correction test are summarized in Table 4.5. The offset voltage standard deviation was computed for every comparator separately and then averaged for both technologies.

Table 4.5 Offset voltage standard deviation.

	180 nm	**40 nm**
Before correction	8.46 mV	7.7 mv
After correction	1.23 mV	0.46 mV

4.4.2 ADC performance

In order to measure the ADC nonlinearity, a ramp test was carried out with offset voltage correction active. The results are shown in Fig. 4.10 and Fig. 4.11 for the 180 nm and 40 nm chips respectively.

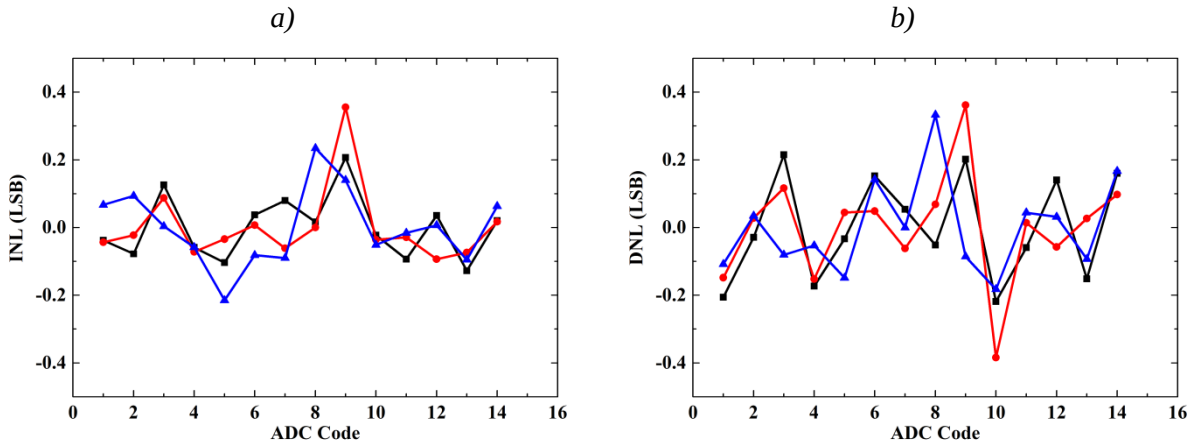

Fig. 4.10 Nonlinearity for the 180 nm chips: a) integral, b) differential.

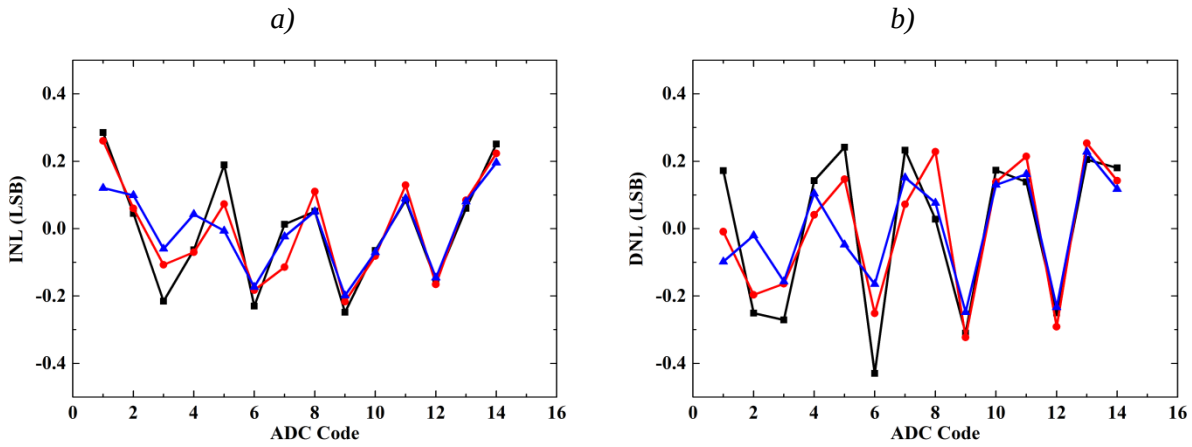

Fig. 4.11 Nonlinearity for the 40 nm chips: a) integral, b) differential.

Finally, the sinewave FFT test was performed to measure the effective number of bits (ENOB) – derived from signal to noise and distortion ratio – and compute the figure of merit (FoM). Due to the limitation in the update rate of the used external reference DAC the output ADC data was decimated by a factor of 40, resulting in a sample frequency of 125 kS/s. A full-scale sinewave of near-Nyquist frequency about 62 kHz was used as an input. The obtained signal spectra are presented in Fig. 4.12.

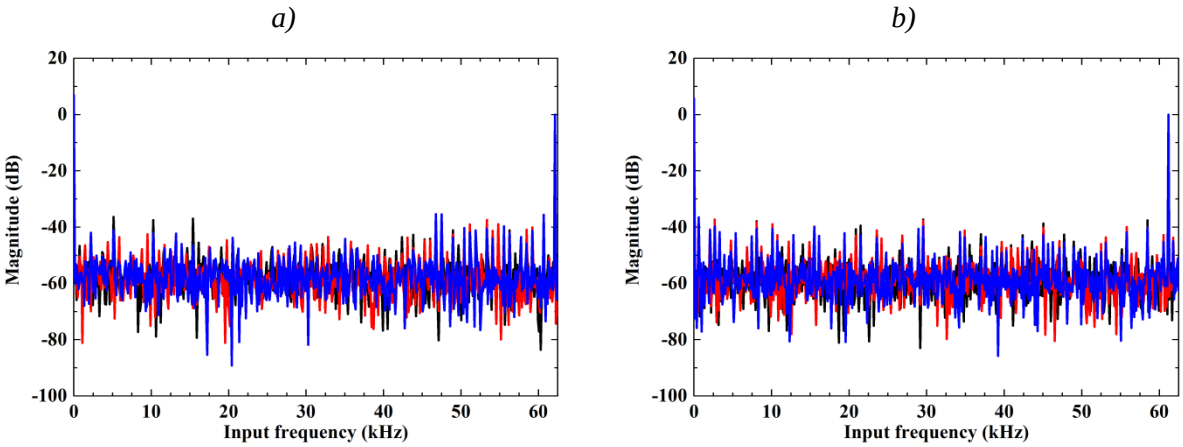

Fig. 4.12 Signal spectrum of near-Nyquist frequency, sampled at 125 kS/s, 5 MHz clock frequency: a) 180 nm chips, b) 40 nm chips.

4.5 Summary

The design and experimental measurement results of two flash ADC prototypes of identical architecture, with small area occupancy, manufactured in different technologies were presented [49]. Migrating the design from 180 nm to 40 nm CMOS process allowed to decrease circuit area over nine times and power consumption three times, maintaining the same performance.

The circuits were designed for X-ray imaging pixel systems. The prototype in well-established 180 nm technology could be integrated in systems with pixel pitch of 170 µm, however its relatively large area occupancy and power consumption could limit the functionality of the system.

The prototype in a modern 40 nm CMOS process has significantly lower area occupancy and power consumption and can be feasibly implemented in future ROICs of pixel architecture with pixel size in the order of 100 µm × 100 µm. The sampling rate allows it to operate with the radiation intensity of up to few megahits per channel per second.

Table 4.6 ADCs parameters summary.

	180 nm	**40 nm**
Resolution	4 bits	
Sampling rate	5 MS/s	
Supply voltage	1.2 V	
Input range	300 mV	
Power	52 µW	17 µW
INL	+0.35/-0.21	+0.28/-0.25
DNL	+0.36/-0.38	+0.25/-0.43
ENOB	3.91	3.86
FoM	686 fJ/conv.step	230 fJ/conv.step
Area	160 µm × 55 µm	35 µm × 25 µm

5. THESIS CONCLUSIONS

The main focus of this thesis was research towards finding ADC architectures and design solutions for implementation in multichannel readout circuits used in radiation detection systems. The emphasis was put especially on the silicon area occupancy, as it is one of the most critical parameters in such systems, and low power consumption of the converter.

A novel trimming system architecture was proposed and implemented in the 5-bit flash ADC array of the STS-XYTER chip, to correct the comparator's offset voltage and arbitrarily shape the ADC's transfer characteristic. The STS-XYTER is a multichannel strip detector readout ASIC for the detection system in the forthcoming CBM experiment at FAIR. The proposed solution, basing on a two-stage architecture built of a global coarse reference and a local fine DAC, allows to reduce the area occupancy of a single trim DAC approximately four times, maintaining its monotonicity. The measurement results confirm the correctness of the design and indicate an improvement in the comparator's offset voltage spread by a factor of 16. To the authors knowledge, such solution has not been reported in the literature before. The ASIC was subject of publication in papers [21] and [30].

Two ADC designs dedicated for pixel systems were proposed. A 7-bit SAR ADC is adequate for medium resolution measurement systems with moderate pixel size. The design has low power consumption of 4.45 μW and achieves very good energy efficiency, with the Walden FoM below 100 fJ/conv.step. The circuit is highly optimized for the lowest area occupancy, measuring only 90 μm × 95 μm which is one of the best results for this resolution range. These parameters make it suitable for application in various measurement systems. The ADC was presented in publication [43].

The second pixel ADC solution, which targets high count rate imaging systems with pixel size of 100 μm × 100 μm and smaller, bases on a 4-bit flash architecture. To achieve the lowest comparator area occupancy, the dynamic offset voltage compensation method is used. The design was implemented in two CMOS technologies: 180 nm and 40 nm. Measurement results indicate an improvement in the offset voltage spread by a factor of 7 and 16 for the 180 nm and 40 nm processes respectively. Additionally, an ultra-low area occupancy and power consumption of the design in 40 nm technology pose a significant step forward towards the inclusion of new functionalities, e.g. compensation of the charge sharing phenomena or colored X-ray, in the future pixel imaging systems. The presented designs were the subjects of publication in papers [46] and [49].

LIST OF FIGURES

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